TPS26750 Technical Reference Manual

Technical Reference Manual

Literature Number: SLVUCR7
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About This Manual

National Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Related Documents

- USB Power Delivery Specification Revision 3.1 www.usb.org/developers/docs
- USB Type-C Cable and Connector Specification Revision 2.0. www.usb.org/developers/docs

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 1

Introduction

1.1 Introduction

1.1.1 Purpose and Scope

This document describes the Host Interface for the TPS26750 Type-C Port Switch / Power Delivery (PD) Controller device.

1.2 PD Controller Host Interface Description

1.2.1 Overview

The PD Controller provides one I2C target. The I2Ct target is meant to be connected to an Embedded Controller (EC).

The Host Interface defines how the registers are accessed from I2C target port and target addresses. Target Address #1 is selected by the customer using the ADCIN1 and ADCIN2 pins on the PD controller. See also Section 6.2 for more details about the target addresses.

The Host Interface provides general status information to the controller of these I2C interfaces about the PD Controller, ability to control the PD Controller, status of USB Type-C® Port and communications to/from a connected device (Port Partner) and/or cable plug through USB PD messages. All Host Interface communication that uses the Unique I2C address is referred to as Unique Address Interface.

The PD Controller supports a register-based Unique Address Interface. Chapter 4 lists the Unique Address Interface registers and provides detailed Unique Address Interface register descriptions.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 and is repeated here in part in Figure 1-1.

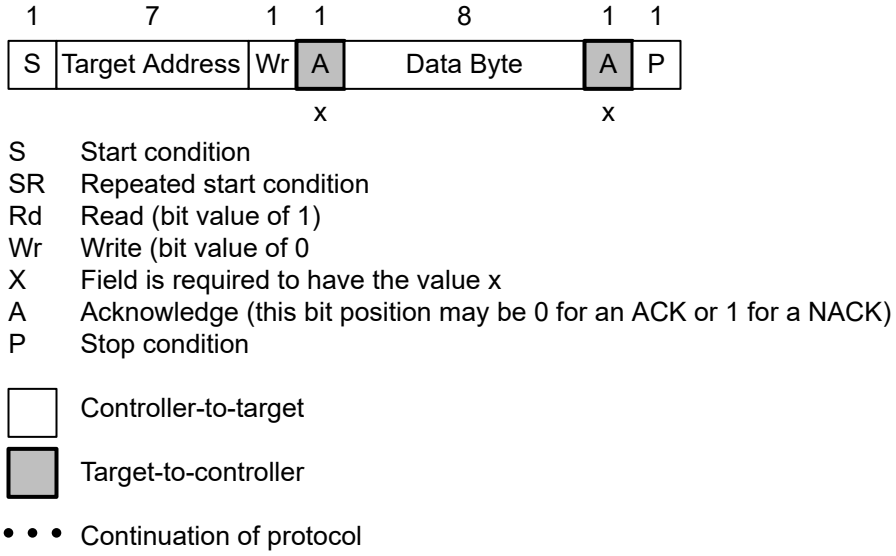

Figure 1-1. I2C Read/Write Protocol Key

1.2.2 Register and field notation

In this document the register names use an ALL CAPS notation, and the field names use a CamelBack notation. For example *TX_SOURCE_CAPS* refers to register 0x32, and *TX_SOURCE_CAPS.numValidPDOs* refers to a specific field in Byte 1 of that register.

Some registers have the same definition, but there are multiple instantiations at different register addresses. The following lists these registers.

- *INT_EVENTx ~ INT_EVENT1* (0x14)
- *INT_MASKx ~ INT_MASK1* (0x16)
- *INT_CLEARx ~ INT_CLEAR1* (0x18)
- *CMDx ~ CMD1* (0x08)
- *DATAx ~ DATA1* (0x09)

In this document, the "x" indicates that it is referring to both instantiations of that register.

1.3 Unique Address Interface

1.3.1 Unique Address Interface Protocol

The Unique Address Interface allows for complex interactions between an I2C controller and a single PD Controller. The I2C target unique address is used to receive or respond to Host Interface protocol commands. Figure 1-2 and Figure 1-3 show the write and read protocols, respectively. The Byte Count used during a register write can be longer than the number of bytes actually written, in other words the controller can issue the stop bit without writing N bytes. Similarly, during a register read, the controller can issue the stop bit before reading all N bytes.

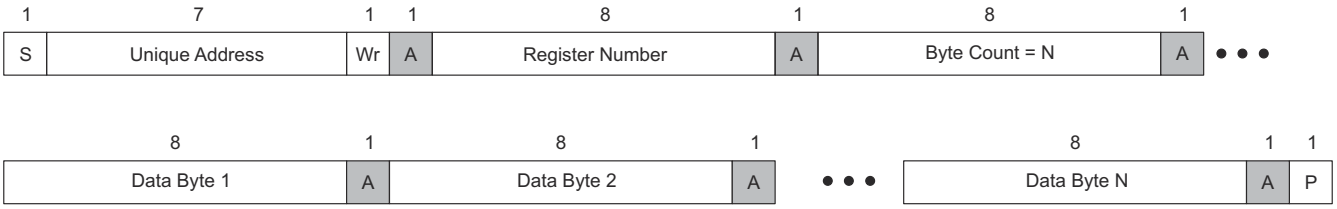

Figure 1-2. I2C Unique Address write register protocol

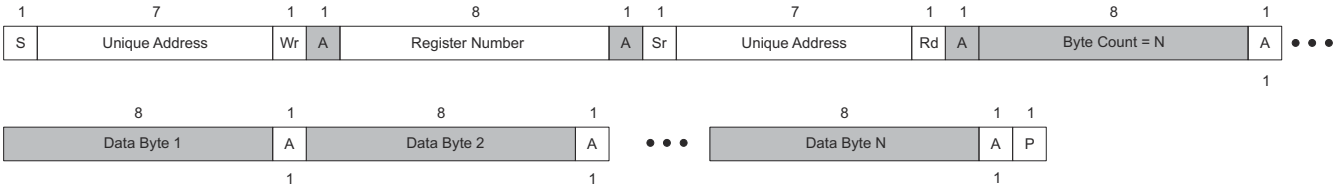

Figure 1-3. I2C Unique Address read register protocol

Chapter 2

PD Controller Policy Modes

2.1 Overview

The PD Controller implements modes for "SRC Policy" (handing out Source contracts), and modes for "SNK Policy" (issuing Requests for Sink contracts).

2.2 Source Policy Mode

The PD Controller uses the *TX_SOURCE_CAPS* register (0x32) to know what PDO(s) to advertise. The PD Controller will automatically respond to Request messages as appropriate, and each port acts independently. The host can dynamically change the *TX_SOURCE_CAPS* register, then issue the 'SSrC' 4CC Task and the PD controller will advertise the new PDO(s).

2.3 Sink Policy Mode

The PD Controller will always prepare its own Request message based on the settings in the *AUTO_NEGOTIATE_SINK* register (0x37) and the *TX_SINK_CAPS* register (0x33). The PD Controller will send its prepared Request message as soon as it is ready. The host can change the *AUTO_NEGOTIATE_SINK* register and/or the *TX_SINK_CAPS* register, then issue the 'GSrC' 4CC Task and the PD controller will re-negotiate the PD contract based on the updated values.

Chapter 3
Register Overview

Note

Some registers contain 'Reserved' fields that should not be overwritten by an I2C Host Controller (EC). To prevent overwriting these 'Reserved' fields the host controller should follow the read-modify-write instruction before configuring any PD registers.

Chapter 4

TPS26750 Registers

Table 4-1 lists the memory-mapped registers for the TPS26750 registers. All register offset addresses not listed in Table 4-1 should be considered as reserved locations and the register contents should not be modified.

Table 4-1. TPS26750 Registers

Offset	Acronym	Register Name	Section
3h	Mode	Mode	Section 4.1
6h	Customer Use	Customer Use	Section 4.2
8h	Command Register for I2Ct	Command Register for I2Ct	Section 4.3
9h	Data Register for CMD1	Data Register for CMD1	Section 4.4
14h	Interrupt Event for I2Ct_IRQ	Interrupt Event for I2Ct_IRQ	Section 4.5
16h	Interrupt Mask for I2Ct_IRQ	Interrupt Mask for I2Ct_IRQ	Section 4.6
18h	Interrupt Clear for I2Ct_IRQ	Interrupt Clear for I2Ct_IRQ	Section 4.7
1Ah	Status	Status	Section 4.8
26h	Power Path Status	Power Path Status	Section 4.9
28h	Port Configuration	Port Configuration	Section 4.10
29h	Port Control	Port Control	Section 4.11
2Dh	Boot Flags	Boot Flags	Section 4.12
30h	Received Source Capabilities	Received Source Capabilities	Section 4.13
31h	Received Sink Capabilities	Received Sink Capabilities	Section 4.14
32h	Transmit Source Capabilities	Transmit Source Capabilities	Section 4.15
33h	Transmit Sink Capabilities	Transmit Sink Capabilities	Section 4.16
34h	Active PDO Contract	Active PDO Contract	Section 4.17
35h	Active RDO Contract	Active RDO Contract	Section 4.18
37h	Autonegotiate Sink	Autonegotiate Sink	Section 4.19
3Fh	Power Status	Power Status	Section 4.20
40h	PD Status	PD Status	Section 4.21
42h	PD3 Configuration	PD3 Configuration	Section 4.22
48h	Received SOP Identity Data Object	Received SOP Identity Data Object	Section 4.23
5Ch	IO Config	IO Config	Section 4.24
69h	Type C State	Type C State	Section 4.25
6Ah	ADC Results	ADC Results	Section 4.26
70h	Sleep Control Register	Sleep Control Register	Section 4.27
72h	GPIO Status	GPIO Status	Section 4.28
77h	Tx Source Capabilities Extended Data Block	Tx Source Capabilities Extended Data Block	Section 4.29
78h	TX Source Info	TX Source Info	Section 4.30
7Ah	Trasmitted PPS Status Data Block	Trasmitted PPS Status Data Block	Section 4.31
7Bh	Transmitted Battery Status Data Objects (BSDO) Register	Transmitted Battery Status Data Objects (BSDO) Register	Section 4.32

Table 4-1. TPS26750 Registers (continued)

Offset	Acronym	Register Name	Section
7Dh	Tx Battery Capabilities	Tx Battery Capabilities	Section 4.33
7Eh	Transmit Sink Capabilities Extended Data Block	Transmit Sink Capabilities Extended Data Block	Section 4.34
98h	Liquid Detection Config	Liquid Detection Config	Section 4.35

Complex bit access types are encoded to fit into small table cells. Table 4-2 shows the codes that are used for access types in this section.

Table 4-2. TPS26750 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

4.1 Mode Register (Offset = 3h) [Reset = 00000000h]

Mode is shown in Table 4-3.

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Indicates the operational state of the port. The PD controller has limited functionality in some modes.

Table 4-3. Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Mode	R	0h	The mode described in 4 ASCII characters. 'APP ' indicates that the PD controller is fully functioning in the application firwmare where all registers are available. 'BOOT' indicates that the PD controller is booting in dead battery. 'PTCH' indicates that the PD controller is in patch mode. Any other values indicates that the PD controller is functioning in limited capacity. In 'BOOT' and 'PTCH' only the follow register addresses are accessible: Mode (0x03), Command (0x09), Data (0x08), Int Event (0x14), Int Mask (0x16), Int Clear (0x18), and Boot Flags (0x2D).

4.2 Customer Use Register (Offset = 6h) [Reset = 0000000000000000h]

Customer Use is shown in Table 4-4.

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These 8 bytes are allocated for customer use as needed. The PD controller does not use this register. This register may be changed during application customization.

Table 4-4. Customer Use Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	Customer Use	R	0h	These 8 bytes are allocated for customer use as needed. The PD controller does not use this register. This register may be changed during application customization.

4.3 Command Register for I2Ct (Offset = 8h) [Reset = 00000000h]

Command Register for I2Ct is shown in Table 4-5.

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Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

Table 4-5. Command Register for I2Ct Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Command	R/W	0h	Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

4.4 Data Register for CMD1 (Offset = 9h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Data Register for CMD1 is shown in Table 4-6.

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Data register for the primary command interface (CMD1).

Table 4-6. Data Register for CMD1 Field Descriptions

Bit	Field	Type	Reset	Description
511-0	Data	R/W	0h	Data register for the primary command interface (CMD1).

4.5 Interrupt Event for I2Ct_IRQ Register (Offset = 14h) [Reset = 00000000000000002000008h]

Interrupt Event for I2Ct_IRQ is shown in Table 4-7.

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Interrupt event bit field for IRQ. If any bit in this register is 1, then the IRQ pin is pulled low. Only the interrupt events enabled in INT_MASK1 (0x16) will be asserted.

Table 4-7. Interrupt Event for I2Ct_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R	0h	Reserved
82	I2C Controller NACked	R	0h	A transaction on the I2C Controller was NACKed.
81	Ready for Patch	R	0h	Device ready for a patch bundle from the host.
80	Patch Loaded	R	0h	Patch was loaded to the device.
79	RESERVED	R	0h	Reserved
78	RESERVED	R	0h	Reserved
77	RESERVED	R	0h	Reserved
76	RESERVED	R	0h	Reserved
75-74	RESERVED	R	0h	Reserved
73	RESERVED	R	0h	Reserved
72	RESERVED	R	0h	Reserved
71	RESERVED	R	0h	Reserved
70	RESERVED	R	0h	Reserved
69-67	RESERVED	R	0h	Reserved
66	MBRD Buffer Ready	R	0h	Receive memory buffer full and ready to be read using the 'MBRd' command.
65	TX Memory Buffer Empty	R	0h	Transmit memory buffer empty.
64	RESERVED	R	0h	Reserved
63	RESERVED	R	0h	Reserved
62	RESERVED	R	0h	Reserved
61	RESERVED	R	0h	Reserved
60	Liquid Detection	R	0h	Asserted when Liquid Detection is detected or removed. Read 0x98 to determine the state of Liquid Detection.
59	RESERVED	R	0h	Reserved
58	RESERVED	R	0h	Reserved
57	Ext DCDC Source Safe State	R	0h	Used for EC controlled battery charger or DC/DC applications to indicate when the PD controller is no longer going to act as a source. This interrupt will be set when acting as a source and receiving/ sending an Accept message to a Power Role Swap.
56	Ext DCDC Sink Safe State	R	0h	Used for EC controlled battery charger or DC/DC applications to indicate when the PD controller is no longer going to act as a sink. This interrupt will be set when acting as a sink and receiving/sending an Accept message to a Power Role Swap. This interrupt will also be set when acting as a sink and recieving an Explicit PD Contract Accept from the connected source.
55	RESERVED	R	0h	Reserved
54	RESERVED	R	0h	Reserved
53	RESERVED	R	0h	Reserved
52	RESERVED	R	0h	Reserved
51	Discover Mode Completed	R	0h	Set when the Discover Modes process has completed.
50	RESERVED	R	0h	Reserved
49	RESERVED	R	0h	Reserved

Table 4-7. Interrupt Event for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
48	RESERVED	R	0h	Reserved
47	RESERVED	R	0h	Reserved
46	Unable to Source Error	R	0h	The Source was unable to increase the voltage to the negotiated voltage of the contract.
45	RESERVED	R	0h	Reserved
44	RESERVED	R	0h	Reserved
43	Plug Early Notification	R	0h	A connection has been detected but not debounced.
42	Sink Transition Completed	R	0h	This event only occurs when in source mode (PD_STATUS.PresentPDRole = 1b). It occurs tSrcTransition (ms) after sending an Accept message to a Request message, just before sending the PS_RDY message.
41-40	RESERVED	R	0h	Reserved
39	Message Data Error	R	0h	An erroneous message was received.
38	Protocol Error	R	0h	An unexpected message was received from the partner device.
37	RESERVED	R	0h	
36	Missing Get Capabalities Message Error	R	0h	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
35	Power Event Occurred Error	R	0h	An OVP, or ILIM event occurred on VBUS. Or a TSD event occurred.
34	Can Provide Voltage or Current Later Error	R	0h	The USB PD Source can provide acceptable voltage and current, but not at the present time. A "wait" message was sent or received.
33	Cannot Provide Voltage or Current Error	R	0h	The USB PD Source cannot provide an acceptable voltage and/or current. A Reject message was sent to the Sink or a Capability Mismatch was received from the Sink.
32	Device Incompatible Error	R	0h	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
31	RESERVED	R	0h	Reserved
30	CMD1 Complete	R	0h	Set whenever a non-zero value in CMD1 register is set to zero or ! CMD.
29-28	RESERVED	R	0h	Reserved
27	PD Status Updated	R	0h	Set whenever contents of PD_STATUS register (0x40) change.
26	Status Updated	R	0h	Set whenever contents of STATUS register (0x1A) change.
25	RESERVED	R	0h	Reserved
24	Power Status Updated	R	0h	Set whenever contents of POWER_STATUS register (0x3F) change.
23	Power Path Switch Changed	R	0h	Set whenever contents of POWER_PATH_STATUS register (0x26) changes.
22	RESERVED	R	0h	Reserved
21	USB Host No Longer Present	R	0h	Set when STATUS.UsbHostPresent transitions to anything other than 11b.
20	USB Host Present	R	0h	Set when STATUS.UsbHostPresent transitions to 11b.
19	RESERVED	R	0h	Reserved
18	Data Swap Requested	R	0h	A DR swap was requested by the Port Partner.
17	Power Swap Requested	R	0h	A PR swap was requested by the Port Partner.
16	RESERVED	R	0h	Reserved
15	Sink Cap Message Received	R	0h	This is asserted when a Sink Capabilities message is received from the Port Partner.
14	Source Capabalities Message Received	R	0h	This is asserted when a Source Capabilities message is received from the Port Partner.

Table 4-7. Interrupt Event for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	New Contract as Provider	R	0h	An RDO from the far-end device has been accepted and the PD Controller is a Source. This is asserted after the PS_RDY message has been sent. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
12	New Contract as Consumer	R	0h	Far-end source has accepted an RDO sent by the PD Controller as a Sink. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
11	RESERVED	R	0h	Reserved
10	RESERVED	R	0h	Reserved
9	Overcurrent	R	0h	Set whenever an Overcurrent field (VBUS or VCONN) in the POWER_PATH_STATUS register (0x26) changes.
8	RESERVED	R	0h	Reserved
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	Data Swap Complete	R	0h	A Data Role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
4	Power Swap Complete	R	0h	A Power role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
3	Plug Insert or Removal	R	1h	USB Plug Status has Changed. See Status register (0x1A) for more plug details.
2	RESERVED	R	0h	Reserved
1	PD Hardreset	R	0h	A PD Hard Reset has been performed. See PD_STATUS.HardResetDetails for more information.
0	RESERVED	R	0h	Reserved

4.6 Interrupt Mask for I2Ct_IRQ Register (Offset = 16h) [Reset = 00000000000000000000h]

Interrupt Mask for I2Ct_IRQ is shown in Table 4-8.

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Interrupt mask bit field for INT_EVENT1. Bytes 1 to 10 of this register needs to be enabled through the Application Customization Tool but Byte 11 (Bits 80-87) are enabled by default.

Table 4-8. Interrupt Mask for I2Ct_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	RESERVED	R/W	0h	
78	RESERVED	R/W	0h	
77	RESERVED	R/W	0h	
76	RESERVED	R/W	0h	
75	RESERVED	R/W	0h	
74	RESERVED	R/W	0h	
73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	
71	RESERVED	R/W	0h	
70	RESERVED	R/W	0h	
69	RESERVED	R/W	0h	
68	RESERVED	R/W	0h	
67	RESERVED	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	RESERVED	R/W	0h	
63	RESERVED	R/W	0h	
62	RESERVED	R/W	0h	
61	RESERVED	R/W	0h	Reserved
60	Liquid Detection	R/W	0h	Liquid Detection
59	RESERVED	R/W	0h	
58	RESERVED	R/W	0h	
57	Ext DCDC Source Safe State	R/W	0h	
56	Ext DCDC Sink Safe State	R/W	0h	
55	RESERVED	R/W	0h	
54	RESERVED	R/W	0h	
53	RESERVED	R/W	0h	
52	RESERVED	R/W	0h	
51	Discover mode Completed	R/W	0h	
50	RESERVED	R/W	0h	
49	RESERVED	R/W	0h	
48	RESERVED	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	

Table 4-8. Interrupt Mask for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
45	RESERVED	R/W	0h	Reserved
44	RESERVED	R/W	0h	
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	RESERVED	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	
36	Missing Get Capabalities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	RESERVED	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	RESERVED	R/W	0h	
24	Power Status Updated	R/W	0h	Set whenever contents of POWER_STATUS register (0x3F) change.
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	RESERVED	R/W	0h	
10	RESERVED	R/W	0h	
9	Overcurrent	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	

Table 4-8. Interrupt Mask for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

4.7 Interrupt Clear for I2Ct_IRQ Register (Offset = 18h) [Reset = 00000000000000000000h]

Interrupt Clear for I2Ct_IRQ is shown in Table 4-9.

Return to the Summary Table.

Interrupt clear bit field for INT_EVENT1. Writing 1 to a specific bit will clear that specific event in INT_EVENT1. Bits set in this register are cleared from INT_EVENT1.

Table 4-9. Interrupt Clear for I2Ct_IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	RESERVED	R/W	0h	
78	RESERVED	R/W	0h	
77	RESERVED	R/W	0h	
76	RESERVED	R/W	0h	
75	RESERVED	R/W	0h	
74	RESERVED	R/W	0h	
73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	
71	RESERVED	R/W	0h	
70	RESERVED	R/W	0h	
69	RESERVED	R/W	0h	
68	RESERVED	R/W	0h	
67	RESERVED	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	RESERVED	R/W	0h	
63	RESERVED	R/W	0h	
62	RESERVED	R/W	0h	
61	RESERVED	R/W	0h	Reserved
60	Liquid Detection	R/W	0h	Liquid Detection
59	RESERVED	R/W	0h	
58	RESERVED	R/W	0h	
57	Ext DCDC Source Safe State	R/W	0h	
56	Ext DCDC Sink Safe State	R/W	0h	
55	RESERVED	R/W	0h	
54	RESERVED	R/W	0h	Reserved
53	RESERVED	R/W	0h	
52	RESERVED	R/W	0h	
51	Discover mode Completed	R/W	0h	
50	RESERVED	R/W	0h	
49	RESERVED	R/W	0h	
48	RESERVED	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	

Table 4-9. Interrupt Clear for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
45	RESERVED	R/W	0h	Reserved
44	RESERVED	R/W	0h	
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	RESERVED	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	
36	Missing Get Capabalities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	RESERVED	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	RESERVED	R/W	0h	
24	Power Status Updated	R/W	0h	Set whenever contents of POWER_STATUS register (0x3F) change.
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	RESERVED	R/W	0h	
10	RESERVED	R/W	0h	
9	Overcurrent	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	

Table 4-9. Interrupt Clear for I2Ct_IRQ Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

4.8 Status Register (Offset = 1Ah) [Reset = 0000000000h]

Status is shown in Table 4-10.

Return to the Summary Table.

Status bit field for non-interrupt events.

Table 4-10. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-34	RESERVED	R	0h	Reserved
33-32	RESERVED	R	0h	Reserved
31	RESERVED	R	0h	Reserved
30	SOC Ack Timeout	R	0h	Indicates whether the attached SoC has responded timely. 0h = SoC has responded timely 1h = SoC has not responded timely
29-28	RESERVED	R	0h	Reserved
27	BIST	R	0h	Indicates if a BIST procedure is in progress. 0h = No BIST in progress 1h = BIST in progress
26	RESERVED	R	0h	Reserved
25-24	Acting as Legacy	R	0h	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device. It can take approximately 10 seconds for the PD controller to determine that it is attached to a legacy source or sink. 0h = PD Controller is not in a legacy (non PD) mode 1h = PD Controller is acting like a legacy sink 2h = PD Controller is acting like a legacy source 3h = Acting as legacy sink due to dead-battery.
23-22	USB Host Present	R	0h	USB host attachment status. 0h = No host present 1h = Attached source is not data capable 2h = Attached source is not USB PD capable 3h = Host present
21-20	VBUS Status	R	0h	Indicates the present state of VBUS. 0h = At vSafe0V (less than 0.8V) 1h = At vSafe5V (4.75V to 5.5V) 2h = Within expected limits 3h = Not within any of the other specified ranges
19-7	RESERVED	R	0h	Reserved
6	Data Role	R	0h	PD controller data role. This is only valid once there is a connection. 0h = Upward-facing port (UFP) 1h = Downward-facing port (DFP)
5	Port Role	R	0h	Current state of PD Controller CCx terminations. This also indicates the PD Controller Power Role, once connected. This bit does not toggle during Unattached.* state transitions. 0h = PD Controller is in the Sink role 1h = PD Controller is Source (CCx pull-up active)
4	Plug Orientation	R	0h	Plug orientation indicator. Indicates port orientation when known (requires connection). 0h = Upside-up orientation (plug CC on CC1) 1h = Upside-down orientation (plug CC on CC2)
3-1	Connection State	R	0h	Details of a connected plug. 0h = No connection 1h = Port is disabled 2h = Audio connection (Ra/Ra) 3h = Debug connection (Rd/Rd) 4h = No connection Ra detected (Ra but no Rd) 5h = Reserved (may be used for Rp/Rp Debug connection) 6h = Connection present no Ra detected 7h = Connection present Ra detected

Table 4-10. Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	Plug Present	R	0h	Status of the plug 0h = No plug is connected 1h = A plug is connected

4.9 Power Path Status Register (Offset = 26h) [Reset = 0000000000h]

Power Path Status is shown in Table 4-11.

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Power Path Status. This is a hardware dependent register.

Table 4-11. Power Path Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-38	Power Source	R	0h	Indicates current PD Controller power source. NOTE: Since the Dead Battery flag forces PD Controller to be powered from VBUS, only 10b is valid when this flag is set. Any other setting indicates that the Dead Battery flag is not set. 0h = Reserved 1h = PD Controller is powered from VIN_3V3 2h = PD Controller is powered from VBUS 3h = Reserved
37-35	RESERVED	R	0h	Reserved
34	PPCable1 Overcurrent	R	0h	PP_CABLE1 overcurrent indicator. Asserted if an overcurrent condition exists on PP_CABLE1 (VCONN).
33-29	RESERVED	R	0h	Reserved
28	PP1 Overcurrent	R	0h	PP5V overcurrent indicator. Asserted if an overcurrent conditions exists on PP1 switch (PP5V).
27-21	RESERVED	R	0h	Reserved
20-18	RESERVED	R	0h	Reserved
17-15	RESERVED	R	0h	Reserved
14-12	PP3 Switch	R	0h	Indicates current state of PP3 (PP_EXT). 0h = PP3 switch disabled 1h = PP3 switch currently disabled due to fault 2h = PP3 switch enabled (system output) 3h = PP3 switch enabled (system input)
11-9	RESERVED	R	0h	Reserved
8-6	PP1 Switch	R	0h	Indicates current state of PP1 switch (PP5V). 0h = PP1 switch disabled 1h = PP1 switch currently disabled due to fault 2h = PP1 switch enabled (system output)
5-2	RESERVED	R	0h	Reserved
1-0	PPCable1 Switch	R	0h	Indicates current state of PP_CABLE1 switch. 0h = PP_CABLE1 switch disabled 1h = PP_CABLE1 switch currently disabled 2h = PP_CABLE1 switch CC1 enabled (system output) 3h = PP_CABLE1 switch CC2 enabled (system output)

4.10 Port Configuration Register (Offset = 28h) [Reset = 00000000000000000000000012E0002h]

Port Configuration is shown in Table 4-12.

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Configuration for port-specific hardware. This register configures hardware that is specific for each port and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by Application Customization.

Table 4-12. Port Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
135-130	RESERVED	R/W	0h	Reserved
129-128	RESERVED	R/W	0h	Reserved
127-96	RESERVED	R/W	0h	Reserved
95-80	RESERVED	R/W	0h	Reserved
79-73	RESERVED	R/W	0h	Reserved
72	RESERVED	R/W	0h	Reserved
71-64	RESERVED	R/W	0h	Reserved
63-48	RESERVED	R/W	0h	Reserved
47-32	RESERVED	R/W	0h	Reserved
31	RESERVED	R/W	0h	Reserved
30-29	APDO ILIM Over Shoot	R/W	0h	Current limit overshoot for APDO contracts. Configures the current limit overshoot when power role is source and negotiated PD contract is variable type. This field is used to increase the current limit configuration of a supported BQ device. 0h = 25mA overshoot for APDO current 1h = 50mA above negotiated variable PDO current 2h = 75mA above negotiated variable PDO current 3h = Static 2900mA current limit
28-27	APDO VBUS UVP Threshold	R/W	0h	VBUS UVP threshold for APDO contracts. Configures the VBUS UVP threshold when power role is source and negotiated PDO contract is variable type. 0h = 90% below negotiated variable PDO voltage 1h = 88% below negotiated variable PDO voltage 2h = 92% below negotiated variable PDO voltage 3h = Reserved
26-24	VBUS Sink UVP Trip HV	R/W	1h	VBUS disconnect when power role is sink. The disconnect threshold is set to (1-VBUS_SinkUvpTripHV)*(min expected VBUS). The 000b setting follows the USB-C specification requirements. Use a non-zero value for additional margin. 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40% 7h = 50%
23-22	RESERVED	R/W	0h	Reserved
21-20	OVP for PP5V	R/W	2h	VBUS OVP settings while sourcing from PP1 (PP5V). See data-sheet for voltage range. 0h = Use setting 0: 5.25 V 1h = Use setting 1: 5.5 V 2h = Use setting 2: 5.8 V 3h = Use setting 3: 6.1 V
19-18	RESERVED	R/W	0h	Reserved

Table 4-12. Port Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	VBUS OVP Usage	R/W	2h	OVP configuration settings. These two bits are used to select the OVP trip-point. The PD controller automatically computes the lowest threshold that does not overlap with the expected maximum voltage (including maximum tolerance allowed by USB PD specification). The OVP trip-point will be set at the selected percentage of the computed threshold. 0h = 100% 1h = 105% 2h = 111% 3h = 114%
15	RESERVED	R/W	0h	Reserved
14-13	USB3 Rate	R/W	0h	USB3 configuration. 0h = USB3 not supported 1h = USB3 Gen1 signaling rate supported 2h = USB3 Gen2 signaling rate supported 3h = Reserved
12	RESERVED	R/W	0h	
11	USB Communication Capable	R/W	0h	USB communications capable. Assert this bit in systems that are USB communications capable.
10	Disable PD	R/W	0h	Assert this bit to disable USB PD.
9-8	TypeC Support Options	R/W	0h	Configuration for optional features. This register controls whether optional Type-C state machine states are supported. NOTE: These states are mutually-exclusive and these options only exist when specific Type-C state machines are used. 0h = No Type-C optional states are supported 1h = Try.SRC state is supported as a DRP 2h = Try.SNK state is supported as a DRP 3h = Reserved
7-2	RESERVED	R/W	0h	Reserved
1-0	TypeC State machine	R/W	2h	Configuration of the Type-C State machine. This fields sets the default Type-C state of the PD controller. 0h = Sink state machine only 1h = Source state machine only 2h = DRP state machine 3h = Disabled

4.11 Port Control Register (Offset = 29h) [Reset = 00815152h]

Port Control is shown in Table 4-13.

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Configuration bits affecting system policy. These bits may change during normal operation and are used for controlling the respective port. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. Initialized by Application Customization.

Table 4-13. Port Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Charger Detect Enable	R/W	0h	Configure the types of legacy chargers to detect. 0h = Do not detect any legacy chargers 1h = Detect BC 1.2 chargers 2h = Reserved 3h = Detect BC 1.2 and proprietary legacy chargers
29	RESERVED	R/W	0h	Reserved
28-26	Charger Advertise Enable	R/W	0h	Configure the types of legacy chargers to emulate. 0h = Do not emulate any legacy charger 1h = BC 1.2 CDP only 2h = BC 1.2 DCP only 3h = Reserved 4h = Reserved 5h = DCP Auto 1 (2.7V and DCP) 6h = DCP Auto 2 (1.2V 2.7V and DCP) 7h = Reserved
25	DCD Enable	R/W	0h	Enable for Data-Contact Detection. Assert this bit to enable Data Contact Detect as defined by BC 1.2 for sinks.
24	Resistor 15k Present	R/W	0h	Configure D+ and D- termination. Assert this bit if there is a 15kOhm pull-down on D+ and D- (USB2.0 Host Phy pull-downs enabled). This should not be used for DCP or DCP Auto modes. 0h = System does NOT have 15 kOhm pull-down 1h = System has 15 kOhm pull-down
23	RESERVED	R/W	0h	Reserved
22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	0h	Reserved
20	Enable Current Monitor	R/W	0h	Assert this bit to enable the current monitor (peak and average) that are read from the ADC_RESULTS register. While asserted the PD controller will remain in the active power mode.
19	Unconstrained Power	R/W	0h	External power configuration. This also sets the Unconstrained Power bit defined by USB PD. When this bit is changed from 1 to 0 the PD controller will not attempt a power role swap with the Port Partner. If a power role swap is desired the host should issue a 'SWSr' 4CC command. 0h = No external power 1h = External power present
18	RESERVED	R/W	0h	Reserved
17	RESERVED	R/W	0h	Reserved
16	RESERVED	R/W	0h	Reserved
15	Initiate Swap to DFP	R/W	0h	Configure DR_Swap to DFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as UFP.
14	Process Swap to DFP	R/W	1h	Configure response to DR_Swap to DFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a DFP. Otherwise, the PD Controller will reject such a request.

Table 4-13. Port Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	Initiate Swap to UFP	R/W	0h	Configure DR_Swap to UFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as DFP.
12	Process Swap to UFP	R/W	1h	Configure response to DR_Swap to UFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a UFP. Otherwise, the PD Controller will reject such a request.
11	RESERVED	R/W	0h	Reserved
10	RESERVED	R/W	0h	Reserved
9	RESERVED	R/W	0h	Reserved
8	RESERVED	R/W	0h	Reserved
7	Initiate Swap to Source	R/W	0h	Configure PR_Swap to source initiation. If this bit is asserted, the PD Controller automatically initiates and sends PR_Swap requests to the Port Partner when appropriate if presently operating as Sink (C/P).
6	Process Swap to Source	R/W	1h	Configure response to PR_Swap to source. If this bit is asserted, the PD Controller will automatically accept a PR_Swap request to become a Source. Otherwise, the PD Controller will reject such a request.
5	Initiate Swap to Sink	R/W	0h	Configure PR_Swap to sink initiation. If this bit is asserted, the PD Controller automatically initiates and sends PR_Swap requests to the Port Partner when appropriate if presently operating as Source (P/C).
4	Process Swap to Sink	R/W	1h	Configure response to PR_Swap to sink. If this bit is asserted, the PD Controller will automatically accept a PR_Swap request to become a Sink. Otherwise, the PD Controller will reject such a request.
3-2	RESERVED	R/W	0h	Reserved
1-0	TypeC Current	R/W	2h	Type-C Current advertisement. This setting is ignored if a Source role is not enabled and active. This setting is also ignored during an explicit USB PD contract, where the Rp value is used for collision avoidance as required by the USB PD specification. Note that when PP5V is low, the FW will only use the default Type-C current regardless of the value in this field. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Reserved

4.12 Boot Flags Register (Offset = 2Dh) [Reset = 0000000000h]

Boot Flags is shown in Table 4-14.

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Detailed status of boot process. This register provides details on PD Controller boot flags, Customer OTP configuration, and silicon revision

Table 4-14. Boot Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	Revision ID	R	0h	Revision ID for the PD controller.
31-29	Patch Config Source	R	0h	Source of patch configuration. This field indicates the source of the configuration patch that has been successfully loaded. 0h = No configuration has been loaded 4h = Reserved 5h = A configuration has been loaded from EEPROM 6h = A configuration has been loaded from I2C 7h = Reserved
28-27	RESERVED	R	0h	Reserved
26-25	RESERVED	R	0h	
24	RESERVED	R	0h	Reserved
23-20	RESERVED	R	0h	Reserved
19	System TSD	R	0h	System thermal shut-down indicator. This bit is asserted if the PD controller is rebooting after the system thermal sensor caused a reset.
18	RESERVED	R	0h	Reserved
17	RESERVED	R	0h	Reserved
16-14	RESERVED	R	0h	Reserved
13	Region 1 CRC Fail	R	0h	Region 1 CRC status indicator. This bit is asserted when the CRC of data read from Region 1 of EEPROM memory failed.
12	Region 0 CRC Fail	R	0h	Region 0 CRC status indicator. This bit is asserted when the CRC of data read from Region 0 of EEPROM memory failed.
11	RESERVED	R	0h	Reserved
10	Patch Download Error	R	0h	Asserted when a patch download error occurs.
9	Region 1 EEPROM Error	R	0h	Region 1 status indicator. This bit is asserted when an error occurred attempting to read Region 1 of EEPROM memory. A retry may have been successful.
8	Region 0 EEPROM Error	R	0h	Region 0 status indicator. This bit is asserted when an error occurred attempting to read Region 0 of EEPROM memory. A retry may have been successful.
7	Region 1 Invalid	R	0h	Region 1 header status indicator. This bit is asserted when Region 1 header of the EEPROM memory was invalid.
6	Region 0 Invalid	R	0h	Region 0 header status indicator. This bit is asserted when Region 0 header of the EEPROM memory was invalid.
5	Region 1	R	0h	Region 1 attempted indicator. This bit is asserted when Region 1 of the EEPROM memory was attempted.
4	Region 0	R	0h	Region 0 attempted indicator. This bit is asserted when Region 0 of the EEPROM memory was attempted.
3	I2C EEPROM Present	R	0h	EEPROM presence indicator. This bit is asserted when an EEPROM device was discovered during boot.
2	Dead Battery Flag	R	0h	Dead Battery flag indicator. This bit is asserted when the PD Controller booted in dead-battery mode.
1	RESERVED	R	0h	Reserved
0	Patch Header Error	R	0h	Asserted when a patch bundle header errors.

4.13 Received Source Capabilities Register (Offset = 30h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Received Source Capabilities is shown in Table 4-15.

Return to the Summary Table.

Received Source Capabilties. This register stores latest Source Capabilities message received over BMC.

Table 4-15. Received Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-392	Source PDO 13	R	0h	EPR Sixth Source Capabilities PDO received
391-360	Source PDO 12	R	0h	EPR Fifth Source Capabilities PDO received
359-328	Source PDO 11	R	0h	EPR Fourth Source Capabilities PDO received
327-296	Source PDO 10	R	0h	EPR Third Source Capabilities PDO received
295-264	Source PDO 9	R	0h	EPR Second Source Capabilities PDO received
263-232	Source PDO 8	R	0h	EPR First Source Capabilities PDO received
231-200	Source PDO 7	R	0h	Seventh Source Capabilities PDO received
199-168	Source PDO 6	R	0h	Sixth Source Capabilities PDO received
167-136	Source PDO 5	R	0h	Fifth Source Capabilities PDO received
135-104	Source PDO 4	R	0h	Fourth Source Capabilities PDO received
103-72	Source PDO 3	R	0h	Third Source Capabilities PDO received
71-40	Source PDO 2	R	0h	Second Source Capabilities PDO received
39-8	Source PDO 1	R	0h	First Source Capabilities PDO received
7	RESERVED	R	0h	Reserved
6	Last Src Cap Received is EPR	R	0h	Flag showing if the last received Source Capability is an EPR capability.
5-3	Number of Valid EPR PDOs	R	0h	Number of valid EPR PDOs in this register. Each EPR PDO is 4 bytes. (max of 6)
2-0	Number Valid PDOs	R	0h	Number of valid SPR PDOs in this register. Each PDO is 4 bytes. (max of 7)

4.14 Received Sink Capabilities Register (Offset = 31h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Received Sink Capabilities is shown in Table 4-16.

Return to the Summary Table.

Received Sink Capabilities. This register stores latest Sink Capabilities message received over BMC.

Table 4-16. Received Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-392	Sink PDO 13	R	0h	EPR Sixth Sink Capabilities PDO received
391-360	Sink PDO 12	R	0h	EPR Fifth Sink Capabilities PDO received
359-328	Sink PDO 11	R	0h	EPR Fourth Sink Capabilities PDO received
327-296	Sink PDO 10	R	0h	EPR Third Sink Capabilities PDO received
295-264	Sink PDO 9	R	0h	EPR Second Sink Capabilities PDO received
263-232	Sink PDO 8	R	0h	EPR First Sink Capabilities PDO received
231-200	Sink PDO 7	R	0h	Seventh Sink Capabilities PDO received
199-168	Sink PDO 6	R	0h	Sixth Sink Capabilities PDO received
167-136	Sink PDO 5	R	0h	Fifth Sink Capabilities PDO received
135-104	Sink PDO 4	R	0h	Fourth Sink Capabilities PDO received
103-72	Sink PDO 3	R	0h	Third Sink Capabilities PDO received
71-40	Sink PDO 2	R	0h	Second Sink Capabilities PDO received
39-8	Sink PDO 1	R	0h	First Sink Capabilities PDO received
7	RESERVED	R	0h	Reserved
6	Last Sink Cap Received Is EPR	R	0h	Flag showing if the last received Sink Capability is an EPR capability.
5-3	RX Sink Num Valid EPR PDOs	R	0h	Number of valid EPR PDOs in this register. Each EPR PDO is 4 bytes. (max of 6)
2-0	Number Valid PDOs	R	0h	Number of valid SPR PDOs in this register. Each PDO is 4 bytes. (max of 7)

4.15 Transmit Source Capabilities Register (Offset = 32h) [Reset = 0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000002C2601912C2AA801h]

Transmit Source Capabilities is shown in Table 4-17.

Return to the Summary Table.

Source Capabilities for sending. This register stores PDOs and settings for outgoing Source Capabilities PD messages. Initialized by Application Customization.

Table 4-17. Transmit Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
503-485	RESERVED	R/W	0h	Reserved
484	RESERVED	R/W	0h	Reserved
483	RESERVED	R/W	0h	Reserved
482	RESERVED	R/W	0h	Reserved
481	RESERVED	R/W	0h	Reserved
480	RESERVED	R/W	0h	Reserved
479	RESERVED	R/W	0h	Reserved
478	RESERVED	R/W	0h	Reserved
477	RESERVED	R/W	0h	Reserved
476	RESERVED	R/W	0h	Reserved
475	RESERVED	R/W	0h	Reserved
474	RESERVED	R/W	0h	Reserved
473	RESERVED	R/W	0h	Reserved
472	RESERVED	R/W	0h	Reserved
471-452	RESERVED	R/W	0h	Reserved
451-450	RESERVED	R/W	0h	Reserved
449-448	RESERVED	R/W	0h	Reserved
447-446	RESERVED	R/W	0h	Reserved
445-444	RESERVED	R/W	0h	Reserved
443-442	RESERVED	R/W	0h	Reserved
441-440	RESERVED	R/W	0h	Reserved
439-408	TX Source PDO 13	R/W	0h	EPR Sixth Source Capabilities PDO content.
407-376	TX Source PDO 12	R/W	0h	EPR Fifth Source Capabilities PDO content.
375-344	TX Source PDO 11	R/W	0h	EPR Fourth Source Capabilities PDO content.
343-312	TX Source PDO 10	R/W	0h	EPR Third Source Capabilities PDO content.
311-280	TX Source PDO 9	R/W	0h	EPR Second Source Capabilities PDO content.
279-248	TX Source PDO 8	R/W	0h	EPR First Source Capabilities PDO content.
247-216	TX Source PDO 7	R/W	0h	SPR Seventh Source Capabilities PDO contents.
215-184	TX Source PDO 6	R/W	0h	SPR Sixth Source Capabilities PDO contents.
183-152	TX Source PDO 5	R/W	0h	SPR Fifth Source Capabilities PDO contents.
151-120	TX Source PDO 4	R/W	0h	SPR Fourth Source Capabilities PDO contents.
119-88	TX Source PDO 3	R/W	0h	SPR Third Source Capabilities PDO contents.
87-56	TX Source PDO 2	R/W	2Ch	SPR Second Source Capabilities PDO contents.
55-24	TX Source PDO 1	R/W	2601912Ch	SPR First Source Capabilities PDO contents.
23-22	RESERVED	R/W	0h	Reserved
21-20	RESERVED	R/W	0h	Reserved
19-18	RESERVED	R/W	0h	Reserved

Table 4-17. Transmit Source Capabilities Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	RESERVED	R/W	0h	Reserved
15-14	RESERVED	R/W	0h	Reserved
13-12	RESERVED	R/W	0h	Reserved
11-10	RESERVED	R/W	0h	Reserved
9-8	Power Path for PDO 1	R/W	0h	Configures which PP to use for PDO1. 0h = PP5V is used for this PDO 2h = PP_EXT is used for this PDO
7-6	RESERVED	R/W	0h	Reserved
5-3	TX Source Num Valid EPR PDOs	R/W	0h	Number of valid EPR PDOs in this register. Each EPR PDO is 4 bytes. (max of 6)
2-0	Number Valid PDOs	R/W	1h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

4.16 Transmit Sink Capabilities Register (Offset = 33h) [Reset = 000000000000000000000000000000000000000000000000000000000000000000000000000000000000002D12C3601912C04h]

Transmit Sink Capabilities is shown in Table 4-18.

Return to the Summary Table.

Sink Capabilities for sending. This register stores PDOs for outgoing Sink Capabilities USB PD messages. Initialized by Application Customization. The PD controller transmits the contents of this register as a Sink_Capabilities message after receiving a Get_Sink_Cap message unless its configuration or USB PD rules require a different response in the context. Writes to this register have no immediate effect. The PD controller updates and uses this register each time it needs to send a Sink Capabilities message.Each PDO in this TX_SINK_CAPS register follows the definition from the USB PD specification. For more details on the meaning of each field refer to the USB PD specification.

Table 4-18. Transmit Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-392	TX Sink PDO 13	R/W	0h	EPR Sixth Sink Capabilities PDO contents.
391-360	TX Sink PDO 12	R/W	0h	EPR Fifth Sink Capabilities PDO contents.
359-328	TX Sink PDO 11	R/W	0h	EPR Fourth Sink Capabilities PDO contents.
327-296	TX Sink PDO 10	R/W	0h	EPR Third Sink Capabilities PDO contents.
295-264	TX Sink PDO 9	R/W	0h	EPR Second Sink Capabilities PDO contents.
263-232	TX Sink PDO 8	R/W	0h	EPR First Sink Capabilities PDO contents.
231-200	TX Sink PDO 7	R/W	0h	SPR Seventh Sink Capabilities PDO contents.
199-168	TX Sink PDO 6	R/W	0h	SPR Sixth Sink Capabilities PDO contents.
167-136	TX Sink PDO 5	R/W	0h	SPR Fifth Sink Capabilities PDO contents.
135-104	TX Sink PDO 4	R/W	0h	SPR Fourth Sink Capabilities PDO contents.
103-72	TX Sink PDO 3	R/W	0h	SPR Third Sink Capabilities PDO contents.
71-40	TX Sink PDO 2	R/W	0002D12Ch	SPR Second Sink Capabilities PDO contents.
39-8	TX Sink PDO 1	R/W	3601912Ch	SPR First Sink Capabilities PDO contents.
7-6	RESERVED	R/W	0h	Reserved
5-3	TX Sink Num Valid EPR PDOs	R/W	0h	Number of valid EPR PDOs in this register. Each EPR PDO is 4 bytes. (max of 6)
2-0	Number Valid PDOs	R/W	4h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

4.17 Active PDO Contract Register (Offset = 34h) [Reset = 000000000000h]

Active PDO Contract is shown in Table 4-19.

Return to the Summary Table.

Power data object for active contract. This register stores PDO data for the current explicit USB PD contract, or all zeroes if no contract.

Table 4-19. Active PDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
47-42	RESERVED	R	0h	Reserved
41-32	First PDO Control Bits	R	0h	Contains bits 29:20 of the first PDO. It does not matter which PDO was selected, this field is always drawn from the first PDO.
31-0	Active PDO	R	0h	Power data object. This field contains the contents of the PDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

4.18 Active RDO Contract Register (Offset = 35h) [Reset = 00000000000000000000000000h]

Active RDO Contract is shown in Table 4-20.

Return to the Summary Table.

Power data object for the active contract. This register stores the RDO of the current explicit USB PD contract, or all zeroes if no contract.

Table 4-20. Active RDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
96-95	RESERVED	R	0h	Reserved
95-32	RESERVED	R	0h	Reserved
31-28	Object Position	R	0h	As defined by USB PD.
27	Give Back Flag	R	0h	As defined by USB PD.
26	Capability Missmatch	R	0h	As defined by USB PD.
25	USB Communication Capable	R	0h	As defined by USB PD.
24	No USB Suspend	R	0h	As defined by USB PD.
23	Unchunked Supported	R	0h	As defined by USB PD.
22-20	RESERVED	R	0h	Reserved
19-10	Operating Current	R	0h	As defined by USB PD.
9-0	Max Min Operation Current	R	0h	As defined by USB PD.

4.19 Autonegotiate Sink Register (Offset = 37h) [Reset = 00000000000000000000000000000000000191904114503Eh]

Autonegotiate Sink is shown in Table 4-21.

Return to the Summary Table.

Configuration for sink power negotiations. This register defines the voltage range between which the system can function properly, allowing the PD Controller to negotiate its own contracts. Initialized by Application Customization.

Table 4-21. Autonegotiate Sink Register Field Descriptions

Bit	Field	Type	Reset	Description
191-181	RESERVED	R/W	0h	Reserved
180-169	AVS Output Voltage	R/W	0h	AVS operating voltage
168-167	RESERVED	R/W	0h	Reserved
166-160	AVS Operating Current	R/W	0h	AVS operating current
159-129	RESERVED	R/W	0h	Reserved
128	EPR AVS Enable Sink Mode	R/W	0h	Enable Sink EPR AVS mode. If this bit is asserted, then the PD controller will attempt to negotiate a EPR AVS sink contract.
127-116	RESERVED	R/W	0h	Reserved
115-105	PPS Output Voltage	R/W	0h	This is the desired output voltage in 20mV units. This is inserted as-is into the Request USB PD message. Note that some PD controllers are unable to turn on the gate-drivers if VBUS less than 3.8V, check the VBUS UVLO value in the data-sheet.
104-103	RESERVED	R/W	0h	Reserved
102-96	PPS Operating Current	R/W	0h	Operation current in Sink PPS mode. This is the desired operating current in 50 mA units. This is inserted as-is into the Request USB PD message.
95-70	RESERVED	R/W	0h	Reserved
69	PPS Disable Sink Upon Non APDO Contract	R/W	0h	Sink path handling during supply type transition. If this bit is asserted and the selected supply type is NOT a PPS APDO, then the sink path is disabled before sending the Request message. The host should only assert this bit after a PPS contract has been negotiated. This bit has no effect unless PPSEnableSinkMode is asserted.
68	PPS Required Full Voltage Range	R/W	0h	Select only a source with full voltage range. If this bit is asserted, a PPS supply type is not selected unless the APDO.MinVoltage ≤ TX_SINK_CAPS.MinPpsVoltage, APDO.MaxVoltage ≥ TX_SINK_CAPS.MaxPpsVoltage, and APDO.MaxCurrent ≥ TX_SINK_CAPS.MaxPpsCurrent. This bit has no effect unless PPSEnableSinkMode is asserted.
67	PPS Source Operating Mode	R/W	0h	Selection for CV or CC mode. If this bit is set to 1, then the PD controller assumes the system is in constant voltage mode and sets the VBUS disconnect threshold accordingly. If this bit is set to 0, then the PD controller will assume the system is in current limit mode and it will lower the VBUS disconnect threshold accordingly.
66-65	PPS Request Interval	R/W	0h	Sink PPS request interval. This field sets the frequency at which the PD controller will send a new request to the source even if the host has not made any change in the request. 0h = 8 seconds 1h = 4 seconds 2h = 2 seconds 3h = 1 second
64	PPS Enable Sink Mode	R/W	0h	Enable Sink PPS mode. If this bit is asserted, then the PD controller will attempt to negotiate a PPS sink contract. PPS contracts are prioritized over any other supply type.
63-62	RESERVED	R/W	0h	Reserved

Table 4-21. Autonegotiate Sink Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
61-52	Auto Neg Capabilities Mismatch Power	R/W	0h	Capabilities Mismatch Power Threshold. If the selected PDO offers less power than what is specified in this register, then the PD controller will assert the Capability Mismatch bit in its Request message unless NoCapabilityMismatch is set to 1. (250mW per LSB)
51-42	Auto Neg Min Voltage	R/W	64h	Minimum voltage to request. During PD power contract negotiation, the PD controller will only select voltages that are greater than or equal to the value specified in this field. Not used unless AutoComputeSinkMinVoltage=0. (50mV per LSB)
41-32	Auto Neg Max Voltage	R/W	190h	Maximum voltage to request. During PD power contract negotiation, the PD controller will only select voltages that are less than or equal to the value specified in this field. Not used unless AutoComputeSinkMinVoltage=0. (50mV per LSB) See description in AutoComputeSinkMinPower.
31-22	Auto Neg Sink Min Required Power	R/W	104h	Minimum operating power required by the Sink. The PD Controller will always attempt to receive this power level from the Source. (250mW per LSB)
21-12	Auto Neg Max Current	R/W	145h	Maximum current to request. The PD controller will not request more current than indicated by this field. The host should ensure that the max current for all PDO's in the TX_SINK_CAPS register do not exceed this value. (10mA per LSB).
11-8	RESERVED	R/W	0h	Reserved
7	RESERVED	R/W	0h	Reserved
6	Auto Disable Sink Upon Capability Mismatch	R/W	0h	Sink path and capability mismatch settings. If this bit is asserted, then any time the implicit or explicit power contract would cause the Capability Mismatch bit to be set the PD controller will disable the sinking path. This bit should only be asserted if the NoCapabilityMismatch bit is set to 0.
5	Auto Compute Sink Max Voltage	R/W	1h	Configuration for maximum voltage. The PD controller can automatically compute ANMaxVoltage, or allow the host to specify it. 0h = Provided by host 1h = Computed by PD controller
4	Auto Compute Sink Min Voltage	R/W	1h	Configuration for minimum voltage. The PD controller can automatically compute ANMinVoltage, or allow the host to specify it. 0h = Provided by host 1h = Computed by PD controller
3	No Capability Mismatch	R/W	1h	Configuration for capability mismatch in RDO. There are two conditions that will trigger a capability mismatch: • If the attached source does not offer a PDO whose power is greater or equal to the ANSinkCapMismatchPower field in this register. • PPS is enabled in this register and the attached source did not offer a PPS PDO that matches the requirements in TX_SINK_CAPS. If either condition is true, then the PD controller will assert the capability mismatch bit in its request unless this bit is asserted. 0h = Capabiltiy mismatch enabled 1h = Capability mismatch disabled.

Table 4-21. Autonegotiate Sink Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	Auto Compute Sink Min Power	R/W	1h	Minimum power sink requires. The minimum sink power is the largest power reported in any valid PDO in the TX_SINK_CAPS (0x33). The power for a particular PDO from the TX_SINK_CAPS follows for each supply type: • Battery Supply: OperatingPower • Variable Supply: MaxVoltage*OperatingCurrent • Fixed Supply: Voltage*OperatingCurrent. However, if the TX_SINK_CAPS register includes Battery supply type PDO(s), then ANSinkMinRequiredPower = maximum OperatingPower in a Battery supply type PDO. 0h = Provided by host 1h = Computed by PD controller
1	No USB Suspend	R/W	1h	Value used for the NoUSBSusp Flag in the RDO. This is as defined by USB PD.
0	Auto Neg RDO Priority	R/W	0h	Configuration for tie-breaker in PDO selection. The PD controller will find the set of PDO's that fulfill the voltage requirements. From that set of PDO's it will pick the one with higher power. If two acceptable PDO's have the same power, Fixed Supply Type is preferred, and then Variable Supply has second preference. If two PDO's have the same power and the same type, then this bit determines which PDO is selected. 0h = Higher voltage 1h = Lower voltage

4.20 Power Status Register (Offset = 3Fh) [Reset = 0000h]

Power Status is shown in Table 4-22.

Return to the Summary Table.

Details about the power of the connection. This register reports status regarding the power of the connection.

Table 4-22. Power Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0h	Reserved
9-8	Charger Advertise Status	R	0h	Charger Advertise Status 0h = Charger advertise disabled or not run 1h = Charger advertisement in process 2h = Charger advertisement complete 3h = Reserved
7-4	Charger Detect Status	R	0h	0h = Charger detection disabled or not run 1h = Charger detection in progress 2h = Charger detection complete none detected 3h = Charger detection complete SDP detected 4h = Charger detection complete BC 1.2 CDP detected 5h = Charger detection complete BC 1.2 DCP detected 6h = Charger detection complete Divider1 DCP detected 7h = Charger detection complete Divider2 DCP detected 8h = Charger detection complete Divider3 DCP detected 9h = Charger detection complete 1.2V DCP detected
3-2	TypeC Current	R	0h	This field is redundant with PD_STATUS.CCPullUp in register 0x40 when SourceSink is 1b. This field is redundant with PORT_CONTROL.TypeCCurrent in register 0x29 when SourceSink is 0b. This field is intended for Type-C Sink operation. If the port is connected as source, the field is updated upon initial connection only. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Explicit PD contract sets current
1	SourceSink	R	0h	Source / Sink indicator. This bit is equivalent to PresentPDRole in register 0x40. It is replicated in this register for convenience. 0h = Connection requests power 1h = Connection provides power (PD Controller as sink)
0	Power Connection	R	0h	Asserted if there is a connection. This bit is asserted when PlugPresent is TRUE and ConnState is greater than 5h. So it is redundant with information from register 0x1A. It is replicated in this register for convenience. 0h = No connection 1h = Connection present

4.21 PD Status Register (Offset = 40h) [Reset = 00000000h]

PD Status is shown in Table 4-23.

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Status of PD and Type-C state-machine. This register contains details regarding the status of PD messages and the Type-C state machine.

Table 4-23. PD Status Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	RESERVED	R	0h	Reserved
27-22	RESERVED	R	0h	Reserved
21-16	Hard Reset Details	R	0h	Reason for Hard Reset 0h = Reset value no hard reset 1h = Received from Port Partner 2h = Requested by host 3h = Invalid DR_Swap request during Active Mode 4h = DischargeFailed. 5h = NoResponseTimeOut. 6h = SendSoftReset. 7h = Sink_SelectCapability. 8h = Sink_TransitionSink. 9h = Sink_WaitForCapabilities. Ah = SoftReset. Bh = SourceOnTimeout. Ch = Source_CapabilityResponse. Dh = Source_SendCapabilities. Eh = SourcingFault. Fh = UnableToSource. 10h = FRS failure 11h = Unexpected message 12h = Failure to to complete the VCONN recovery sequence within 200ms after PP5V rising edge
15-13	RESERVED	R	0h	Reserved
12-8	Soft Reset Details	R	0h	Reason for Soft Reset 0h = Reset value no soft reset 1h = Soft reset received from Port Partner 2h = Reserved 3h = Reserved 4h = Received source capabilities message was invalid 5h = Message retries were exhausted 6h = Received an accept message unexpectedly 7h = Received a control message unexpectedly 8h = Received a GetSinkCap message unexpectedly 9h = Received a GetSourceCap message unexpectedly Ah = Received a GotoMin message unexpectedly Bh = Received a PS_RDY message unexpectedly Ch = Received a Ping message unexpectedly Dh = Received a Reject message unexpectedly Eh = Received a Request message unexpectedly Fh = Received a Sink Capabilities message unexpectedly 10h = Received Source Capabilities message unexpected 11h = Received a Swap message unexpectedly 12h = Received a Wait Capabilities message unexpectedly 13h = Received an unknown control message 14h = Received an unknown data message 15h = To initialize SOP' controller in plug 16h = To initialize SOP'' controller in plug 17h = Received an Extended message unexpectedly 18h = Received an unknown Extended message 19h = Received a data message unexpectedly 1Ah = Received a Not Supported message unexpectedly 1Bh = Received a Get_Status message unexpectedly

Table 4-23. PD Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	Present PD Role	R	0h	Present PD power role. The PD Controller is acting under this PD power role. 0h = Sink 1h = Source
5-4	Port Type	R	0h	Present Type-C power role. The PD Controller is acting under this Type-C power role. 0h = Sink/Source 1h = Sink 2h = Source 3h = Source/Sink
3-2	CC Pullup	R	0h	CC Pull-up value. The pull-up value detected by PD Controller when in CC Pull-down mode. 0h = Not in CC pull-down mode / no CC pull-up detected 1h = USB Default current 2h = 1.5 A (SinkTxNG) 3h = 3.0 A (SinkTxOK)
1-0	RESERVED	R	0h	Reserved

4.22 PD3 Configuration Register (Offset = 42h) [Reset = 0008801Ah]

PD3 Configuration is shown in Table 4-24.

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PD3.0 configuration settings.

Table 4-24. PD3 Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	0h	Reserved
24	RESERVED	R/W	0h	Reserved
23-22	RESERVED	R/W	0h	Reserved
21	RESERVED	R/W	0h	Reserved
20	Support PPS Status	R/W	0h	Supports PPS Status Message. If this bit is asserted the PD controller will respond to a Get_PPS_Status message with the contents of the TX_PPS_SDB register (0x7A).
19	Support Get Revision	R/W	1h	Supports Revision Message. If this bit is asserted the PD controller will respond to a Get_Revision USB PD message with the supported PD Spec Version.
18	Support Get Source Info	R/W	0h	Support Source Info Message. If this bit is asserted the PD controller will respond to a Get_Source_Info USB PD message with the contents of TX_Source_Info register (0x78).
17	Support Sink Cap Extended	R/W	0h	Support Sink Capabilities Extended message. If this bit is asserted the PD controller will respond to a Get_Sink_Capabilities_Extended message USB PD message with the contents of the TX_SKEDB register (0x7E).
16	RESERVED	R/W	0h	Reserved
15	RESERVED	R/W	0h	Reserved
14	RESERVED	R/W	0h	Reserved
13	RESERVED	R/W	0h	Reserved
12	RESERVED	R/W	0h	Reserved
11	Support Battery Status Message	R/W	0h	Support Battery Status message. If this bit is asserted the PD controller will respond to a Get_Battery_Status USB PD message with the contents of the TX_BSDO register (0x7B).
10	Support Battery Capabilities Message	R/W	0h	Support Battery Capability message. If this bit is asserted the PD controller will respond to a Get_Battery_Capabilities USB PD message with the contents of the TX_BCDB register (0x7D).
9	RESERVED	R/W	0h	Reserved
8	Support Source Extended Message	R/W	0h	Enable Source Capabilities Extended. If this bit is asserted the PD controller will respond to a Get_Source_Capabilities_Extended USB PD message with the contents of the TX_SCEDB register (0x77).
7-5	RESERVED	R/W	0h	Reserved
4	Unchunked Supported	R/W	1h	Enable unchunked support. If this bit is asserted the PD controller will support unchunked messaging (up to 260 bytes). The host is responsible to consume the unchunked message before the PD controller will be able to receive another long unchunked message.
3-2	RESERVED	R/W	0h	Reserved
1-0	RESERVED	R/W	0h	Reserved

4.23 Received SOP Identity Data Object Register (Offset = 48h) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Received SOP Identity Data Object is shown in Table 4-25.

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Received Discover Identity ACK (SOP). Latest Discover Identity response received over USB PD using SOP.

Table 4-25. Received SOP Identity Data Object Register Field Descriptions

Bit	Field	Type	Reset	Description
199-168	RX ID SOP VDO 6	R	0h	6th VDO. The sixth Data Object for Discover Identity response is context-specific.
167-136	RX ID SOP VDO 5	R	0h	5th VDO. The fifth Data Object for Discover Identity response is context-specific.
135-104	RX ID SOP VDO 4	R	0h	4th VDO. The fourth Data Object for Discover Identity response is context-specific as defined in USB PD.
103-72	RX ID SOP VDO 3	R	0h	Product VDO. The third Data Object for Discover Identity response.
71-40	RX ID SOP VDO 2	R	0h	Cert Stat VDO. The second Data Object for Discover Identity response.
39-8	RX ID SOP VDO 1	R	0h	ID Header VDO. The first Data Object in Discover Identity response.
7-6	Response Type	R	0h	Type of response received. 0h = SOP Discover Identity REQ not sent or pending 1h = Responder ACK received 2h = Responder NAK received or response timeout 3h = Responder BUSY received
5-3	RESERVED	R	0h	Reserved
2-0	Number Valid VDOs	R	0h	Number of valid VDO's in this register. (Max of 6)

4.24 IO Config Register (Offset = 5Ch) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000CCFh]

IO Config is shown in Table 4-26.

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Application-specific GPIO Configurations. This register cannot be modified at run-time, the GPIO configurations are set according to the configuration during the boot process.

Table 4-26. IO Config Register Field Descriptions

Bit	Field	Type	Reset	Description
391-384	GPIO 12 Mapped Event	R	0h	Event table mapping for GPIO12. See GPIO Event table.
383-376	GPIO 11 Mapped Event	R	0h	Event table mapping for GPIO11. See GPIO Event table.
375-368	GPIO 10 Mapped Event	R	0h	Event table mapping for GPIO10. See GPIO Event table.
367-352	RESERVED	R	0h	Reserved
351-344	GPIO 7 Mapped Event	R	0h	Event table mapping for GPIO7. See GPIO Event table.
343-336	GPIO 6 Mapped Event	R	0h	Event table mapping for GPIO6. See GPIO Event table.
335-328	GPIO 5 Mapped Event	R	0h	Event table mapping for GPIO5. See GPIO Event table.
327-320	GPIO 4 Mapped Event	R	0h	Event table mapping for GPIO4. See GPIO Event table.
319-312	GPIO 3 Mapped Event	R	0h	Event table mapping for GPIO3. See GPIO Event table.
311-304	GPIO 2 Mapped Event	R	0h	Event table mapping for GPIO2. See GPIO Event table.
303-296	GPIO 1 Mapped Event	R	0h	Event table mapping for GPIO1. See GPIO Event table.
295-288	GPIO 0 Mapped Event	R	0h	Event table mapping for GPIO0. See GPIO Event table.
287-269	RESERVED	R	0h	Reserved
268-256	GPIO Event Polarity	R	0h	Controls polarity of a selected output event for each GPIO. Assert the bit for a given GPIO to invert the polarity of the event mapped to it. This field has no impact for input GPIO Events.
255-230	RESERVED	R	0h	Reserved
229	GPIO 5 Analog Input Control	R	0h	Assert when GPIO5 is used as an analog input. This must also be asserted when PORT_CONTROL.ChargerDetectEnable or ChargerAdvertiseEnable is non-zero.
228	GPIO 4 Analog Input Control	R	0h	Assert when GPIO4 is used as an analog input. This must also be asserted when PORT_CONTROL.ChargerDetectEnable or ChargerAdvertiseEnable is non-zero.
227	RESERVED	R	0h	Reserved
226	GPIO AI Enable GPIO 2	R	0h	Assert when GPIO4 is used as an analog input.
225	RESERVED	R	0h	Reserved
224	GPIO AI Enable GPIO 0	R	0h	Assert when GPIO4 is used as an analog input.
223-205	RESERVED	R	0h	Reserved
204-192	Internal Pull Up Enable	R	0h	Controls weak pull-up setting for each configurable GPIO (1=Enabled, 0=Disabled).
191-173	RESERVED	R	0h	Reserved
172-160	Internal Pull Down Enable	R	0h	Controls weak pull-down setting for each configurable GPIO (1=Enabled, 0=Disabled).
159-140	RESERVED	R	0h	Reserved
139-128	RESERVED	R	0h	Reserved
127-109	RESERVED	R	0h	Reserved
108-96	Open Drain Output Enable	R	0h	Controls push-pull (0) vs. open-drain (1) setting for each configurable GPIO.
95-77	RESERVED	R	0h	Reserved

Table 4-26. IO Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
76-64	Initial Value	R	0h	Controls default output level for each GPIO enabled as output (0=Drive Low, 1=Drive High)
63-45	RESERVED	R	0h	Reserved
44-32	GPIO Interrupt Enable	R	0h	Controls interrupt enable for each GPIO (1=Interrupt Enabled, 0=Interrupt Disabled). Note that all GPIO pins may not be configured as inputs (see the data-sheet).
31-13	RESERVED	R	0h	Reserved
12-0	GPIO Output Enable	R	CCFh	Controls output enable for each GPIO (1=Output Enabled, 0=Hi-Z). Note that all GPIO may not be configurable as an output (see data-sheet).

4.25 Type C State Register (Offset = 69h) [Reset = 00000000h]

Type C State is shown in Table 4-27.

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Contains current status of both CCn pins.

Table 4-27. Type C State Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TypeC Port State	R	0h	Present state of Type-C state-machine. 0h = Disabled 5h = ErrorRecovery 24h = Unattached.Accessory 2Bh = AttachWait.Accessory 45h = Try.SRC 4Eh = TryWait.SNK 4Fh = Try.SNK 50h = TryWait.SRC 60h = Attached.SRC 61h = Attached.SNK 62h = AudioAccessory 63h = DebugAccessory 64h = AttachWait.SRC 65h = AttachWait.SNK 66h = Unattached.SNK 67h = Unattached.SRC
23-16	CC2 Pin State	R	0h	State of CC2 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (SInk only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
15-8	CC1 Pin State	R	0h	State of CC1 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (SInk only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
7-0	CC Pin for PD	R	0h	CC pin used for PD communication. 0h = Not connected 1h = CC1 is used for USB PD communication 2h = CC2 is used for USB PD communication

4.26 ADC Results Register (Offset = 6Ah) [Reset = 00000000000000000000000000h]

ADC Results is shown in Table 4-28.

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Provides access to measurements from the internal ADC. The PD controller periodically measures the pins mentioned in this register and updates the register accordingly. The frequency of the update depends upon the mode of the PD controller. For example, in Unconnected Sleep the PD controller will not update these registers. This register should only be used for debug purposes and not for end solutions.

Table 4-28. ADC Results Register Field Descriptions

Bit	Field	Type	Reset	Description
103-96	RESERVED	R	0h	Reserved
95-88	IVBUS_Peak	R	0h	Most recent current peak estimate through PP5V. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent peak current. It is cleared upon attach for a new connection.(16.5mA per LSB)
87-80	GPIO2	R	0h	Most recent voltage on the GPIO2 pin. (14mV per LSB)
79-72	GPIO0	R	0h	Most recent voltage on the GPIO0 pin. (14mV per LSB)
71-64	GPIO5	R	0h	Most recent voltage on the GPIO5 pin. (14mV per LSB)
63-56	GPIO4	R	0h	Most recent voltage on the GPIO4 pin. (14mV per LSB)
55-48	RESERVED	R	0h	Reserved
47-40	IVBUS_Mean	R	0h	Most recent current mean estimate through PP5V. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent mean current. It is cleared upon attach for a new connection.(16.5mA per LSB)
39-32	RESERVED	R	0h	Reserved
31-24	VBUS	R	0h	Most recent voltage on the VBUS pin. (98mV per LSB)
23-16	LDO3V3	R	0h	Most recent voltage on the LDO_3V3 pin. (14mV per LSB)
15-8	ADCIN2	R	0h	Most recent voltage on the ADCIN2 pin. (14mV per LSB)
7-0	ADCIN1	R	0h	Most recent voltage on the ADCIN1 pin. (14mV per LSB)

4.27 Sleep Control Register (Offset = 70h) [Reset = 03h]

Sleep Control Register is shown in Table 4-29.

Return to the Summary Table.

Sleep configurations.

Table 4-29. Sleep Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-1	Sleep Time	R/W	1h	Minimum time the PD controller waits before entering sleep mode. 0h = Reserved 1h = 100 ms 2h = 1000 ms 3h = Reserved
0	Sleep Mode Allowed	R/W	1h	If this bit is asserted the PD controller will enter sleep modes after device is idle for Sleep Time.

4.28 GPIO Status Register (Offset = 72h) [Reset = 0000000000000000h]

GPIO Status is shown in Table 4-30.

Return to the Summary Table.

Captures status and settings of all GPIO pins. Check the device-specific datasheet for the available GPIO because it may vary by device type.

Table 4-30. GPIO Status Register Field Descriptions

Bit	Field	Type	Reset	Description
63-40	RESERVED	R	0h	Reserved
39	GPIO 7 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
38	GPIO 6 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
37	GPIO 5 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
36	GPIO 4 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
35	GPIO 3 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
34	GPIO 2 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
33	GPIO 1 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
32	GPIO 0 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
31-13	RESERVED	R	0h	Reserved
12	GPIO 12 Data	R	0h	Asserted if a logic high is detected on the GPIO.
11	GPIO 11 Data	R	0h	Asserted if a logic high is detected on the GPIO.
10	GPIO 10 Data	R	0h	Asserted if a logic high is detected on the GPIO.
9-8	RESERVED	R	0h	Reserved
7	GPIO 7 Data	R	0h	Asserted if a logic high is detected on the GPIO.
6	GPIO 6 Data	R	0h	Asserted if a logic high is detected on the GPIO.
5	GPIO 5 Data	R	0h	Asserted if a logic high is detected on the GPIO.
4	GPIO 4 Data	R	0h	Asserted if a logic high is detected on the GPIO.
3	GPIO 3 Data	R	0h	Asserted if a logic high is detected on the GPIO.
2	GPIO 2 Data	R	0h	Asserted if a logic high is detected on the GPIO.
1	GPIO 1 Data	R	0h	Asserted if a logic high is detected on the GPIO.
0	GPIO 0 Data	R	0h	Asserted if a logic high is detected on the GPIO.

4.29 Tx Source Capabilities Extended Data Block Register (Offset = 77h) [Reset = 00000000000000000000000000000000h]

Tx Source Capabilities Extended Data Block is shown in Table 4-31.

Return to the Summary Table.

Transmit Source Capabilities Extended Data Block (SCEDB). If the PD3 configuration register (0x42) bit SourceCapExtMsg is set to zero, the PD controller responds to a Get_Source_Cap_Extended USB PD message with a Not_Supported message. If the SourceCapExtMsg bit is set to 1 then the response is generated from the contents of this register based on USB PD requirements. The VID, PID, and XID fields are taken from the PD internal firmware configurable through the Application Customization Tool, the FW version is taken from the PD internal firmware, the HW version is taken from the REV_ID word in the Boot Flags register (0x2D), then the contents of this register are appended.

Table 4-31. Tx Source Capabilities Extended Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
119-112	Source EPR PDP	R/W	0h	Source's EPR PDP rating as defined by the USB PD specification.
111	RESERVED	R/W	0h	Reserved
110-104	Source PDP	R/W	0h	Source's PDP rating as defined by the USB PD specification.
103-100	Number Hot Swappable Batteries	R/W	0h	Number of hot swappable batteries / battery slots as defined by the USB PD specification. (Max of 1)
99-96	Number Fixed Batteries	R/W	0h	Number of fixed batteries / battery slots as defined by the USB PD specification. (Max of 3)
95-88	Source Inputs	R/W	0h	Source inputs as defined by the USB PD specification. The Barrel_Jack_Event GPIO Event can modify bit 0 of this field automatically upon rising and falling edges. The host may choose to set bit 1 of this field to 1 when it enables the Barrel_Jack_Event GPIO Event.
87-80	Touch Temperature	R/W	0h	Touch temperature as defined by the USB PD specification.
79-64	Peak Current 3	R/W	0h	Peak Current 3 as defined by the USB PD specification.
63-48	Peak Current 2	R/W	0h	Peak Current 2 as defined by the USB PD specification.
47-32	Peak Current 1	R/W	0h	Peak Current 1 as defined by the USB PD specification.
31-24	Touch Current	R/W	0h	Touch current as defined by the USB PD specification.
23-16	Compliance	R/W	0h	Compliance as defined by the USB PD specification.
15-8	Hold Up Time	R/W	0h	Hold up time as defined by the USB PD specification.
7-0	Voltage Regulation	R/W	0h	Voltage regulation as defined by the USB PD specification.

4.30 TX Source Info Register (Offset = 78h) [Reset = 00000000h]

TX Source Info is shown in Table 4-32.

Return to the Summary Table.

Transmit Source info. If the PD3 configuration register (0x42) bit SupportGetSourceInfo is set to 0 and a Get_Source_Info message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportGetSourceInfo bit is set to 1 and a Get_Source_Info message is received then the contents of this register are sent in response. This register is automatically updated by the PD firmware and does not require any EC implementation.

Table 4-32. TX Source Info Register Field Descriptions

Bit	Field	Type	Reset	Description
31	Port Type Shared Assured	R	0h	Shared/Assured Capacity Port: Shared = 0, Assured = 1
30-24	RESERVED	R	0h	Reserved
23-16	Port Maximum PDP	R	0h	Power the port is designed to supply. (250mW per LSB)
15-8	Port Present PDP	R	0h	Power the port is presently capable of supplying. (250mW per LSB)
7-0	Port Reported PDP	R	0h	Power the port is actually advertising. (250mW per LSB)

4.31 Trasmitted PPS Status Data Block Register (Offset = 7Ah) [Reset = 00000000h]

Trasmitted PPS Status Data Block is shown in Table 4-33.

Return to the Summary Table.

Transmit PPS Status Data Block (BSDO). If the PD3 configuration register (0x42) bit SupportPPSStatus is set to zero and a Get_PPS_Status message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportPPSStatus bit is set to 1 and a Get_PPS_Status message is received then the contents of this register are sent in response.

Table 4-33. Trasmitted PPS Status Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	Reserved
27	OMF	R/W	0h	Real Time Flag as defined by the USB PD spec.
26-25	PTF	R/W	0h	Real Time Flag as defined by the USB PD spec.
24	RESERVED	R/W	0h	Reserved
23-16	Output Current	R/W	0h	Output current as defined by the USB PD spec. (50mA per LSB). 0xFF = this field not supported
15-0	Output Voltage	R/W	0h	Output voltage as defined by the USB PD spec.(20mV per LSB, 0xFFFF = this field not supported)

4.32 Transmitted Battery Status Data Objects (BSDO) Register (Offset = 7Bh) [Reset = 00000000000000000000000FFFF0200h]

Transmitted Battery Status Data Objects (BSDO) Register is shown in Table 4-34.

Return to the Summary Table.

Transmit Battery Status Data Objects (BSDO). The host should also program the Tx Source Capabilities Extended register (0x77) in order to specify the number of each type of battery such that it is consistent with the contents of this register. This feature must be enabled in the PD3_CONFIG register (0x42) SupportBatteryStatusMsg bit. The PD controller does not take any automatic action if this register is written. If the SupportBatteryStatusMsg bit is set to 0 and a Get_Battery_Status message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportBatteryStatusMsg bit is set to 1, and a Get_Battery_Status message is received then the contents of this register are sent in response.

Table 4-34. Transmitted Battery Status Data Objects (BSDO) Register Field Descriptions

Bit	Field	Type	Reset	Description
127-112	Hot Swappable Battery 0 Present Info	R/W	0h	Battery status data object returned for fixed battery index 0.
111-104	Hot Swappable Battery 0 Battery Info	R/W	0h	Battery status data object returned for hot-swappable battery index 0.
103-96	RESERVED	R/W	0h	Reserved
95-80	Fixed Battery 2 Present Capacity	R/W	0h	Battery status data object returned for fixed battery index 0.
79-72	Fixed Battery 2 Battery Info	R/W	0h	Battery status data object returned for fixed battery index 2.
71-64	RESERVED	R/W	0h	Reserved
63-48	Fixed Battery 1 Present Capacity	R/W	0h	Battery status data object returned for fixed battery index 0.
47-40	Fixed Battery 1 Battery Info	R/W	0h	Battery status data object returned for fixed battery index 1.
39-32	RESERVED	R/W	0h	Reserved
31-16	Fixed Battery 0 Present Capacity	R/W	FFFFh	Battery status data object returned for fixed battery index 0.
15-8	Fixed Battery 0 Battery Info	R/W	2h	Battery status data object returned for fixed battery index 0.
7-0	RESERVED	R/W	0h	Reserved

4.33 Tx Battery Capabilities Register (Offset = 7Dh) [Reset = 0000000000000000000000000000000000000000000000000000000000000000h]

Tx Battery Capabilities is shown in Table 4-35.

Return to the Summary Table.

Transmit Battery Capability Data Block (BCDB). The host should also program the Tx Source Capabilities Extended register (0x77) in order to specify the number of each type of battery such that it is consistent with the contents of this register. This feature must be enabled in the PD3_CONFIG register (0x42) bit SupportBatteryCapMsg. The PD controller does not take any automatic action if this register is written. If the SupportBatteryCapMsg is 0 and a Get_Battery_Capabilities message is received, then the contents of this register are ignored and the PD controller sends a Not_Supported message. If the SupportBatteryCapMsg is 1 and a Get_Battery_Capabilities message is received, then the contents of this register are sent in response.

Table 4-35. Tx Battery Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
287-280	Battery Type	R/W	0h	Battery type for hot-swappable battery index 0.
279-264	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for hot-swappable battery index 0.
263-248	Battery Design Capacity	R/W	0h	Battery design capacity for hot-swappable battery index 0.
247-232	PID 3	R/W	0h	PID for hot-swappable battery index 0.
231-216	VID 3	R/W	0h	VID for hot-swappable battery index 0.
215-208	Battery Type	R/W	0h	Battery type for fixed battery index 2.
207-192	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for fixed battery index 2.
191-176	Battery Design Capacity	R/W	0h	Battery design capacity for fixed battery index 2.
175-160	PID 2	R/W	0h	PID for fixed battery index 2.
159-144	VID 2	R/W	0h	VID for fixed battery index 2.
143-136	Battery Type	R/W	0h	Battery type for fixed battery index 1.
135-120	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for fixed battery index 1.
119-104	Battery Design Capacity	R/W	0h	Battery design capacity for fixed battery index 1.
103-88	PID 1	R/W	0h	PID for fixed battery index 1.
87-72	VID 1	R/W	0h	VID for fixed battery index 1.
71-64	Battery Type	R/W	0h	Battery type for fixed battery index 0.
63-48	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for fixed battery index 0.
47-32	Battery Design Capacity	R/W	0h	Battery design capacity for fixed battery index 0.
31-16	PID 0	R/W	0h	PID for fixed battery index 0.
15-0	VID 0	R/W	0h	VID for fixed battery index 0.

4.34 Transmit Sink Capabilities Extended Data Block Register (Offset = 7Eh) [Reset = 00000000000000000000000000000000h]

Transmit Sink Capabilities Extended Data Block is shown in Table 4-36.

Return to the Summary Table.

Transmit Sink Capabilities Data Block (SKEDB). This feature must be enabled in the PD3_CONFIG register (0x42) bit SupportSinkCapExtended. The PD controller does not take any automatic action if this register is written. If the SupportSinkCapExtended bit is 0 and a Get_Sink_Cap_Extended message is received, then the contents of this register are ignored and the PD controller sends a Not_Supported message. If the SupportSinkCapExtended bit is 1 and a Get_Sink_Cap_Extended message is received, then the contents of this register are used to formulate the response. The VID, PID, and XID fields are taken from the PD internal firmware configurable through the Application Customization Tool, the FW version is taken from the PD internal firmware, the HW version is taken from the REV_ID word in the Boot Flags register (0x2D). Finally, the PD controller appends the contents of this register. Refer to the latest USB PD specification for detailed description of each field. The values in this register are not used by the PD controller to affect behavior, it just simply uses these contents to respond.

Table 4-36. Transmit Sink Capabilities Extended Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
111-104	EPR Sink Maximum PDP	R/W	0h	EPR Sink maximum PDP as defined in the USB PD specification.
103-96	EPR Sink Operational PDP	R/W	0h	EPR Sink operational PDP as defined in the USB PD specification.
95-88	EPR Sink Minimum PDP	R/W	0h	EPR Sink minimum PDP as defined in the USB PD specification.
87-80	Sink Maximum PDP	R/W	0h	Sink maximum PDP as defined in the USB PD specification.
79-72	Sink Operational PDP	R/W	0h	Sink operational PDP as defined in the USB PD specification.
71-64	Sink Minimum PDP	R/W	0h	Sink minimum PDP as defined in the USB PD specification.
63-56	Sink Modes	R/W	0h	Sink modes as defined in the USB PD specification.
55-48	Battery Info	R/W	0h	Battery information as defined in the USB PD specification.
47-40	Touch Temprature	R/W	0h	Touch temperature as defined by the USB PD specification.
39-32	Compliance	R/W	0h	Compliance as defined by the USB PD specification.
31-16	Sink Load Char	R/W	0h	Sink load characteristics as defined in the USB PD specification.
15-8	Load Step	R/W	0h	Load step as defined in the USB PD specification.
7-0	SKEDB Version	R/W	0h	SKEDB Version as defined in the USB PD specification.

4.35 Liquid Detection Config Register (Offset = 98h) [Reset = 00000000000000000000h]

Liquid Detection Config is shown in Table 4-37.

Return to the Summary Table.

Liquid Detection Configuration

Table 4-37. Liquid Detection Config Register Field Descriptions

Bit	Field	Type	Reset	Description
82	Enable Liquid Detection	R/W	0h	Enables liquid detection on the SBU pins connected to the GPIO on the PD Controller. In order for this to function correctly the proper external liquid detection circuitry must be in place.
81	Enable Corrosion Mitigation	R/W	0h	Enable corrosion mitigation. Corrosion mitigation will disconnect the port, disabled the port, and pull down CC pins.
80	Liquid Detection State	R/W	0h	Liquid Detection State
79-76	Sample Time in 10ms Liquid	R/W	0h	Sample Time in multiples of 10ms (10ms per LSB as ms)
75-72	Sample Time in 10ms No Liquid	R/W	0h	Sample Time in multiples of 10ms (10ms per LSB as ms)
71-64	High Threshold ADC Liquid	R/W	0h	High Threshold ADC Liquid (14mV per LSB as mV)
63-56	Low Threshold ADC Liquid	R/W	0h	Low Threshold ADC Liquid (14mV per LSB as mV)
55-48	High Threshold ADC No Liquid	R/W	0h	High Threshold ADC No Liquid, provides hysteresis for exit out of Liquid Detected. (14mV per LSB as mV)
47-40	Low Threshold ADC No Liquid	R/W	0h	Low Threshold ADC No Liquid, provides hysteresis for exit out of Liquid Detected. (14mV per LSB as mV)
39-32	Number of Samples	R/W	0h	Number of samples (must be 2^N) to take average
31-16	Sleep Time In Sec Liquid	R/W	0h	Sleep in multiples of 1s when liquid is detected (1000ms per LSB as ms)
15-0	Sleep Time In Sec No Liquid	R/W	0h	Sleep in multiples of 1s when liquid is not detected. (1000ms per LSB as ms)

Chapter 5

4CC Task Detailed Descriptions

5.1 Overview

This section describes the 4CC Tasks defined by the PD Controller Host Interface. The Tasks are categorized into various sub-groups in this section. All Tasks that return data using the DATAx registers will always ensure the proper output data is loaded into those registers before setting the CMDx register to 0 to indicate Task completion. DATAx is never modified by PD Controller after CMDx has been changed to 0, to ensure the Host can retrieve data from the previously-executed Task, and to ensure the Host can load these registers for a future Task without risk of overwriting. Note that other registers can continue to be updated after a Task completes, as Tasks can have additional side effects.

Many of the Tasks return a status code in the first byte of the DATAx register. The standard Task response byte is defined in Table 5-1. The remaining DATAx bytes can be used at each Task's discretion.

Table 5-1. Standard Task Response

Description	**Tasks are a special form of Tasks that return a status code in the first byte of the DATAX register.**			
Output DATAX	**Bit**	**Name**	**Description**	
	Byte 1: Task Return Code			
	7:4	Reserved	Reserved for standard Tasks. May be used by certain Tasks for Task-specific return codes. Successful return codes can use this byte provided TaskResult is 0x0.	
	3:0	TaskResult	Standard Task return codes.	
			0x0	Task completed successfully.
			0x1	Task timed-out.
			0x2	Reserved.
			0x3	Task rejected.
			0x4	Task rejected because the Rx Buffer was locked. This is for Tasks that can require the PD controller to use the Rx Buffer.
			0x5-0xF	Reserved for standard Tasks. May be used by certain Tasks for Task-specific error codes. Treated as an error when encountered.

5.2 CPU Control Tasks

5.2.1 'Gaid' - Return to normal operation

Table 5-2. 'Gaid' - Return to normal operation.

Description	The 'Gaid' Task causes a warm restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default AppConfig state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller is in the 'APP ' mode, then it immediately goes to the Error Recovery state then after delaying 1 second (typical) it does a warm restart. The register settings revert back to the original AppConfig configuration set by the user in the Application Customization Tool.

5.2.2 'GAID' - Cold reset request

Table 5-3. 'GAID' - Cold reset request

Description	The 'GAID Task causes a cold restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete. This Task forces the PD Controller to reboot its OTP bootloader.
Side Effects	The 'Gaid' Task causes a cold restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller immediately goes to the Error Recovery state, then after delaying 1 second (typical) it does a cold restart. The register settings revert back to the default state of the PD before entering 'APP' mode.

5.3 PD Message Tasks

5.3.1 'SWSk' - PD PR_Swap to Sink

Table 5-4. 'SWSk' - PD PR_Swap to Sink

Description	The 'SWSk' Task instructs PD Controller to attempt to become a Sink through PR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'SWSk' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Source. The 'SWSk' Task shall be considered rejected if: • The Source indicated through Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSk' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSk' Task shall be considered successful if: • PD Controller is already in the Sink power role. • The PR_Swap is Accepted and completes normally.
Side Effects	When the 'SWSk' Task completes successfully PD Controller will have transitioned to the Sink power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

5.3.2 'SWSr' - PD PR_Swap to Source

Table 5-5. 'SWSr' - PD PR_Swap to Source

Description	The 'SWSr' Task instructs PD Controller to attempt to become a Source through PR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'SWSr' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Sink. The 'SWSr' Task shall be considered rejected if: • The Sink previously indicated through Sink or Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSr' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSr' Task shall be considered successful if: • PD Controller is already in the Source power role. • The PR_Swap is Accepted and completes normally.
Side Effects	When the 'SWSr' Task completes successfully PD Controller will have transitioned to the Source power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

5.3.3 'SWDF' - PD DR_Swap to DFP

Table 5-6. 'SWDF' - PD DR_Swap to DFP

Description	**The 'SWDF' Task instructs PD Controller to attempt to become a DFPthrough DR_Swap at the first opportunity while maintaining policy enginecompliance. If there are any active Alternate Modes as a UFP PD Controller willattempt to exit those Modes first before sending the DR_Swap.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'SWDF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the DFP. The 'SWDF' Task shall be considered rejected if: • The UFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWDF' Task shall be considered successful if: • PD Controller is already in the DFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

5.3.4 'SWUF' - PD DR_Swap to UFP

Table 5-7. 'SWUF' - PD DR_Swap to UFP

Description	**The 'SWUF' Task instructs PD Controller to attempt to become a UFPthrough DR_Swap at the first opportunity while maintaining policy enginecompliance. If there are any active Alternate Modes as a DFP PD Controller willexit those Modes first before attempting the DR_Swap.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'SWUF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the UFP. The 'SWUF' Task shall be considered rejected if: • The DFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWUF' Task shall be considered successful if: • PD Controller is already in the UFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

5.3.5 'GSkC' - PD Get Sink Capabilities

Table 5-8. 'GSkC' - PD Get Sink Capabilities

Description	**The 'GSkC' Task instructs PD Controller to issue a Get_Sink_Cap message to the Port Partner at the first opportunity while maintaining policy engine compliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'GSkC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails. • The Port Partner is a Source and indicated it was not Dual-Role Power. • The Port Partner responds to the Get_Sink_Cap message with a Reject or Not_Supported message. The 'GSkC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSkC' Task shall be considered successful if: • The Get_Sink_Cap message is sent, GoodCRC'ed and a Sink Capabilities message is received and processed.
Side Effects	When the 'GSkC' Task completes successfully the *RX_SINK_CAPS* register (0x31) will have been updated.
Additional Information	None

5.3.6 'GSrC' - PD Get Source Capabilities

Table 5-9. 'GSrC' - PD Get Source Capabilities

Description	**The 'GSrC' Task instructs PD Controller to issue a Get_Source_Cap message to the Port Partner device at the first opportunity while maintaining policy engine compliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'GSrC' Task completes either when the Source Capabilities message is received or the Task otherwise fails. The 'GSrC' Task shall be considered rejected if: • The Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The Port Partner responds to the Get_Source_Cap message with a Reject or Not_Supported message. The 'GSrC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSrC' Task shall be considered successful if: • The Get_Source_Cap message is sent, GoodCRC'ed and a Source Capabilities message is received and processed.
Side Effects	When the 'GSrC' Task completes successfully the *RX_SOURCE_CAPS* register (0x30) will have been updated.
Additional Information	None

5.3.7 'ESkC' - PD EPR Get Sink Capabilities

Table 5-10. 'ESkC' - PD EPR Get Sink Capabilities

Description	**The 'ESkC' Task instructs PD Controller to issue a EPR_Get_Sink_Cap message to the Port Partner at the first opportunity while maintaining policy engine compliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'ESkC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails. • The Port Partner is a Source and indicated it was not Dual-Role Power. • The Port Partner responds to the EPR_Get_Sink_Cap message with a Reject or Not_Supported message. The 'ESkC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'ESkC' Task shall be considered successful if: • The EPR_Get_Sink_Cap message is sent, GoodCRC'ed and a EPR_Sink_Capabilities message is received and processed.
Side Effects	When the 'ESkC' Task completes successfully the *RX_SINK_CAPS* register (0x31) will have been updated.
Additional Information	The 'ESnK' Task can only be sent if the PD is capable of operating as a Source or DRP and supports EPR mode.

5.3.8 'ESrC' - PD EPR Get Source Capabilities

Table 5-11. 'ESrC' - PD EPR Get Source Capabilities

Description	**The 'ESrC' Task instructs PD Controller to issue a EPR_Get_Source_Cap message to the Port Partner device at the first opportunity while maintaining policy engine compliance.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'ESrC' Task completes either when the EPR Source Capabilities message is received or the Task otherwise fails. The 'ESrC' Task shall be considered rejected if: • The Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The Port Partner responds to the EPR_Get_Source_Cap message with a Reject or Not_Supported message. The 'ESrC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'ESrC' Task shall be considered successful if: • The EPR_Get_Source_Cap message is sent, GoodCRC'ed and a EPR_Source_Capabilities message is received and processed.
Side Effects	When the 'GSrC' Task completes successfully the *RX_SOURCE_CAPS* register (0x30) will have been updated.
Additional Information	The 'ESrC' Task can only be sent if the PD is capable of operating as a Sink or DRP and supports EPR mode.

5.3.9 'GPPI' - PD Get Port Partner Information

The 'GPPI' Task can be used to cause the PD controller to issue these types of USB PD Get messages:

- Get_Source_Cap_Extended (control message)
- Get_Sink_Cap_Extended (control message)
- Get_Status (Control message)
- Get_Country_Codes (Control message)
- Get_Country_Info (Data message)
- Get_Battery_Status (Extended message)
- Get_Battery_Cap (Extended message)
- Get_Manufacturer_Info (Extended message)

The PD controller does not have dedicated registers to store the response to these messages. The host must get that response from the DATAX register associated with this Task.

The host must NOT use 'GPPI' to send Get_Sink_Capabilities or Get_Source_Capabilities messages, because the USB PD spec requires specific actions be taken by the PD controller any time those messages are received. While executing the 'GPPI' Task, the PD controller does not parse the returned message to carry out those checks. Instead, the host must use 'GSkC' to send Get_Sink_Capabilities and 'GSrC' to send Get_Source_Capabilities messages.

This Task is defined to enable supporting any new Get message that can be defined by USB PD in the future.

Table 5-12. 'GPPI' - Send a USB PD Get* Message

Description	**The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	15	Reserved		
	14:13	FrameType	00b	SOP
			01b	SOP'
			10b	SOP''
			11b	Reserved
	12:8	NumBytes		
	7	Reserved		
	6:5	MessageCategory	00b	Control message (no payload)
			01b	Data message (requires payload)
			10b	Extended message (requires payload)
			11b	Reserved
	4:0	MessageType	This field must be the MessageType as defined in the USB PD specification. It specifies the Type of message the PD controller will send.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.			

Table 5-12. 'GPPI' - Send a USB PD Get* Message (continued)

Description	The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.
Task Completion	The 'GPPI' Task completes either when the appropriate message is received or the Task otherwise fails. The 'GPPI' Task shall be considered rejected if: • Sending the requested message can violate the USB PD spec. For example, the Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The PortPartner replies with a Reject or Not_Supported message. • The USB PD spec revision (PlugPartnerNegSpecRev or PortPartnerNegSpecRev in PD3_STATUS register (0x41) does not allow sending the requested message. The 'GPPI' Task shall be considered timed-out if: • The requested message is sent, GoodCRC'ed and the recipient (Port Partner or Cable Plug) fails to respond within the time required by the PD spec. • A PD Hard Reset or a disconnection happens before the Task completes. The 'GPPI' Task shall be considered successful if: • The requested message is sent, GoodCRC'ed and an appropriate response is received and processed. The 'GPPI' Task shall be aborted when the Rx Buffer is locked. The Rx Buffer is locked after data from a receive message is placed in the DATAX register. The Rx Buffer is unlocked after disconnect and by the 'MBRd' Task.
Side Effects	If necessary, the PD controller can issue a VCONN_Swap in order to send the requested message to a Cable Plug. If the PD controller is in the sink power role and it reads Rp = SinkTxNG, it will wait until Rp = SinkTxOK before initiating the atomic message sequence requested by this 'GPPI' Task. This can cause an non-deterministic delay in completing the Task.
Additional Information	The PD controller will continue trying to execute this Task until it times out or aborts as described above. The host can want to issue the 'ABRT' Task if the process takes too long. Some scenarios where this can happen are: • The PD controller is required to be the VCONN_Source in order to send any message on SOP or SOP'. The PD controller will continue trying to become the VCONN provider until it is successful. • The PD controller with a sink power role (that is PresentRole = Sink) is required to wait for Rp = SinkTxOK before initiating an Atomic Message Sequence. The PD controller will continue waiting for Rp = SinkTxOK until it is able to send the appropriate message required for this 'GPPI' Task. The host must wait until CMDx reads as 0 or INT_EVENT1.CmdComplete is asserted before issuing the 'MBRd' 4CC Task to read the Rx Buffer after issuing this 'GPPI' Task. While executing the 'GPPI' Task, the PD controller uses the same shared buffer that is used to store other extended messages. Therefore, the host must not use the 'GPPI' Task when any other atomic message sequence is ongoing. To read the PD response received as a result of issuing the 'GPPI' Task after it is completed, the host must use the 'MBRd' 4CC command. The 'MBRd' Task must also be used to unlock the Rx Buffer for other incoming message.

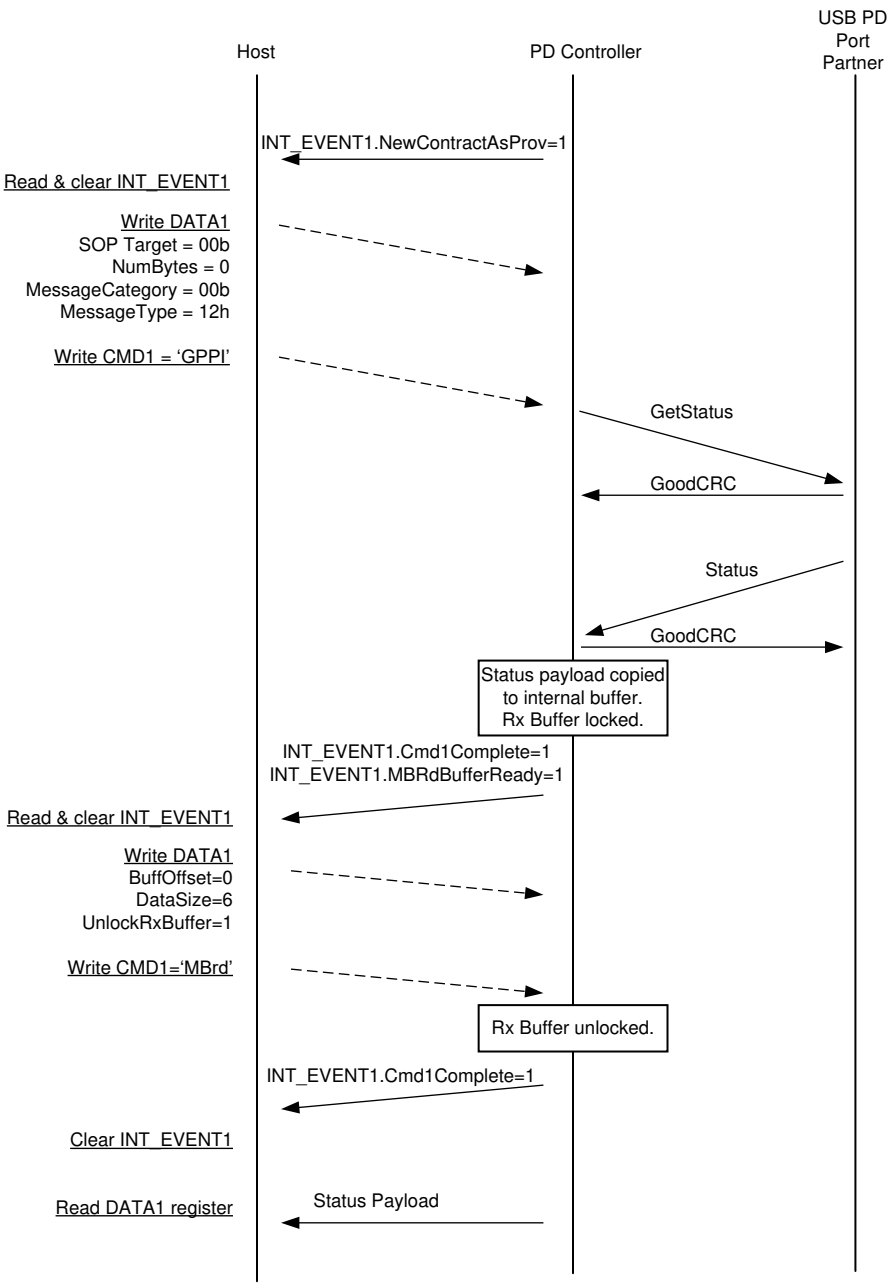


Figure 5-1. Example Sequence for 'GPPI' Task When Host Uses INT_EVENT1

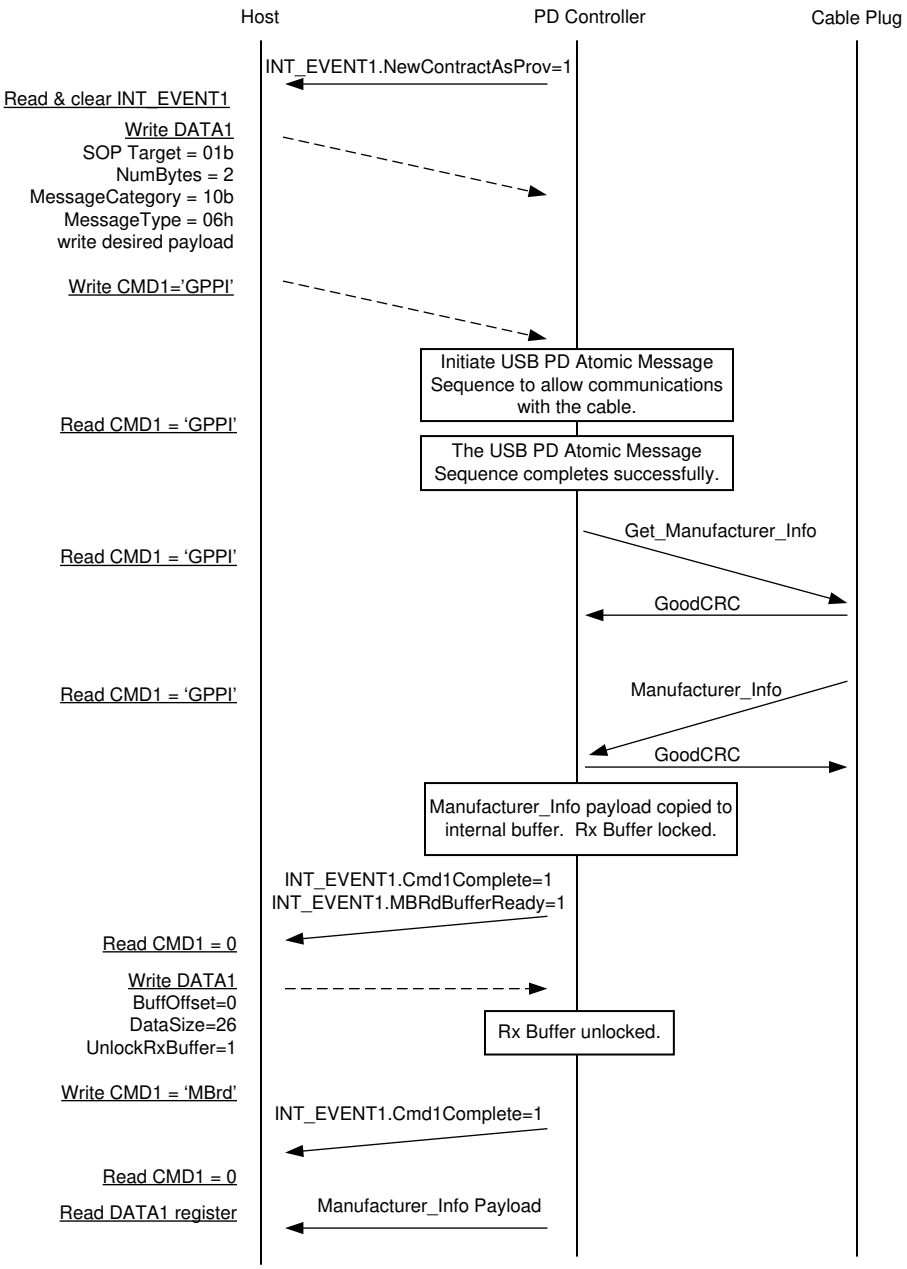


Figure 5-2. Example Sequence for 'GPPI' Task When Host Uses CMD1 Polling

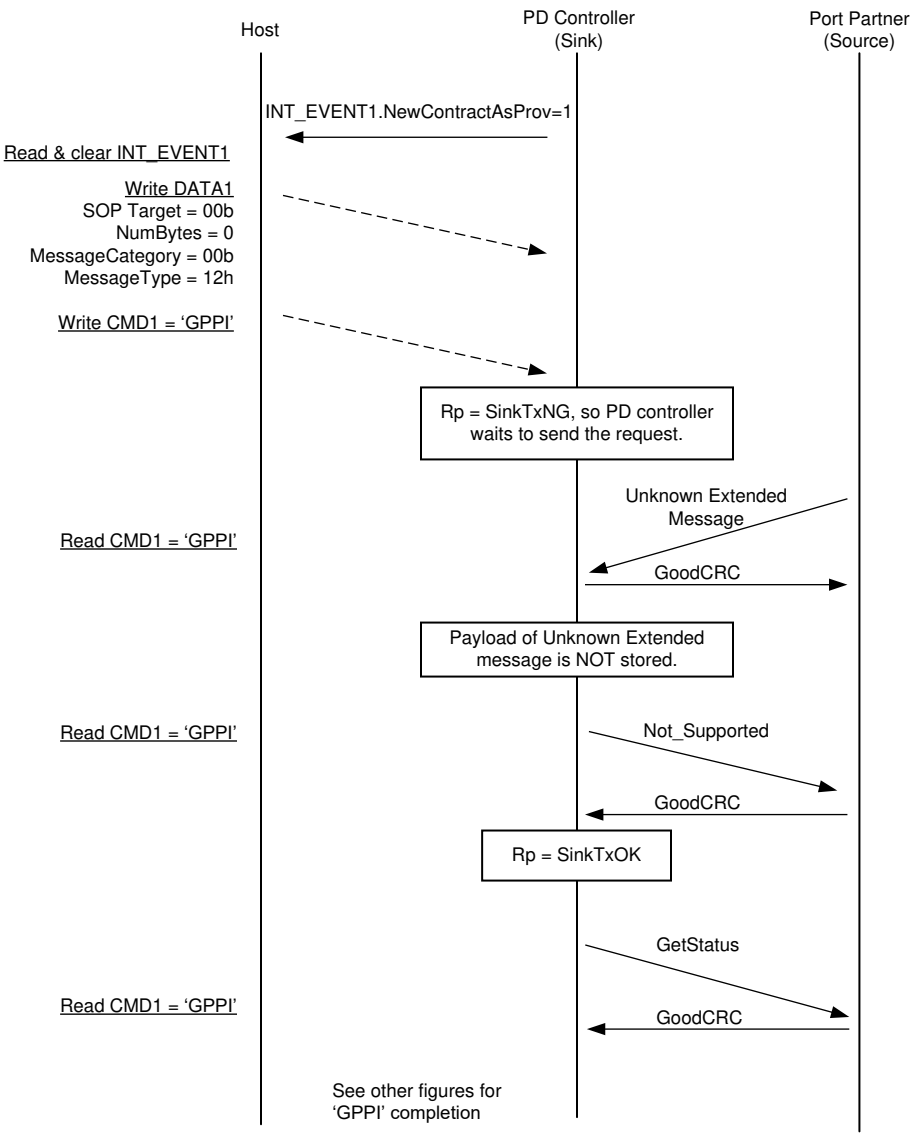


Figure 5-3. 'GPPI' Interrupted by an Unknown Message

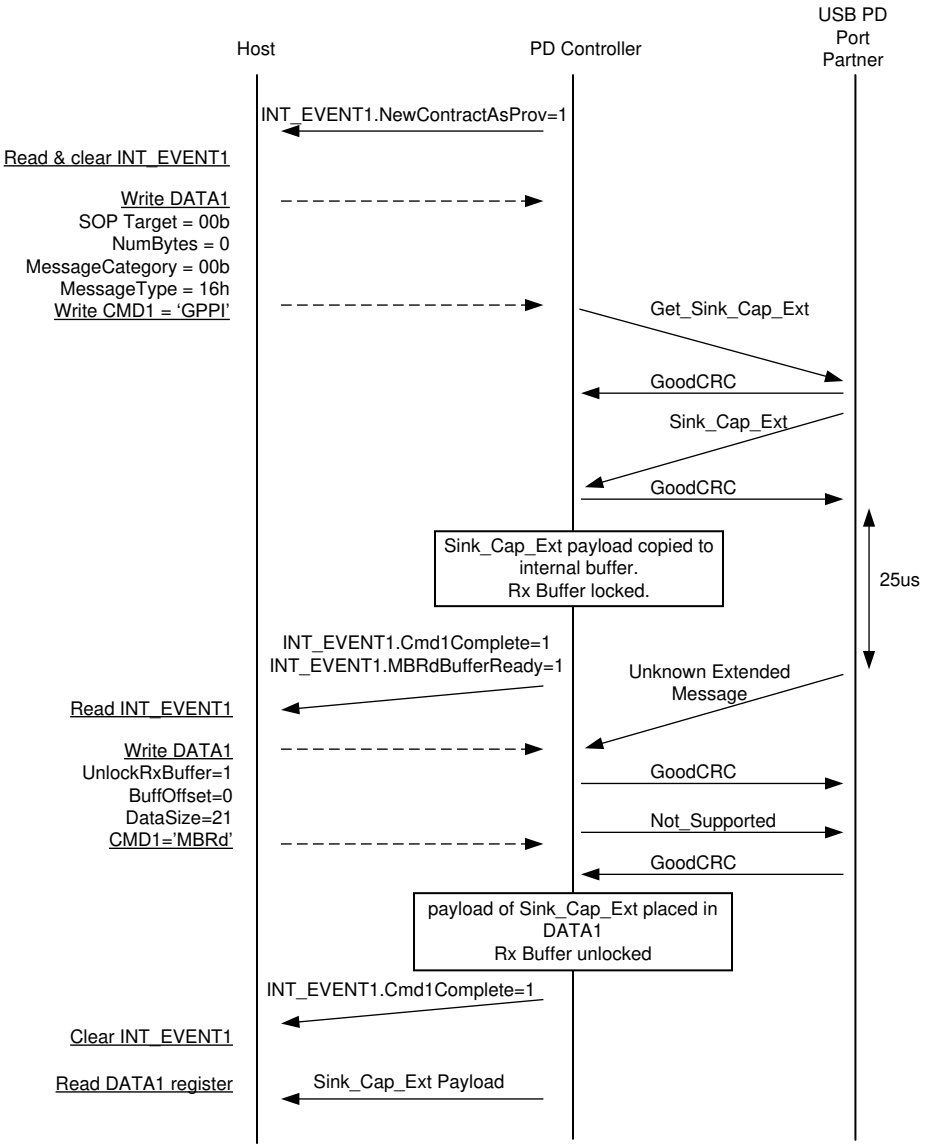


Figure 5-4. 'GPPI' Interrupted by an Unknown Extended Message

5.3.10 'SSrC' - PD Send Source Capabilities

Table 5-13. 'SSrC' - PD Send Source Capabilities

Description	The 'SSrC' Task instructs the PD Controller to send a SourceCapabilities message at the first opportunity while maintaining policy enginecompliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'SSrC' Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails. The 'SSrC' Task shall be considered rejected if: • PD Controller is not in a Source role. The 'SSrC' Task shall be considered timed-out if: • The Source Capabilities message was sent but no GoodCRC was received. The 'SSrC' Task shall be considered successful if: • The Source Capabilities message was sent and a GoodCRC is received.
Side Effects	Other registers can change as a result of the contract negotiation that begins with the new Source Capabilities message.
Additional Information	None

5.3.11 'MBRd' - Message Buffer Read

Table 5-14. 'MBRd' - Read from PD message buffer.

Description	**The MBRd Task instructs the PD Controller to read data from the extended message buffer previously received from the Port Partner.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	23	Reserved	Reserved (Write as 0).	
	22	UnlockRxBuffer	This input controls whether or not the PD controller unlocks its internal buffer after this Task is completed. It is recommended to unlock the internal buffer as soon as possible to make room for other incoming messages. It is important that the host only set this bit to 1 after it has received an alert that the Rx Buffer is locked (that is INT_EVENTx.MBRdBufferReady asserted).	
			0b	Do not clear the internal buffer, another 'MBRd' Task can be used later.
			1b	Clear the internal buffer after this Task completes and the requested data is in the DATAx register.
	21:16	DataSize	Number of data bytes to be read in from the message buffer. Up to 62 bytes can be read at after.	
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible.	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	511:16	DataByte1	First Byte of data read at BuffOffset.	
	15:0	MessageSize	Size of message in bytes.	
Task Completion	The MBRd Task completes after buffer data of DataSize at BuffOffset has been read from the message buffer.			
Side Effects	None			
Additional Information	This Task is required for the host to obtain the information from the response due to the usage of the 'GPPI' Task . The PD controller has a single buffer per port that is shared for these messages.			

5.4 Patch Bundle Update Tasks

The following tasks are used for updating a Patch Bundle.

5.4.1 'PBMs' - Start Patch Burst Mode Download Sequence

Table 5-15. 'PBMs' - Start Patch Burst Download Sequence

Description	**The 'PBMs' Task starts the patch loading sequence. This Task initializes the firmware in preparation for a patch bundle load sequence and indicates what the patch bundle will contain.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	Byte 6: Burst Mode Timeout			
	7:6	Reserved		
	5:0	Timeout value	Timeout value for this task. A non-zero value must be used, it is recommended to always use 0x32 in this field (5 seconds) (LSB of 100ms).	
	Byte 5: I2C target for downloading patch.			
	7	Reserved		
	6:0	I2C target Address	The following target addresses are not valid: • 0x00 • The I2Ct target address of any port selected using the ADCINx pins. Refer to data-sheet.	
	Bytes 0-3: Low Region Binary bundle size in of bytes: [Byte4, Byte3, Byte2, Byte1]			
	39:32	Byte4 of bundle size		
	31:24	Byte3 of bundle size		
	23:16	Byte2 of bundle size		
	15:8	Byte1 of bundle size		
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	PatchStartStatus	Status of the patch start.	
			0x00	Patch start success
			0x04	Invalid bundle size
			0x05	Invalid target address
			0x06	Invalid Timeout value
Task Completion	The 'PBMs' Task completes after output has a valid PatchStartStatus. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			
Side Effects	When the 'PBMs' is successful, the second target address will be set to the input value.			
Additional Information	The host can only issue a 'PBMs' Task to the I2Ct port of the PD controller. If the host issues 'PMBs' a second time, then the PD controller ignores the DATAX input, restarts the burst-mode timer, and resets the pointer to the beginning of the patch space in RAM. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMs' Task.			

5.4.2 'PBMc' - Patch Burst Mode Download Complete

Table 5-16. 'PBMc' - Patch Burst Download Complete

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**			
INPUT DATAX	None			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	319:288	acCalculatedCRC	The CRC calculated in FW for the configuration data.	
	287:256	acTransferredCRC	The CRC transferred along with the configuration data	
	255:240	Reserved	reads as 0	
	239:224	acIndicatedDataSize	The indicated DataSize in the transferred configuration data.	
	223:216	acHeaderVersion	The indicated header version in the transferred configuration data.	
	215:208	acFailCode	An error code indicating why the app config data failed to apply, if it failed to apply	
			0x00	AC_FAIL_NONE: No failure
			0x01	AC_FAIL_WRONG_HEADER_VERSION: The header version is expected to be 1 and was not
			0x02	AC_FAIL_TOO_MUCH_DATA: The DataSize field indicates that you are trying to load more configuration data that there is allocated SRAM for
			0x03	AC_FAIL_CRC_CHECK_FAIL: The CRC comparison failed
	207:200	acState	The current internal state of the AppConfig state machine	
			0x00	AC_NODATA: No configuration data found yet, because we haven't started looking
			0x01	AC_LOADING_DEFAULT: Attempting to load configuration data from a factory default
			0x02	AC_LOADING_SRAM: Attempting to load configuration data from SRAM
			0x03	AC_LOADING_FLASH: Attempting to load configuration data from Flash
			0x04	AC_LOADING_I2C: Attempting to load configuration data from I2C
			0x05	AC_LOADING_DONE: Done loading configuration data, we found valid data
			0x06	AC_ERROR: A generic error state
			0x07	AC_DONE_SUCCESS: Completely done with the app customization process and the records were applied successfully.
			0x08	AC_DONE_FAIL: Completely done with the app customization process and the records were not applied
	199:192	configBundleGood	1 if the top-level state machine found a valid configuration bundle, otherwise 0.	
	191:160	rpRomVersionExpected	The romVersionExpected in the transferred bundle's patch header	
	159:144	rpBundleTotalSize	The bundleTotalSize in the transferred bundle's patch header	
	143:128	rpBundleFlags	The bundleFlags in the transferred bundle's patch header	
	127:96	rpPatchBodyCrc	The patchBodyCrc in the transferred bundle's patch header	
	95:64	rpPatchHeaderCrc	The patchHeaderCrc in the transferred bundle's patch header	

Table 5-16. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	55:48	rpBundleSignature	The bundleSignature in the transferred bundle's patch header	
	47:40	rpState	The current internal state of the RomPatch state machine.	
			0x00	RP_NOPATCH: No patch has been loaded
			0x01	RP_LOADING: In the process of loading patch data
			0x02	RP_LOADINGDONE: All patch data has been received
			0x03	RP_RUNNING: A patch has been loaded and is running. Could also indicate that a NULL patch is active.
			0x04	RP_EARLYLOAD_SKIPPED: Indicates that the early boot process does not need to wait for a patch over I2C
			0x05	RP_UARTBOOTED: Checking for a patch in RAM
			0x06	RP_ERROR: A generic error state
	39:32	patchBundleGood	0x01 if the top-level state machine found a good ROM patch, otherwise 0x00.	
	31:24	AppConfigPatchCompleteStatus	0x00	
			0x40	Warning
			0x80	Failure
	23:16	DevicePatchCompleteStatus	A return code indicating whether the RomPatch state machine executed successfully. This value is always valid, and reflective of the internal state of the RomPatch mechanism, but must only be considered if the bundle transferred did in fact include patch data.	
			0x00	Success
			0x20	Not ready
			0x40	Not a patch
			0x41	Patch header checksum mismatch
			0x42	Patch not compatible with this version of ROM
			0x43	Patch code checksum mismatch
			0x44	Null patch received
			0x45	Error patch received
	15:8	cpReturn	Always returns success, there is no way for it to fail.	
	Byte 1: Return Code			
	7:4	rpReturnIndicator	The most significant nibble of the rpReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
	3:0	acReturnIndicator	The most significant nibble of the acReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
Task Completion	The 'PBMc' Task completes as output has a valid DevicePatchCompleteStatus and AppConfigPatchCompleteStatus. This Task is rejected if the DATAX input does not contain the total patch size. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			

Table 5-16. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**
Side Effects	Before this Task completes it will change the I2C target address from the patch address back to the normal value. Upon successful completion of this Task the PD controller will change the MODE register (0x03) to 'APP ' and move to the application mode.
Additional Information	When the CMDx register goes to 0 check the Output DATAX register for status. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMc' Task.

5.4.3 'PBMe' - End Patch Burst Mode Download Sequence

Table 5-17. 'PBMe' - Patch Burst Mode Exit

Description	The 'PBMe' Task ends the patch loading sequence. This Task instructs the PD controller to complete the patch loading process.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'PBMe' Task completes after it has ended the patch loading sequence. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.
Side Effects	When the 'PBMe' is successful, the second target address will be restored to the value configured by the ADCINx pins. The PD controller leaves the MODE register (0x03) as 'PTCH' and will wait for the patching process to restart.
Additional Information	If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMe' Task.

5.4.4 'GO2P' - Go to Patch Mode

Table 5-18. 'GO2P' - Forces PD controller to return to 'PTCH' mode and wait for patch over I2C.

Description	The 'GO2P' Task causes the PD controller to re-enter the patch mode (MODE = 'PTCH').
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.
Task Completion	The 'GO2P' Task completes after the PD controller has re-entered the patch mode. • If the PD controller has re-entered the patch mode and the MODE register reads as 'PTCH'. The 'GO2P' Task is considered rejected if: • The PD controller did not enter the 'APP' mode without receiving a patch over I2C. • The PD controller did not enter the 'APP' mode with ADCINx configuration option 'NegotiateHighVoltage'.
Side Effects	When the 'GO2P' Task is successful, the MODE register will read as 'PTCH' and the USB PD PHY will be disabled. The PD Controller can temporarily NAK I2C transactions. The host must wait for the IRQ signal to assert (because INT_EVENT1.ReadyForPatch is asserted), and then push the patch as soon as possible.
Additional Information	The 'GO2P' Task must only be used when the ADCINx configuration option NegotiateHighVoltage is used. This task cannot be used with any other available ADCINx configurations.

5.4.5 'FLrd' - Flash Memory Read

Table 5-19. 'FLrd' - External EEPROM Read

Description	The 'FLrd' Task reads the flash at the specified address.		
INPUT DATAX	**Bit**	**Name**	**Description**
	31:0	Flash Address	Flash Address
OUTPUT DATAX	**Bit**	**Name**	**Description**
	127:0	Memory Contents	Memory contents (little-endian).
Task Completion	The 'FLrd' Task completes after selected memory locations are loaded.		
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.		
Additional Information	None		

5.4.6 'FLad' - Flash Memory Write Start Address

Table 5-20. 'FLad' - External EEPROM Start Address

Description	The 'FLad' Task sets start address in preparation the flash write.		
INPUT DATAX	**Bit**	**Name**	**Description**
	31:0	Flash Address	Flash address (treated as 32-bit little-endian value).
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.		
Task Completion	The 'FLad' Task completes after selected memory address is loaded.		
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.		
Additional Information	None		

5.4.7 'FLwd' - Flash Memory Write

Table 5-21. 'FLwd' - External EEPROM Memory Write

Description	**The 'FLwd' Task writes data beginning at the flash start address defined by the 'FLad' Task. The address is auto-incremented.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	511:0	Flash Address	Up to 32 bytes of flash data.	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	ReturnCode	Status of write.	
			0x00h	Flash memory write successful
			0xFFh	Error, flash is busy
Task Completion	The 'FLwd' Task completes after selected the flash is written.			
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.			
Additional Information	None			

5.4.8 'FLvy' - Flash Memory Verify

Table 5-22. 'FLvy' - External EEPROM Verify

Description	**The 'FLvy' Task verifies if the patch/configuration is valid.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	31:0	Flash Address	Flash Address	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	ReturnCode	0x00h	The patch/configuration is valid.
			0x01h	The patch/configuration is not valid.
Task Completion	The 'FLvy' Task completes after header is checked and validated.			
Side Effects	The PD controller ignores the I2Cc_IRQ pin until this Task is completed.			
Additional Information	None			

5.5 System Tasks

5.5.1 'DBfg' - Clear Dead Battery Flag

Table 5-23. 'DBfg' - Clear Dead Battery Flag

Description	The 'DBfg' Task is used to clear the dead battery flag. This Task does not disable the PP_EXT input switch that can have been enabled during dead battery operation.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	The 'DBfg' Task completes after the effects of clearing the Dead Battery Flag are complete.
Side Effects	The Dead Battery Flag causes the PD Controller to take specific actions, so clearing this flag will have side effects. PD Controller 's power input is forced to VBUS until the Dead Battery Flag is cleared, so executing this Task will change PD Controller 's power input.
Additional Information	None

There are several limitations placed on the PD controller while the Dead-Battery Flag is asserted (PowerPathStatus.PowerSource = 10b).

- Fast-Role swap is not supported (on either port).
- A Hard Reset will not be transmitted while in the sink role (on either port).
- VBUS is selected as the main supply for the PD controller, even if the 3.3 V input is present.
- The PD controller will reject PR_Swap requests to become source (on either port).
- The 2nd port in the PD controller that is unconnected will only offer the USB Type-C Default Rp (PortControl.TypeCCurrent is ignored) if it connects as a source.
- A port connected to a source will only act as a Type-C sink regardless of the configuration.
- If no Source Capabilities message is received after the boot process is complete (Status.ActingAsLegacy=11b), the PD controller will not send a Hard Reset until the Dead-Battery Flag is cleared even if the SinkWaitCapTimer expires.

5.5.2 'I2Cr' - I2C read transaction

Table 5-24. 'I2Cr' - Executes I2C read transaction on I2Cc.

Description	**The 'I2Cr' task can be used to cause the PD controller to read from a specified target address and register offset using a I²C read transaction through the I2Cc_SDA and I2Cc_SCL pins.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 3: Number of bytes to read from the target.		
	7:0	NumBytes	
	Byte 2: Register offset to use in the I2C read transaction.		
	7:0	RegisterOffset	
	Byte 1: Target Address		
	7	Reserved	
	6:0	target to use for the transaction.	
OUTPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 2-65: Data Bytes read from the target (in order received)		
	511:0	Data	
	Byte 1: Standard Task Return Code. See also Table 5-1.		
Task Completion	The PD controller completes after it has succesfully read the specified number of bytes, or the I²C transaction terminated for some other reason.		
Side Effects	This task will cause the PD controller to issue a command on the I2Cc port. It can result in INT_EVENTx.I2CControllerNACKed being asserted.		
Additional Information	None		

5.5.3 'I2Cw' - I2C write transaction

Table 5-25. 'I2Cw' - Executes I2C write transaction on I2C3m.

Description	**The 'I2Cw' task can be used to cause the PD controller to write a particular I²C transaction using I2Cc_SDA and I2Cc_SCL.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 4-14: Payload for the I2C transaction		
	Byte 3: Register Offset for the I2C transaction		
	7:0	Register offset	
	Bytes 2: Length		
	7:0	Number of bytes in the transaction payload.	
	Byte 1: Target Address		
	7	Reserved	
	6:0	Target to use for the transaction.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.		
Task Completion	The PD controller maintains a queue of transactions to send on the I2Cc port. If the PD controller has been configured to send transactions upon certain events, it is possible there is a transaction in the queue when the 'I2Cw' task is received. In that case the task will complete successfully after the transaction is inserted into the queue. If the PD controller fails to insert the task into the queue for any reason, the task is rejected. Therefore, when this task is completed succesfully it does not guarantee that the I2C transaction is complete. If possible, the host must use the 'I2Cr' 4CC task to confirm the write was successful.		
Side Effects	When successful, this task will cause the PD controller to issue a command on the I2Cc port. This can result in INT_EVENTx.I2CControllerNACKed being asserted.		
Additional Information	If the DATAX register is written with more than 14 bytes, all bytes beyond byte 14 are ignored. The PD controller has a limit on the maximum length of the I²C write transaction.		

5.5.4 'GPsh' - set GPIO high

Table 5-26. 'GPsh' - GPIO set output high

Description	This Task sets the selected GPIO pin output to logic high.		
INPUT DATAX	Bit	Name	Description
	Byte 1: GPIO number		
	7:0	GPIOnum	GPIO number, check device data-sheet for available GPIO's. For example, GPIOnum = 0 corresponds to GPIO0.
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.		
Task Completion	The ‘GPsh’ Task completes after the new GPIO value is committed to the GPIO register.		
Side Effects	There are many possible expected or unexpected side effects of changing the PD Controller’s GPIOs manually. GPIOs that are connected to PD Controller GPIO Events can not behave properly if they are modified by the ‘GPIO’ Command. Extreme care must be taken with the use of this Task.		
Additional Information	GPIOs must be configured as an output in the App Config for 'GPsO' to work. Use the GPIO Mapped Event "Output Enabled without Event" to configure the GPIO as an output. Use the "Initial Value" field to set the initial value.		

5.5.5 'GPsl' - set GPIO low

Table 5-27. 'GPsl' - GPIO set output low

Description	This Task sets the selected GPIO pin output to logic low.		
INPUT DATAX	Bit	Name	Description
	Byte 1: GPIO number		
	7:0	GPIOnum	GPIO number, check device data-sheet for available GPIO's. For example, GPIOnum = 0 corresponds to GPIO0.
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 5-1.		
Task Completion	The ‘GPsl’ Task completes after the new GPIO value is committed to the GPIO register.		
Side Effects	There are many possible expected or unexpected side effects of changing the PD Controller’s GPIOs manually. GPIOs that are connected to PD Controller GPIO Events can not behave properly if they are modified by the ‘GPIO’ Command. Extreme care must be taken with the use of this Task.		
Additional Information	GPIOs must be configured as an output in the App Config for 'GPsl' to work. Use the GPIO Mapped Event "Output Enabled without Event" to configure the GPIO as an output. Use the "Initial Value" field to set the initial value.		

6.1 PD Controller Application Customization

The PD Controller application binary can be pushed over I2C using the I2Ct port, or the PD controller can read it from an external EEPROM at target address 0x50 on the I2Cc port. The PD Controller application binary provides a way to customize and initialize the settings of the PD Controller. It allows for any register bit accessible through the Host Interface to be changed *before* the PD Controller application starts normal operation, to configure system-related settings that must be correct before any application decision is made. TI provides a GUI tool to create the PD Controller application binary.

6.2 Loading a Patch Bundle

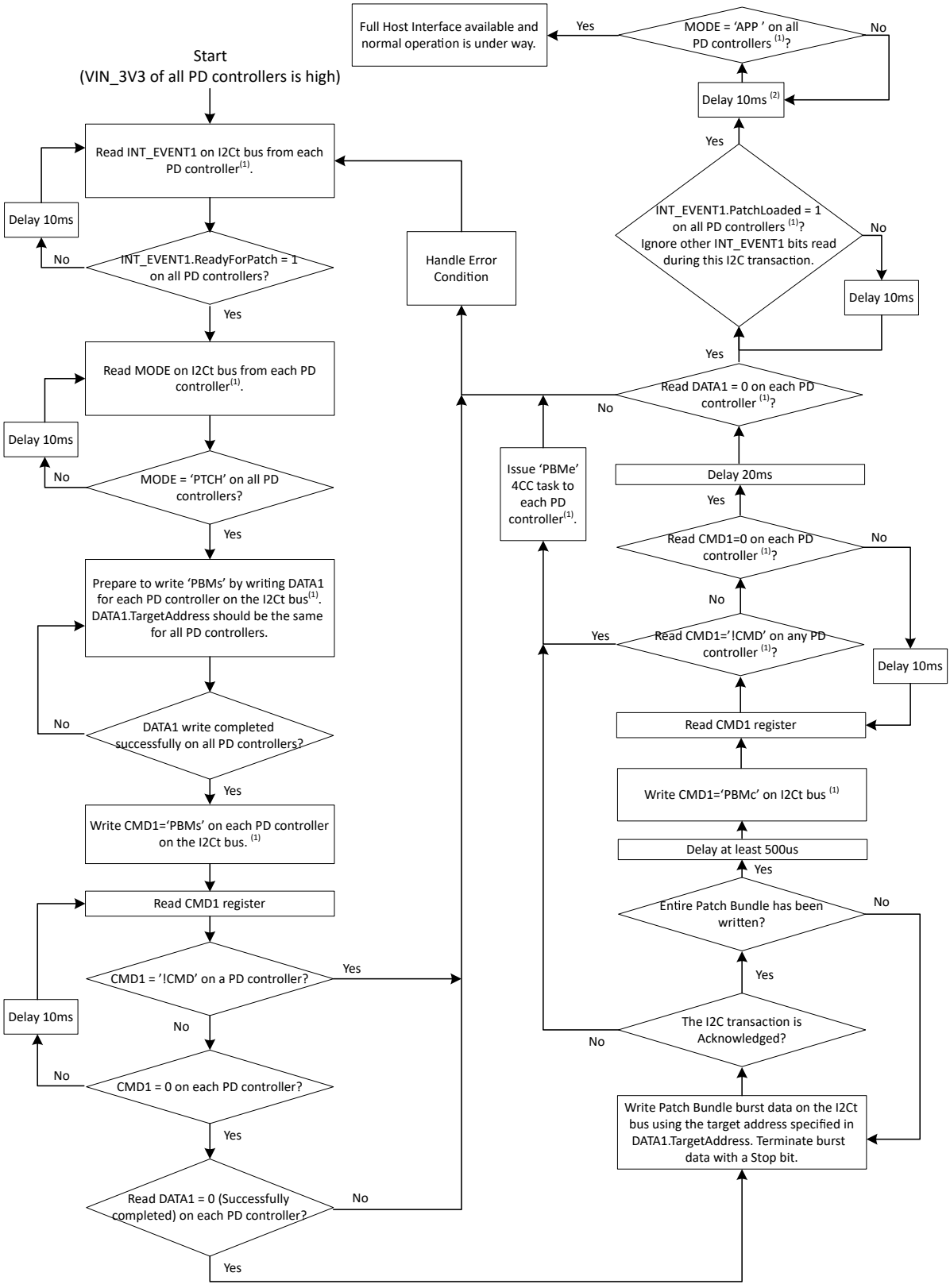
The patch bundle can contain Application Customization data and a Patch binary that modifies the default application firmware in the PD controller. This section will describe how the host can load the patch bundle. The host uses the I2Ct bus for all transactions related to loading the patch bundle. As noted in the flow diagram below, the I2C target address varies depending upon which mode the PD controller is in. The Patch Burst Mode allows the host to push the Patch Bundle to multiple PD controllers simultaneously.

The following flow diagram illustrates the normal successful patch loading process. Other error handling steps can be necessary depending upon the nature of the errors encountered for a particular system. The EC can reset and restart the patch process by issuing a 'PBMe' 4CC Task.

Table 6-1. Use of Target Addresses During Different Modes of Operation

MODE Register Read-Back Value	I2Ct
	Target Address 1
'BOOT'	As configured by ADCINx pins. This is the "Fundamental" I2C target address. BOOT indicates that the PD controller is in the boot stage due to a bad firmware image or incorrect ADCINx settings. APP indicates that the firmware has successfully loaded and is in normal operation. PTCH indicates that the PD controller is waiting for a patch or is in the patch process using the PBMx commands.
'PTCH'(1)	
'APP '(2)	

(1) A successful 'PBMs' Task puts the PD controller into the 'PTCH' mode.
(2) A successful 'PBMc' Task puts the PD controller into the 'APP ' mode.



(1) Use the fundamental I2C target address of each PD controller.
(2) This delay before reading the MODE register, is optional but recommended.

Figure 6-1. Flow for Pushing a Patch Bundle Over the I2Ct Bus to Multiple PD Controllers at the Same Time

While the host is writing the Patch Bundle burst data, the I2C protocol in the following figure must be followed. The host can send the entire Patch Bundle in a single I2C transaction, or it can break it up into multiple transactions. The PD controller increments the pointer into its patch memory space with each byte received on the Patch Target address that was configured by DATA1.TargetAddress as part of the 'PBMs' 4CC Task. The EC can re-issue a 'PBMs' 4CC Task or it can issue a 'PBMe' 4CC Task in order to reset the pointer.

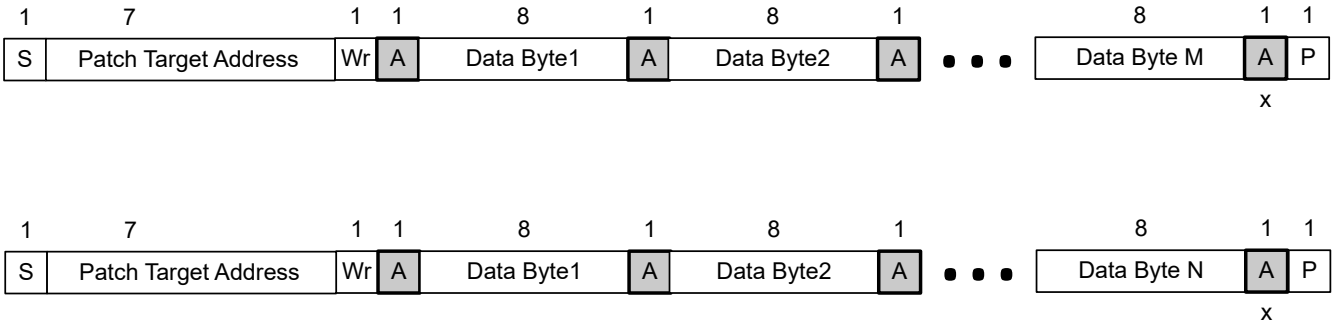


Figure 6-2. Protocol of Patch Bundle Burst Data Assuming it is Broken Into Two Transactions

6.3 AUTO_NEGOTIATE_SINK Register

In general, writing to AUTO_NEGOTIATE_SINK register while a sink contract is in place will not cause an automatic renegotiation, changes will take effect the next time a contract is negotiated. The GSrC command forces a re-evaluation of this register and a new Request message will be issued if appropriate.

However, if a Sink PPS Explicit Contract is already in place there are some fields that do cause the PD controller to automatically reevaluate the register and send a new Request message if appropriate:

- PPSOutputVoltage
- PPSOperatingCurrent
- PPSEnableSinkMode
- PPSRequestInterval
- RequireFullVoltageRange
- PPSSourceMode

If PPSEnableSinkMode is changed while a Sink PPS Explicit Contract is not already in place the PD controller also automatically re-evaluates the register and sends a new Request message if appropriate.

If the first four bytes of this register are written as zero, then the PD controller will always request a 5V Fixed Suppy contract at 100 mA ; unless PPSEnableSinkMode is asserted in which case an APDO can be selected.

In order to implement Sink PPS features in this register, the host shall provide an APDO in the TX_SINK_CAPS register. If the PD controller is evaluating a PPS supply type, it only uses the first APDO in the TX_SINK_CAPS register to determine when to assert the Capability Mismatch bit. Therefore, it is recommended that the host only have one APDO in the TX_SINK_CAPS register. In order to not assert the Capability Mismatch bit, the source APDO advertised by the source must meet these conditions:

- RX_SOURCE_CAPS.APDO.MinVoltage <= TX_SINK_CAPS.APDO.MinVoltage
- RX_SOURCE_CAPS.APDO.MaxVoltage >= TX_SINK_CAPS.APDO.MaxVoltage
- RX_SOURCE_CAPS.APDO.MaxCurrent >= TX_SINK_CAPS.APDO.MaxCurrent

If the source fails any of the conditions above, a sink PPS contract is still requested if one of the source's APDO's meets these conditions:

- RX_SOURCE_CAPS.APDO.MinVoltage <= AUTO_NEGOTIATE_SINK.PPSOutputVoltage
- RX_SOURCE_CAPS.APDO.MinVoltage >= AUTO_NEGOTIATE_SINK.PPSOutputVoltage
- RX_SOURCE_CAPS.APDO.MaxCurrent >= AUTO_NEGOTIATE_SINK.PPSOperatingCurrent

During PPS operation, if the host sets the PPSOutputVolage field to a value outside what the source's APDO can deliver as reported in the RX_SOURCE_CAPS register, then a Fixed Supply PDO will be selected and the sink path can be automatically disabled (see AUTO_NEGOTIATE_SINK.PPSDisableSinkUponNonAPDOContract).

If PPS is enabled, then an APDO that fulfills the requirements is given highest priority.

Below is a highlevel summary of how this register drives the PDO selection when PPS is disabled or no matching APDO is found.

- Parse the received PDO's in the register RX_SOURCE_CAPS. Discard any PDO whose voltage range is below ANMinVoltage or above ANMaxVoltage.
- Calculate the PDO power for each received PDO (RX_SOURCE_CAPS.SourcePdoX). Rank all PDO's according to the PDO power.
  - PDO Power = Voltage * MaximumCurrent (Fixed Supply)
  - PDO Power = MinimumVoltage * MaximumCurrent (Variable Supply)
  - PDO Power = MaximumPower (Battery Supply)
- The PDO with maximum PDO Power that also passes the voltage check is selected. In case there are multiple PDO's that pass the voltage check and have the same maximum PDO Power, several tie breakers are applied as described below:
  - A Fixed supply type is preferred, and Variable supply type is preferred over Battery supply type.
  - If the PDO's being compared have the same supply type, then ANRDOPriority specifies how to break the tie.

6.3.1 AUTO_NEGOTIATE_SINK usage example #1

When attached to a 36W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 2.4A
- PDO4: 20V @ 1.8A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 3A (fixed)
- PDO2: 20V @ 3A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.ANSinkCapMismatchPower = 240d (60W)
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = x (see table below)
- AUTO_NEGOTIATE_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 60 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

Table 6-2. AUTO_NEGOTIATE_SINK usage example #1.

AUTO_NEGOTIATE_SINK		ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	**ANRDOPriority**	**OperatingX**	**MinMaxOperatingX**	**ObjectPosition**	**Capability Mismatch**
0	0	1.8A	3.0A	4	1

Table 6-2. AUTO_NEGOTIATE_SINK usage example #1. (continued)

AUTO_NEGOTIATE_SINK		ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
1	0	1.8A	1.8A	4	0
1	1	2.4A	2.4A	3	0

6.3.2 AUTO_NEGOTIATE_SINK usage example #2

When attached to a 36W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 2.4A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 0.1A (fixed)
- PDO2: 20V @ 3A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 0
- AUTO_NEGOTIATE_SINK.ANMinVoltage = 20V
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = x (see table below)
- AUTO_NEGOTIATE_SINK.ANRDOPriority = 0

The settings give the results in the table below. Note that ANMaxVoltage computed as 20V, but it doesn't affect the result. Because the ANMinVoltage was set to 20V, and the source is not offering 20V none of the source PDO's fulfill the sink requirements. Even though ANSinkCapMismatchPower=0 in this example, because the voltages offered are insufficient, the capability mismatch bit can still be set.

Table 6-3. AUTO_NEGOTIATE_SINK usage example #2.

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	3.0A	3.0A	1	1
1	3.0A	3.0A	1	0

6.3.3 AUTO_NEGOTIATE_SINK usage example #3

When attached to a 45W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 3A
- PDO4: 20V @ 2.25A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 3A (fixed)
- PDO2: 20V @ 2.25A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.ANSinkCapMismatchPower = 180d (45W)
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 1

- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = 0
- AUTO_NEGOTIATE_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 45 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

Table 6-4. AUTO_NEGOTIATE_SINK usage example #3.

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	2.25A	2.25A	4	0
1	3.0A	3.0A	3	0

6.3.4 AUTO_NEGOTIATE_SINK usage example #4

When attached to a 100W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 3A
- PDO4: 20V @ 5A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 3A (fixed)
- PDO2: 20V @ 5A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.ANSinkCapMismatchPower = 240d (60W)
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = 0
- AUTO_NEGOTIATE_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 100 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

Table 6-5. AUTO_NEGOTIATE_SINK usage example #3.

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	5A	5A	4	0
1	5A	5A	4	0

6.4 IO_CONFIG Register

The figure below shows the interface for the GPIO hardware. The register fields GPIO_AI_EN, GPIO_PD_EN, GPIO_PU_EN, GPIO_OE, and GPIO_OD_EN listed in the table below are passed along to the GPIO hardware, independent of the GPIO Event that is configured. The PD controller will then set the signal GPIO_O to high or low to implement the selected output GPIO event. So for example, each output GPIO Event is configurable as

push-pull or open-drain using the GPIO_OD_EN bit. For input GPIO events the PD controller will monitor GPIO_I from the figure.

A given GPIO Event can only be assigned to one GPIO pin.

The ProcHot_N_Event GPIO Event can be assigned to any GPIO, but for some PD controllers only a specific GPIO will have the fast reaction time feature (see device data-sheet).

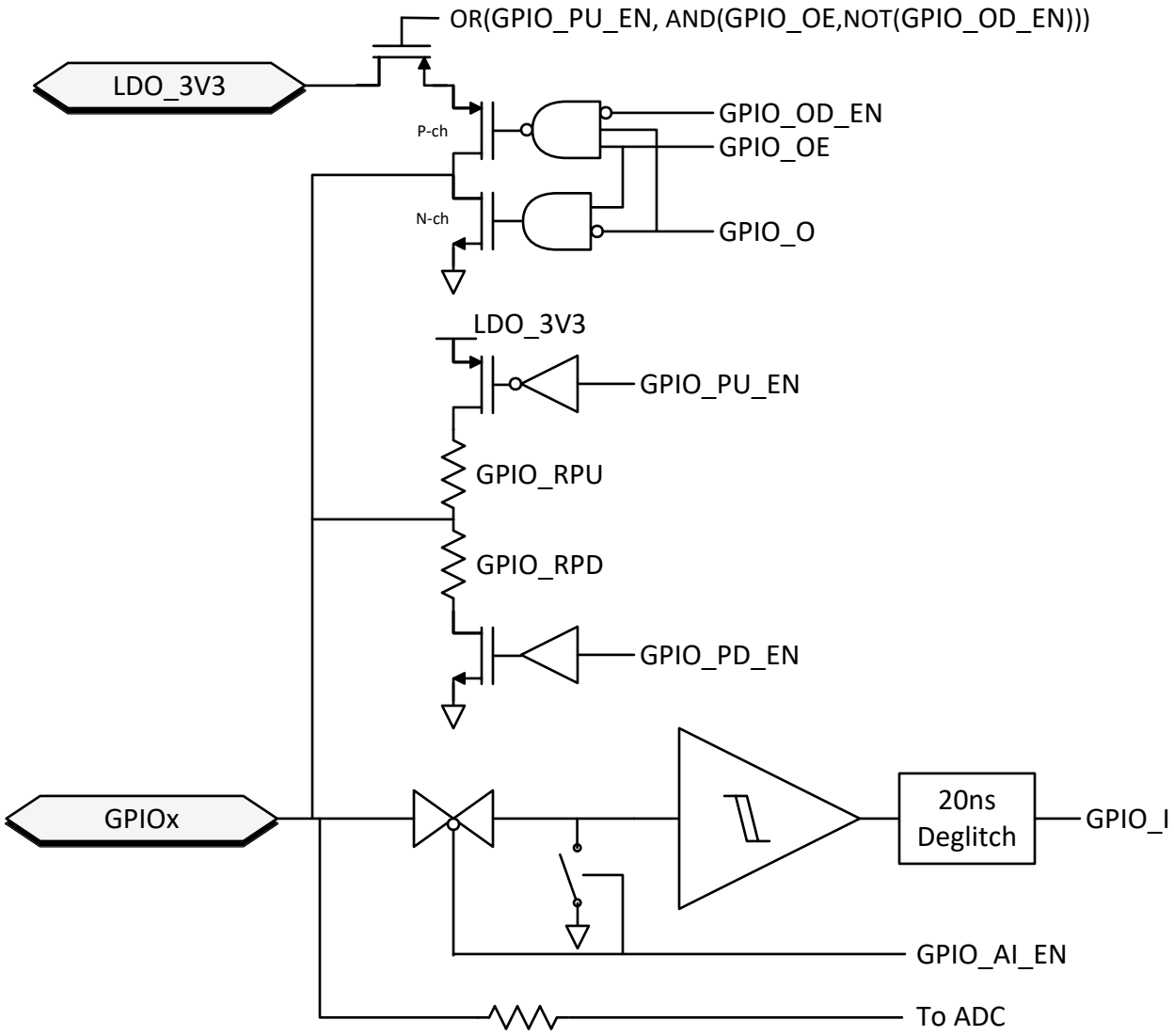


Figure 6-3. Interface to GPIO hardware

6.4.1 GPIO Events

Table 6-6. GPIO Events

Event #	Event Name	I/O	Description
158	WAIT_nPG	Input	GPIO from battery charger to indicate to the PD controller can communicate over I2C during a dead battery power up condition.
157	LIQUID_DETECTED	Output	GPIO is asserted when liquid is detected on the SBU1/2 pins. When liquid is no longer detected on the SBU1/2 pins the GPIO will be de-asserted.
156	LIQUID_NMOS_CONTROL	Output	GPIO used to enable the NMOS in the external liquid detection circuit. The GPIO will toggle during liquid detection.

Table 6-6. GPIO Events (continued)

Event #	Event Name	I/O	Description
155	LIQUID_PMOS_CONTROL	Output	GPIO used to enable the PMOS in the external liquid detection circuit. The GPIO will toggle during liquid detection.
142	EPR_DISCHARGE_EVENT	Output	GPIO is enabled when there is a disconnect or a negative voltage tranistion in EPR mode. This GPIO drives an external discharge circuit.
92	VBUS_SENSE_DIVIDER	Output	GPIO is enable whenever the PD controller is transitioning into EPR mode. This GPIO will enable the external VBUS divider to keep the voltage range within the tolerance of the PD controller.
76	PdNegotiationInProcess	Output	When in source mode, this GPIO is asserted after a Request message is received, before sending the Accept message. The GPIO is de-asserted after the PS_RDY message is sent. When in sink mode, this GPIO is asserted right before sending a Request message, and de-asserted after a PS_RDY message is received. In either mode, the GPIO is de-asserted when a detach occurs.
75	AttachedAsSink	Output	When the PD controller has a port that is connected to a Source, this GPIO will be asserted. The GPIO is de-asserted upon disconnect, hard reset, during power-role swap and during fast-role swap only if none of the ports in the PD controller are connected to a source.
73	EnableSource_Port1	Output	PD controller will assert this GPIO when acting as a source (implicit or explicit contract)
65	Load_Switch_Drive_Port1	Output	When the PD controller enables the PP_EXT1 sinking path, it will pull the selected GPIO low to enable a load-switch. When the PD controller disables the PP_EXT1 sinking path, it will drive the selected GPIO high.
61	Dp_Dm_Mux_Enable_Event_Port1	Output	This GPIO must be used to enable/disable a USB 2.0 D+/D- mux. The GPIO is driven high upon connection, and low upon disconnect on Port1.
50	Debug_Accessory_Mode_Event_Port1	Output	Output: This GPIO is asserted high when a Debug Accessory is attached on Port1.
45	Prevent_DRSwap_To_UFP_Event	Input	When the GPIO is high, the PD controller will reject any DR_Swap messages from the Port Partner requesting to change the data-role from DFP to UFP.
44	UFP_Indicator_Event	Output	The GPIO is driven high when the data role of any port in the PD controller is UFP.
43	Barrel_Jack_Event	Input	When this GPIO is high, the PD controller interprets it to mean that a barrel-jack adaptor is connected and the system has Unconstrained power. A falling edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 0 and TX_SCEDB.SourceInputs[0] to 0. A rising edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 1 and TX_SCEDB.SourceInputs[0] to 1.
35	Fault_Condition_Active_Low_Event_Port1	Output	Asserts low on an overcurrent event on Port1.
33	Fault_Input_Event_Port1	Input	When set low by the system, Port1 enters the Type-C Error Recovery State. When set high, no action is taken.
29	UFP_DFP_Event_Port1	Output	Output: Asserted high when Port1 is operating as UFP. Asserted low when port is operating as DFP.
13	SourcePDOContractBit2_Port1	Output	Output: Bit2 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).

Table 6-6. GPIO Events (continued)

Event #	Event Name	I/O	Description
12	SourcePDOContractBit1_Port1	Output	Output: Bit1 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
11	SourcePDOContractBit0_Port1	Output	Output: Bit0 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
10	SourcePDO4Contract_Port1	Output	Output: Asserted high when a Source PDO4 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
9	SourcePDO3Contract_Port1	Output	Output: Asserted high when a Source PDO3 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
8	SourcePDO2Contract_Port1	Output	Output: Asserted high when a Source PDO2 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
7	SourcePDO1Contract_Port1	Output	Output: Asserted high when a Source PDO1 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO1 has been negotiated.
3	Cable_Orientation_Event_Port1	Output	Output: Indicates the plug orientation on Port1. Low when the plug is connected upside-up (CC1 connected to CC in cable) or disconnected. High when plug is connected upside-down (CC2 connected to CC in cable).
1	PlugEvent_Port1	Output	Output: Asserted high when plug event (attached state) has occurred on Port1, otherwise low.
0	NullEvent	NA	No event associated with this GPIO.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2024	*	Initial Release

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