User's Guide

TPS62913 Inverting Buck Boost EVM User Guide

ABSTRACT

The TPS6291xEVM-161 (BSR161) facilitates the evaluation of the TPS6291x 2-A and 3-A pin-to-pin compatible Low Noise (< 20 μV_{RMS}) and Low Ripple (< 10 μV_{RMS}) buck converters in small 2-mm by 2-mm QFN packages when used in an inverting buck-boost (IBB) topology. The BSR161-001 uses the 3-A TPS62913 to output a -5-V output voltage from input voltages between 3 V and 11.5 V. Due to its extremely low noise, the TPS6291x is a high-efficiency alternative to low-dropout (LDO) linear regulators in noise-sensitive circuits that need a negative output voltage such as optical modules for telecom infrastructure, instrumentation and operational amplifiers for medical, test and measurement, and aerospace and defense applications.

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Trademarks

1 Introduction

The TPS6291x family of devices are Low Noise, Low Ripple, synchronous, step-down converters in a small 2- × 2- × 1-mm QFN package. Two different devices in this family support 2 A or 3 A of output current. Almost any ordinary buck regulator can be converted into an IBB with a few simple changes in the input and output connections. The TPS6291x family is unique as it incorporates both a low noise filter cap, as well as integrated ferrite bead compensation. The ferrite bead configuration is critical to achieve low ripple and stability of the output voltage across the full load current range. This application report details the usage of the TPS6291x conversion from a buck to an IBB, the operation of the converter and things that you need to consider to make your power supply application a success.

1.1 Performance Specification

Table 1-1 provides a summary of the TPS6291xEVM-161 performance specifications.

Table 1-1. TPS62913EVM-161 Performance Specification Summary

Specification	Test Conditions	MIN	TYP	MAX	Unit
Input Voltage	JP2 open or across 1 MHz and S-CONF	3	5	12	V
Output Voltage Setpoint			-5		V
Output Current	At VIN = 3V, and higher for higher VIN per Figure 1-1	0		0.8	A
S-CONF (R4) Setting	1 MHz with SYNC available, no spread spectrum, output discharge enabled				

1.2 EVM Features and Modifications

The printed-circuit board (PCB) for this EVM is designed to accommodate some modifications by the user. Additional output capacitors can be added. The output voltage can be adjusted using feedback resistors, the soft start time and low frequency noise filtering can be changed, a feed-forward capacitor can be added, and the switching frequency, output discharge setting, and spread spectrum setting can be changed. Finally, the loop response can be measured prior to the ferrite bead with some board modifications. See the device data sheet for details of the various settings.

When making modifications for the output voltage, it will affect the average inductor current and output current. For an IBB, the average inductor current is no longer equal to the average output current because the inductor does not always supply the load current. The inductor only feeds the load during the OFF time, which is 1-D of the switching period. Equation 1 can be used to calculate the average inductor current:

$$I_L = \frac{I_O}{(1-D)} \tag{1}$$

The operating duty cycle for an inverting buck-boost converter can be found with Equation 2.

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN})} \times \frac{1}{\eta} \tag{2}$$

Where η is the efficiency at the operating point.

The efficiency term adjusts the equations in this section for power conversion losses and results in a more accurate maximum output current estimate. The peak to peak inductor ripple current is given by Equation 3.

$$\Delta I_L = \frac{V_{IN} \times D}{(f_{SW} \times L)} \tag{3}$$

Where D is the duty cycle, f_{SW} is the switching frequency in Hz, L is the inductance in H, and V_{IN} is the input voltage with respect to ground.

Equation 4 calculates the maximum inductor current.

$$I_{L,Max} = I_{L,Avg} + \frac{\Delta I_L}{2} \quad (4)$$

For example, for an output voltage of -5 V, an input voltage of 3.3 V, 2.2 µH inductor, and 1MHz switching frequency, the following calculations produce the maximum allowable output current based on the TPS62913 minimum current limit value of 3.7A. The efficiency term is estimated to be 85% as a conservative figure.

$$D = \frac{-5}{-5-3.3} \times \frac{1}{0.85} = 0.709 \quad (5)$$

$$\Delta I_L = \frac{3.3 \times 0.709}{1\,MHz \times 2.2\mu H} = 1.06A \quad (6)$$

Rearranging Equation 7 setting $I_{L,Max}$ equal to the minimum current limit value specified in the data sheet gives:

$$I_{L,Avg} = 3.7 - \frac{1.06}{2} = 3.17 \quad (7)$$

This result is then used in Equation 8 to find the maximum achievable output current:

$$I_{OUT} = 3.17 \times (1 - 0.709) = 922\,mA \quad (8)$$

Figure 1-1 plots the maximum output currents for different output voltages (-1.8 V, -3.6 V, -5 V) and input voltage combinations based on an inductor value of 2.2 uH and a switching frequency of 1MHz.

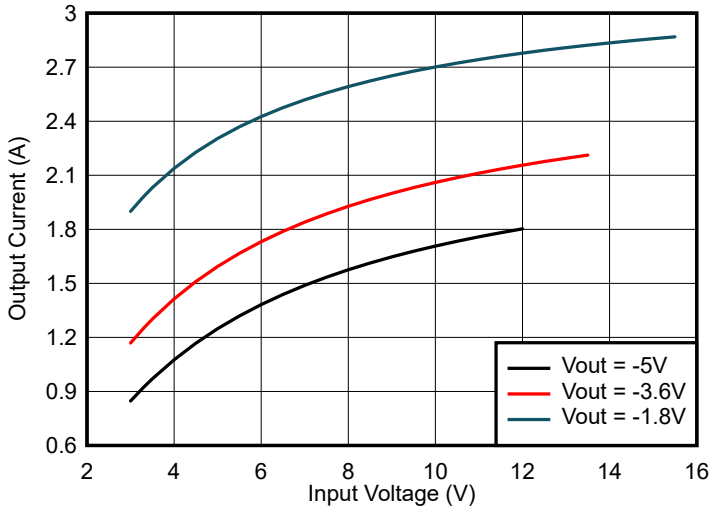


Figure 1-1. Output Current Limitations by Input Voltage and Output Voltage

The input and output voltage for an IBB topology is limited by the recommended operating voltage of the IC, since the input voltage across the IC is from VIN to VOUT rather than from VIN to GND. When looking at the max output current vs VIN, the values are plotted to 17 V + VOUT, so for a -5 V output, the maximum input voltage is 17 V - 5 V, or 12 V.

1.2.1 Input and Output Capacitors

C1 is provided for an additional input capacitor. This capacitor is not required for proper operation but can be used to reduce the input voltage ripple and is included on the EVM since long lead wires are typically used for evaluation. In an actual implementation, this bulk input capacitor is usually not needed.

For an inverting buck-boost configuration, the crossover frequency of the loop must be ~4x or more below the RHP zero. C12 is provided for an additional bulk output capacitor. These capacitors are not required for proper operation but can be used to reduce the crossover frequency. C13 and C18 are provided for high-frequency bypass capacitors.

1.2.2 Enable Level Shifter and Adjustable Threshold Voltage

Because the VOUT is the IC ground in this topology, the EN pin must be referenced to VOUT instead of the ground. In a buck configuration, the specified typical threshold voltage for the enable pin for the TPS6291x is 1.0 V (high) and 0.9 V (low). In the IBB configuration, the VOUT voltage is the reference, so the high threshold is 1.0 V + VOUT and the low threshold is 0.9 V + VOUT. For example, with VOUT = -5 V, then VEN is considered high for voltages above -4 V and low for voltages below -4.1 V. This behavior can cause difficulties for enabling or disabling the part since most applications will not have negative voltages to enable and disable the part. The solution is a logic level shifter, which is implemented on the EVM.

The positive signal that would normally drive the EN signal is not directly connected to the EN/SYNC pin of the TPS6291x. Instead, the signal is tied to the gate of Q1A by using J2. When Q1A is off (J2 jumper installed between EN and GND), Q1B sees 0V across its VGS, and also remains off. In this state, the EN pin sees VOUT, which is below the low level threshold and disables the device.

When the J2 jumper is installed between EN and VIN, this provides enough positive voltage to turn Q1A on (minimum VGS as specified in the MOSFET data sheet), the gate of Q1B is pulled low through Q1A. This drives the VGS of Q1B negative and turns Q1B on. As a consequence, VIN ties to EN through Q2 and the EN/SYNC pin is above the high level threshold, causing the device to turn on. Ensure that the VGD of Q1B remains within the MOSFET ratings during both the enabled and disabled states, or the MOSFETs can be damaged. R2 is an active discharge to accelerate the return to 0V when the J2 jumper is removed.

R3 and R4 can be modified to set a user-selectable input voltage at which the IC turns on.

Power Good Level Shifter

The TPS6291x has a power good (PG) function to indicate when the output voltage has reached the proper level. The PG pin is an open-drain output that requires a pull-up resistor. Because the VOUT is the IC ground in an IBB configuration, the PG pin is referenced to VOUT instead of ground, which means that the device pulls PG to VOUT when it is low. This can cause difficulties in systems that are not able to withstand negative voltages on the PG detection circuit. A level shifter circuit similar to the EN/SYNC implementation is used.

When using the PG function, a voltage (VCC) must be applied on J6. This voltage must not be driven higher than 18V + VOUT. So for a -5 V output, VCC must be less than 12 V.

A 10K resistor pull-up is connected to the PG pin of the device through Q2A. When the PG pin output is low, Q2A is low, causing Q2B to see VCC, which causes the SYS_PG signal to be pulled to GND. This can be seen on pin 1 of J7.

When the PG pin output is high, Q2A is high, causing Q2B to see VOUT, which causes the SYS_PG signal to be pulled to VCC.

1.2.3 NR/SS Capacitor

C5 sets the soft start time and the low frequency noise filtering. This capacitor can be changed to set other soft start times and noise filtering levels. See the TPS62913 data sheet for details.

1.2.4 Feedforward Capacitor

C6 is provided as a feedforward capacitor (C_{FF}). Installing this capacitor can reduce the low-frequency noise, especially for higher output voltages.

1.2.5 S-CONF Resistor

R1 selects the switching frequency when no jumper is installed in J1. R1 selects the settings for spread spectrum, output discharge, and clock synchronization settings. This resistor can be changed or a jumper can be used with J1 to select the VIN (2.2 MHz) or GND (1 MHz) settings. See the TPS62913 data sheet for details.

1.2.6 Loop Response Measurement

The loop response can be measured with simple changes to the circuitry. First, install a 49.9-Ω resistor across R7's pads on the back of the PCB and install a 0-Ω resistor across R8's pads on the back of the PCB. The pads are spaced to allow installation of a 0603-sized resistors. Second, cut the trace on the bottom layer below the added 49.9-Ω resistor. Figure 1-2 shows these changes. Third, cut the short section of trace on the top layer between the via on pin 3 and C7. Figure 1-3 shows this change. Lastly, replace the ferrite bead (FB1) with a

0-Ω resistor. The second LC filter must be removed to break the complete feedback loop and measure the loop response. With these changes, an AC signal (10-mV, peak-to-peak amplitude recommended) can be injected into the control loop across the added 49.9-Ω resistor. Figure 3-6 shows the results of this test.

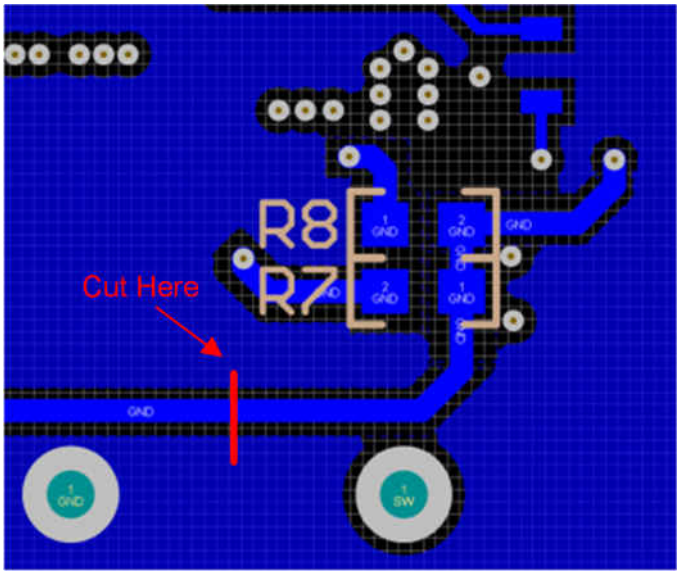


Figure 1-2. Loop Response Measurement Modification (Bottom Layer)

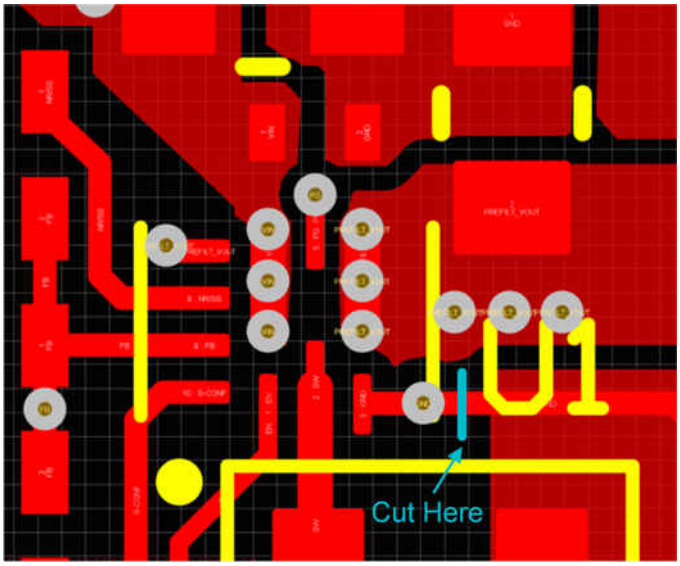


Figure 1-3. Loop Response Measurement Modification (Top Layer)

1.2.7 Single LC Filter Operation

For applications which do not require the lowest output voltage ripple, the TPS6291x can be operated without the second LC filter. To operate with a single LC filter, replace FB1 with a 0-Ω resistor. The capacitors past the ferrite bead may be removed to reduce the amount of output capacitance, but must be enough to keep the Fco four times below the RHPZ.

2 Setup

This section describes how to properly use the EVM.

2.1 Input/Output Connector Descriptions

J3, Pin 1 and 2 – V_{IN}	Positive input connection from the input supply for the EVM.
J3, Pin 3 and 4 – S+/S-	Input voltage sense connections. Measure the input voltage at this point.
J3, Pin 5 and 6 – GND	Return connection from the input supply for the EVM.
J8, Pin 1 and 2 – GND	Output return connection
J8, Pin 3 and 4 – S+/S-	Output voltage sense connections. Measure the output voltage at this point.
J8, Pin 5 and 6 – VOUT_FILT	Filtered output connection.
J7 – SYS_PG/GND	The SYS_PG output is on pin 1 of this header with a convenient ground on pin 2.
J6 - VCC/GND	The VCC source connection for the PG pull-up with a convenient ground on pin 2. This externally supplied voltage should be less than 18 V + VOUT.
J4 – PREFILT_V_{OUT} Ripple Measurement	Use this SMA connector to measure the output voltage ripple before the second LC filter.
J5 – V_{OUT}_FILT Ripple Measurement	Use this SMA connector to measure the output voltage ripple after the second LC filter.
J2 – EN	EN pin input jumper. Place the supplied jumper across VIN and EN to turn on the IC. Place the jumper across GND and EN to turn off the IC. The synchronization function is not supported in this IBB Configuration.
J1 – S-CONF	S-CONF pin input jumper. Place the supplied jumper across 2.2 MHz and S-CONF to operate the IC with a 2.2-MHz switching frequency without spread spectrum or output discharge. Place the jumper across 1 MHz and S-CONF to operate the IC with a 1-MHz switching frequency without spread spectrum or output discharge. Remove the jumper to operate the IC with the S-CONF settings set by R1.

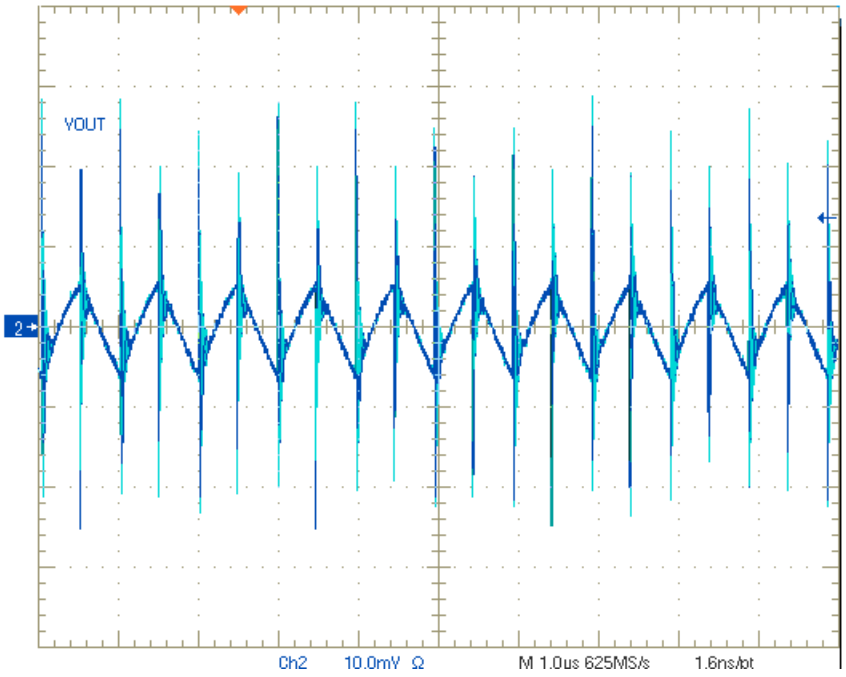
Note

- Set the J1 jumper position before enabling the IC. Changing J1 after enabling the IC has no effect.
- When using the 2.2-MHz setting, ensure that the input voltage and output voltage do not violate the minimum on-time in the device data sheet.

2.2 Ripple Measurement

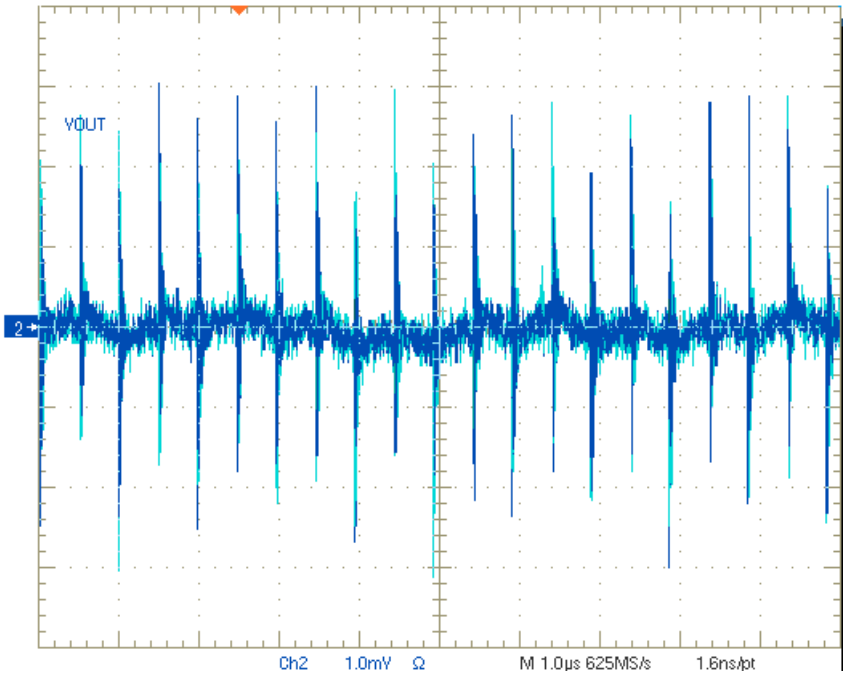
The extremely low noise and low ripple levels of the TPS6291x necessitate a low-noise test setup for accurately measuring the output voltage ripple. The SMA connectors, J4 and J5, should be used to measure the output voltage ripple, before and after the second LC filter. Do not use a normal 10x oscilloscope probe with a high-impedance termination to the oscilloscope. Instead, connect the SMA connector directly to the oscilloscope with a coaxial (coax) cable through a DC blocker. A DC blocker enables the use of the smallest V/div setting on the oscilloscope to view the ripple. To prevent noise pickup and block reflections on the coax cable, the oscilloscope should be set to full bandwidth (BW) and DC coupling with a 50-Ω termination.

Figure 2-1 and Figure 2-2 show the correct measurement settings and output voltage ripple result. The measurement at J4 is prior to the ferrite bead filter, and the measurement at J5 is after the ferrite bead filter.



V_{IN} = 5 V, V_{OUT} = -5 V, I_{OUT} = 1000 mA, FSW = 1 MHz, Full BW, DC Coupling, 50-Ω Termination With DC Blocker

Figure 2-1. Output Voltage Ripple, Measured at J4 (First LC Filter)



V_{IN} = 5 V, V_{OUT} = -5 V, I_{OUT} = 1000 mA, FSW = 1 MHz, Full BW, DC Coupling, 50-Ω Termination With DC Blocker

Figure 2-2. Output Voltage Ripple, Measured at J5 (After Ferrite Bead)

3 Test Results

The TPS62913-IBB-EVM is set to -5 V output, but can be easily modified through the feedback resistors for other output voltages. The efficiency curves below show the performance at 3.3 V, 5 V, and 11.5 V input voltages.

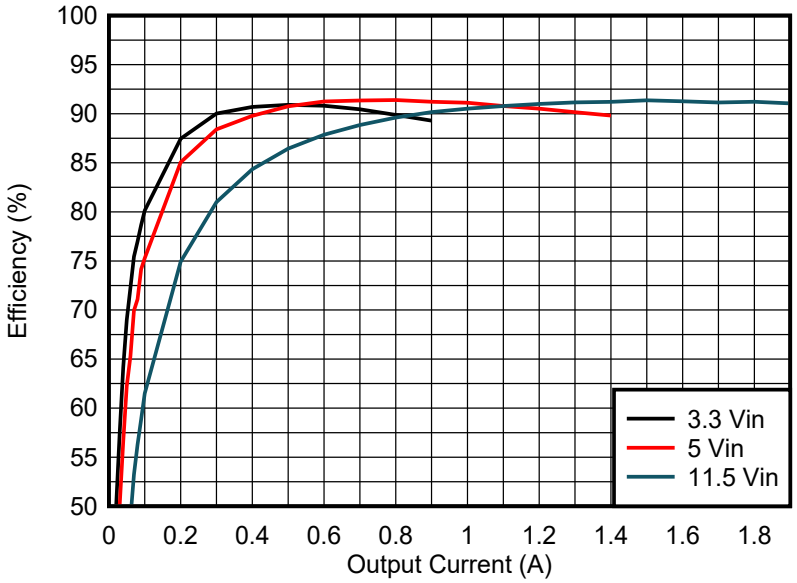


Figure 3-1. Efficiency for -5 V Output with 1MHz f_{SW}

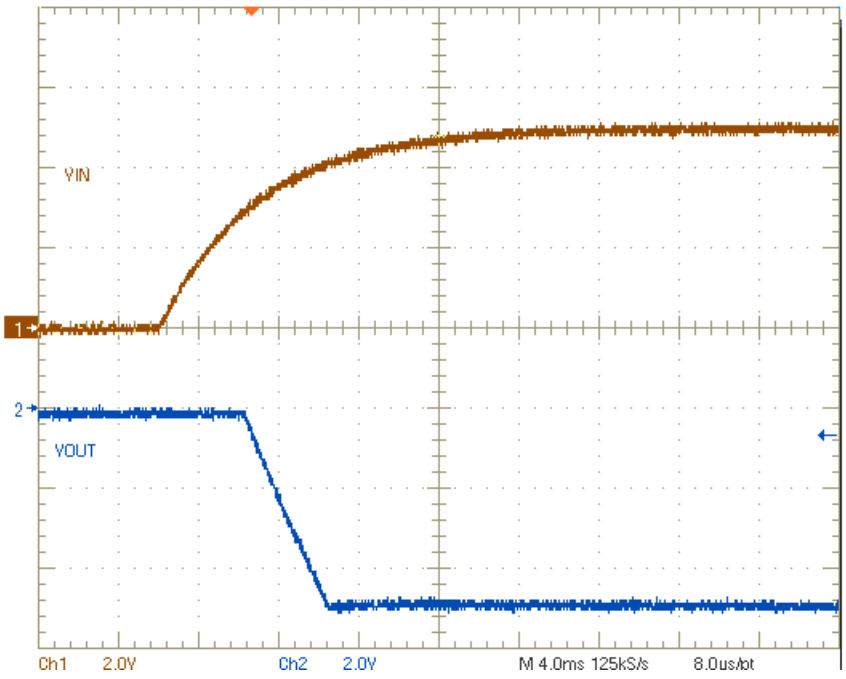


Figure 3-2. Startup with No Load

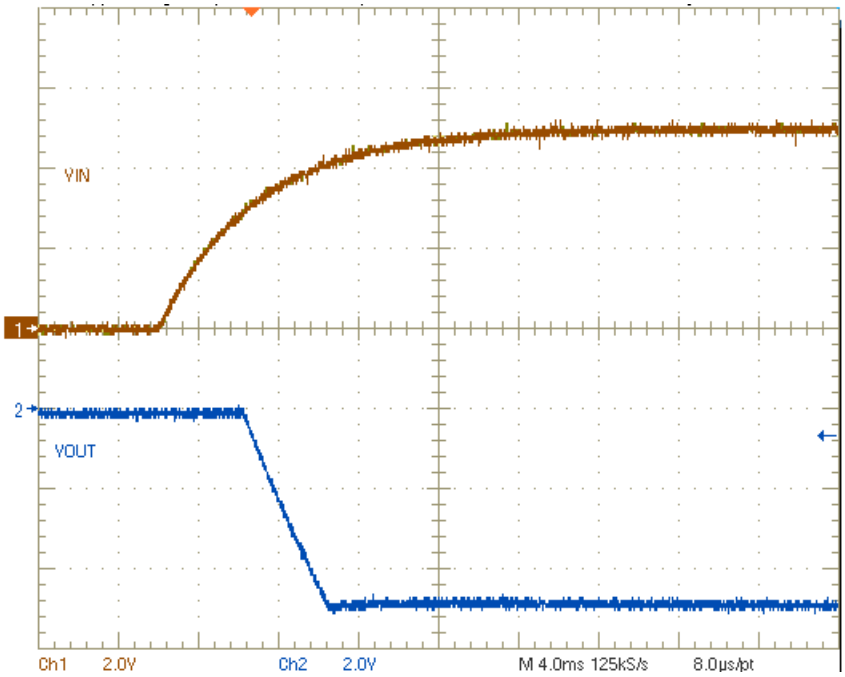


Figure 3-3. Startup with 1A Load

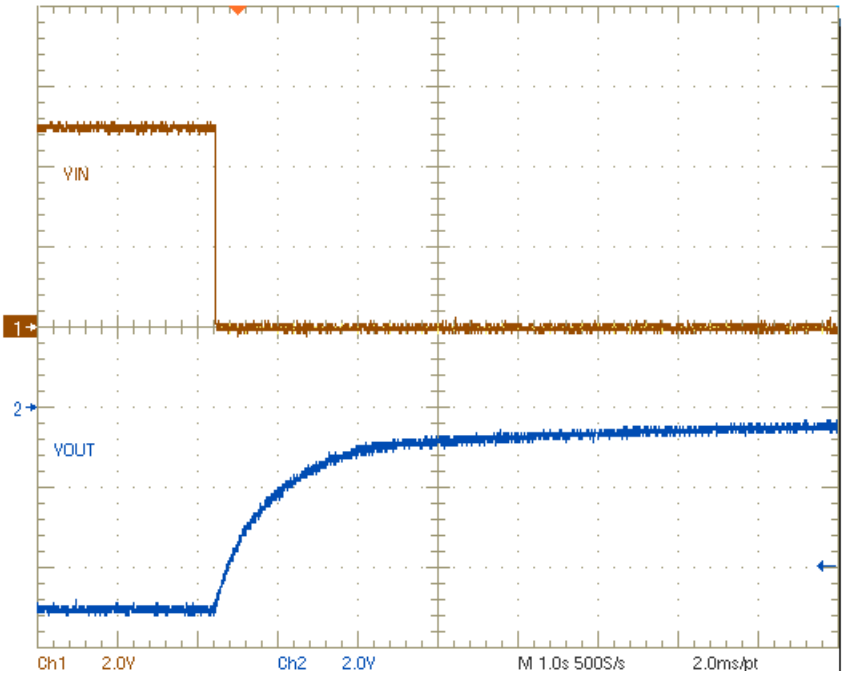


Figure 3-4. Shutdown with No Load

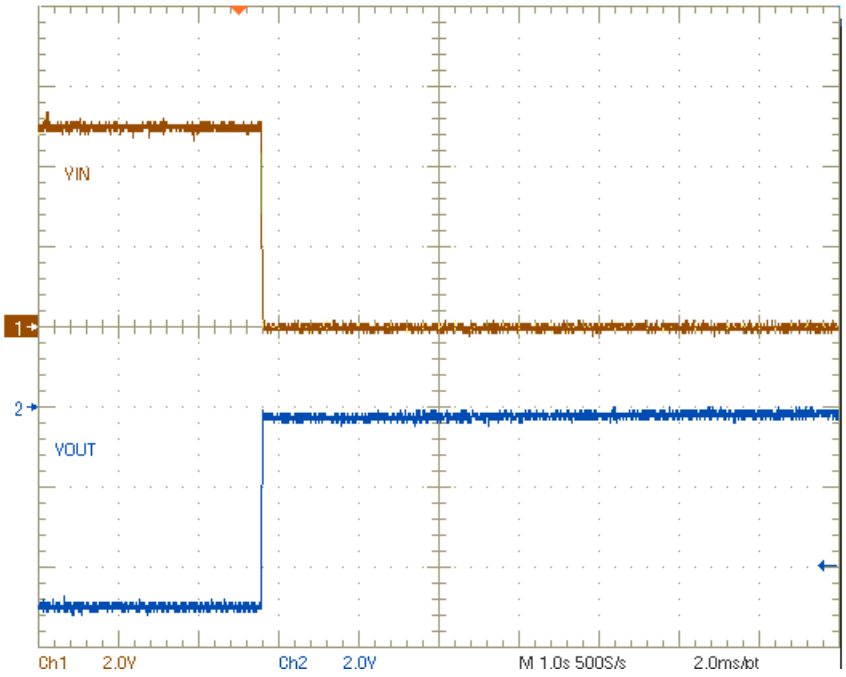


Figure 3-5. Shutdown with 1A Load

Figure 3-6 shows the loop response measurement.

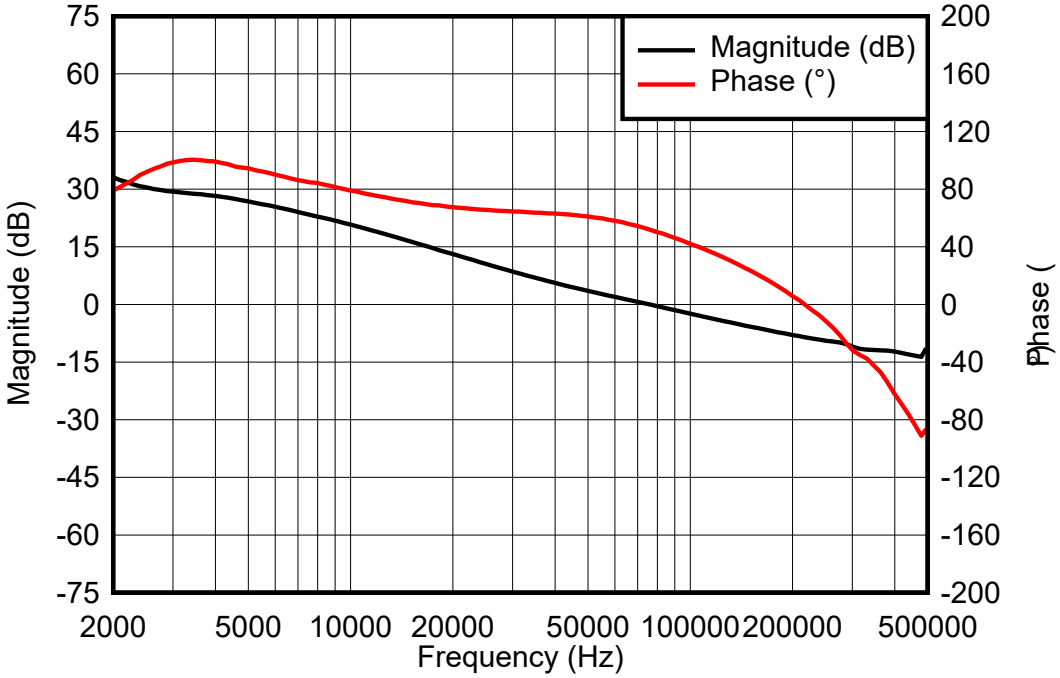


Figure 3-6. Loop Response Measurement (V_{IN} = 5 V, V_{OUT} = -5 V, I_{OUT} = 1000 mA, Ferrite Bead Removed)

4 Board Layout

This section provides the EVM board layout and illustrations in Figure 4-1 through Figure 4-6. The Gerbers are available on the EVM product page.

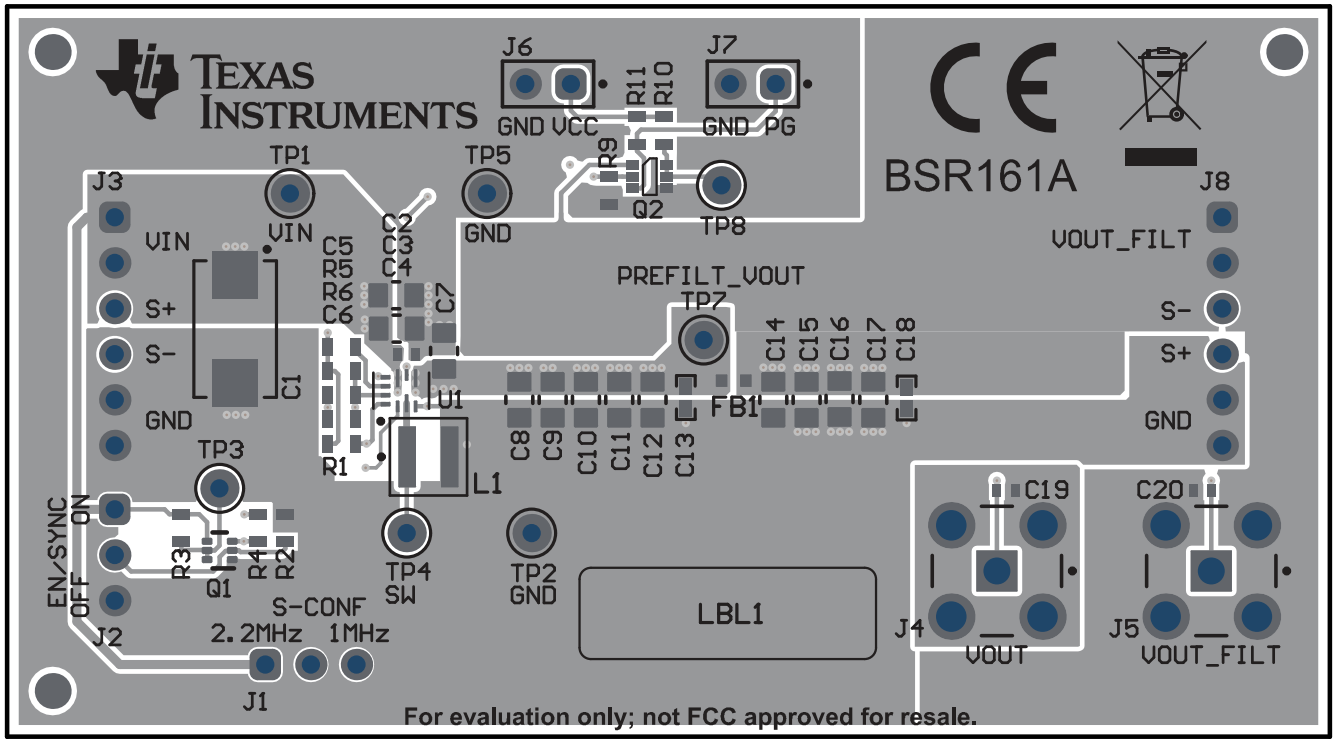


Figure 4-1. Top Assembly

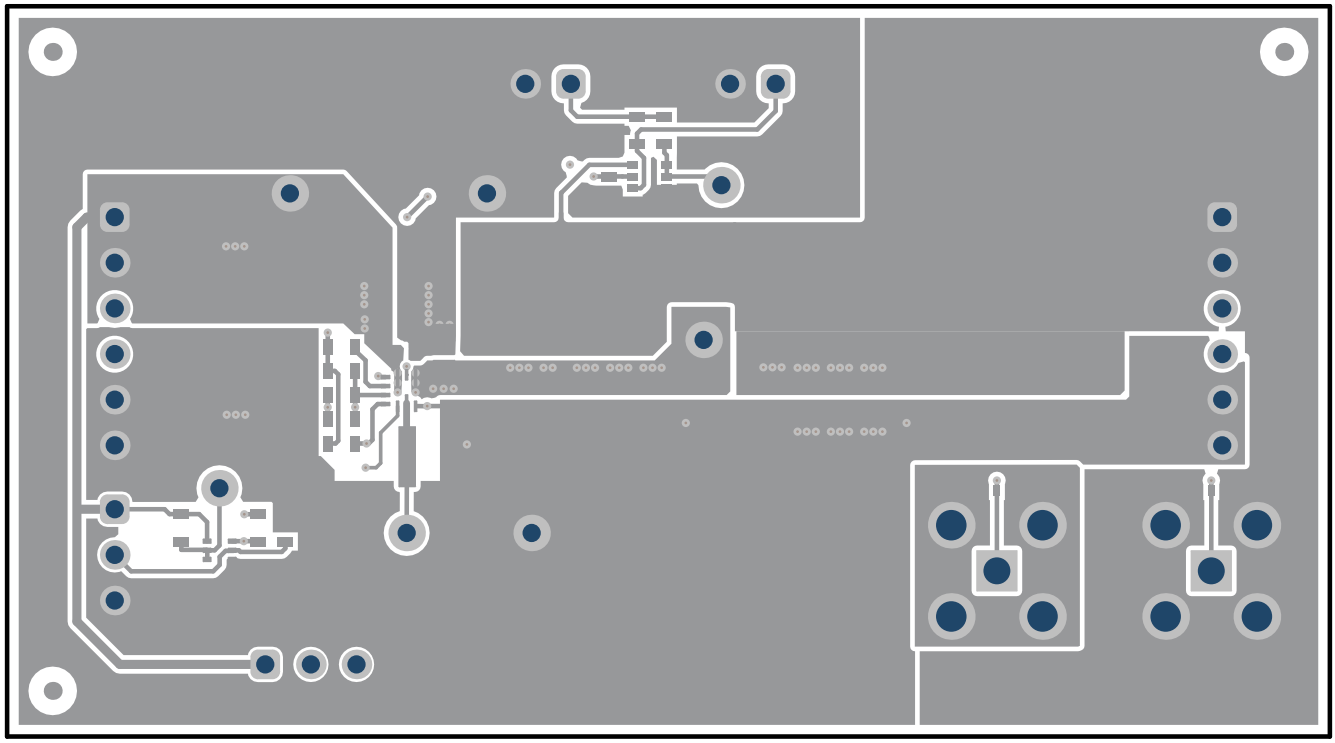


Figure 4-2. Top Layer

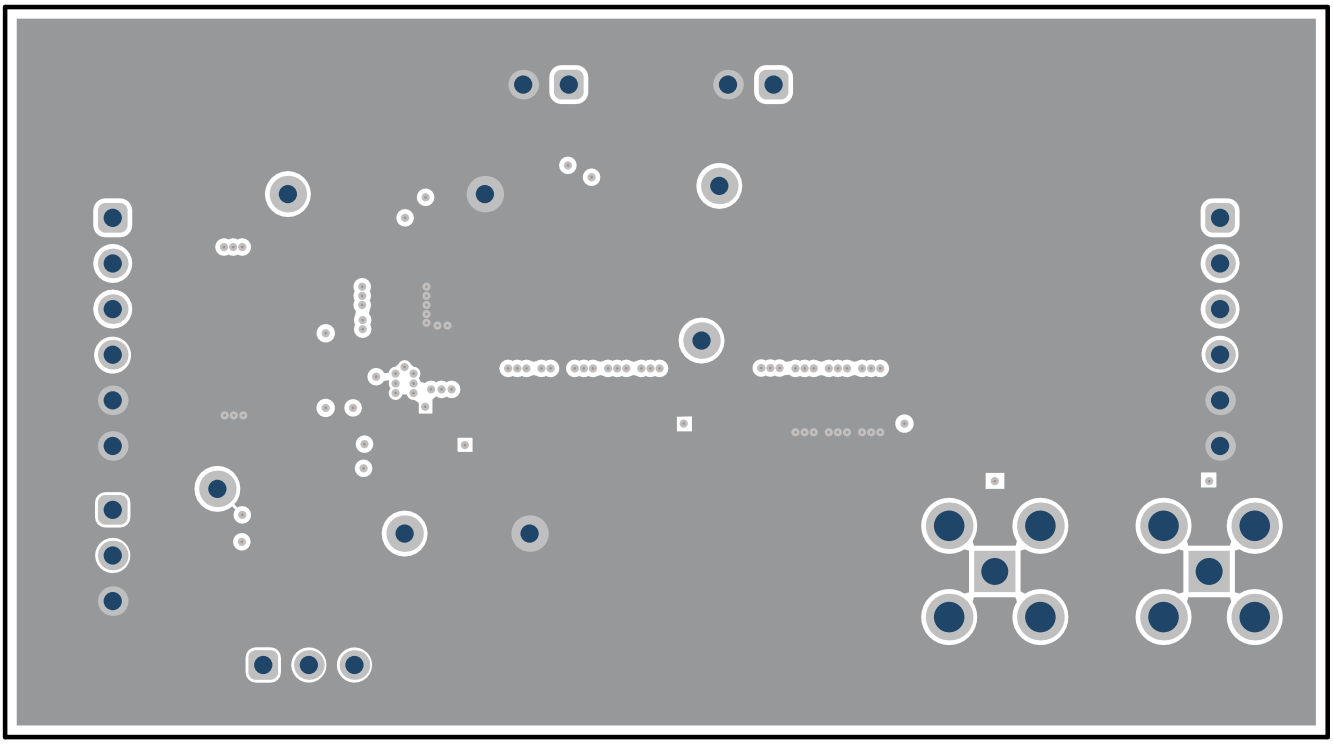


Figure 4-3. Internal Layer 1

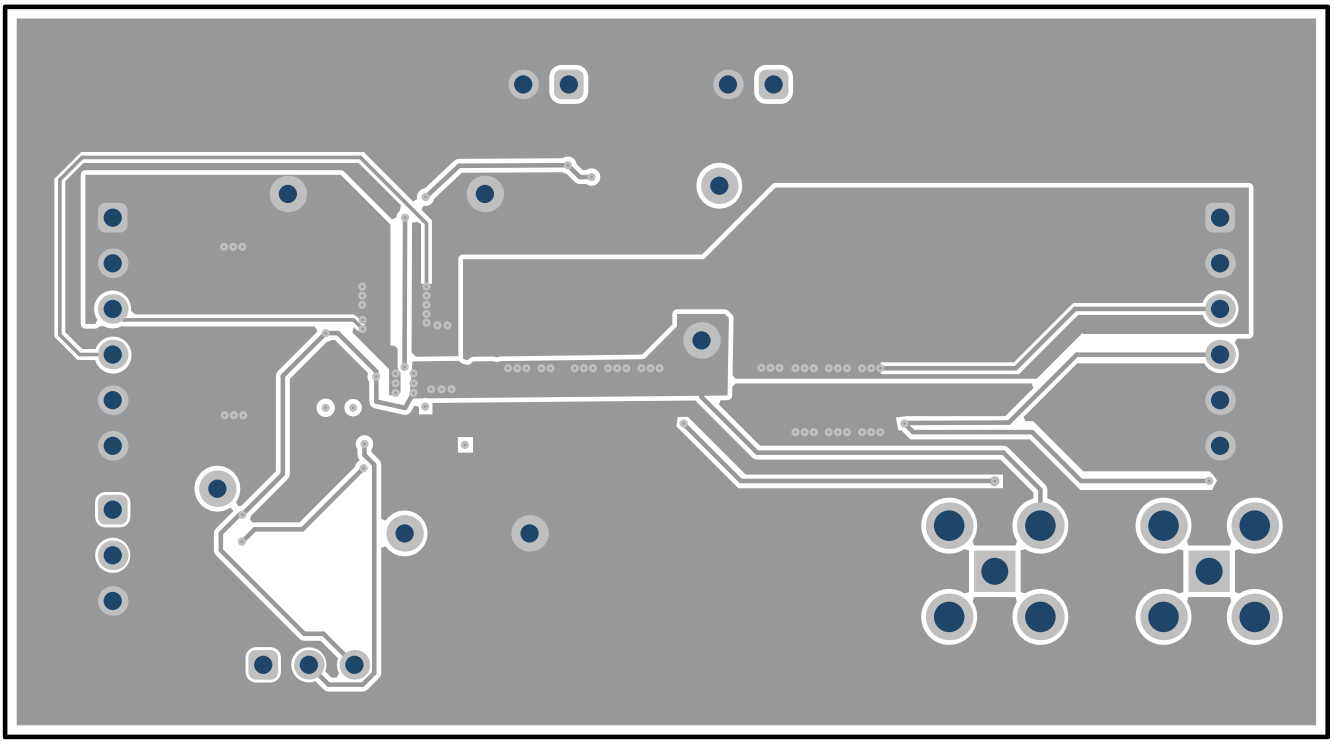


Figure 4-4. Internal Layer 2

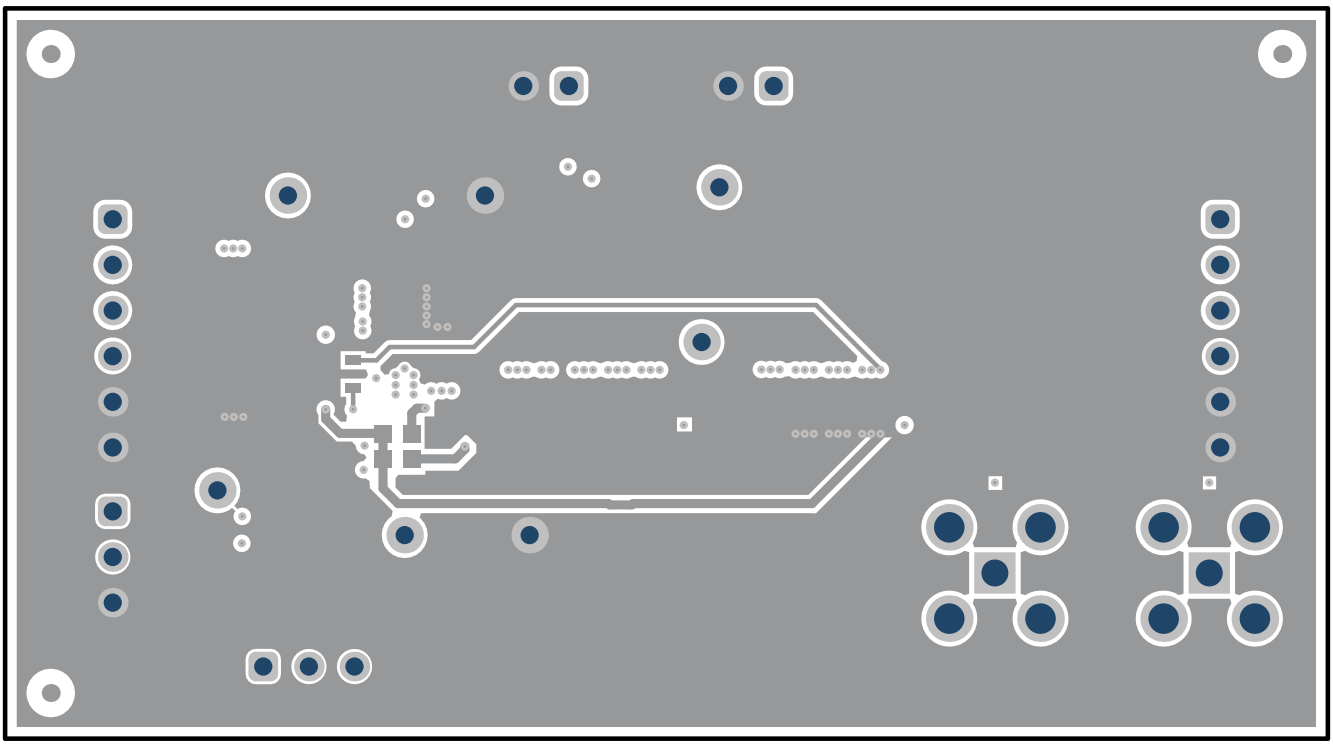


Figure 4-5. Bottom Layer

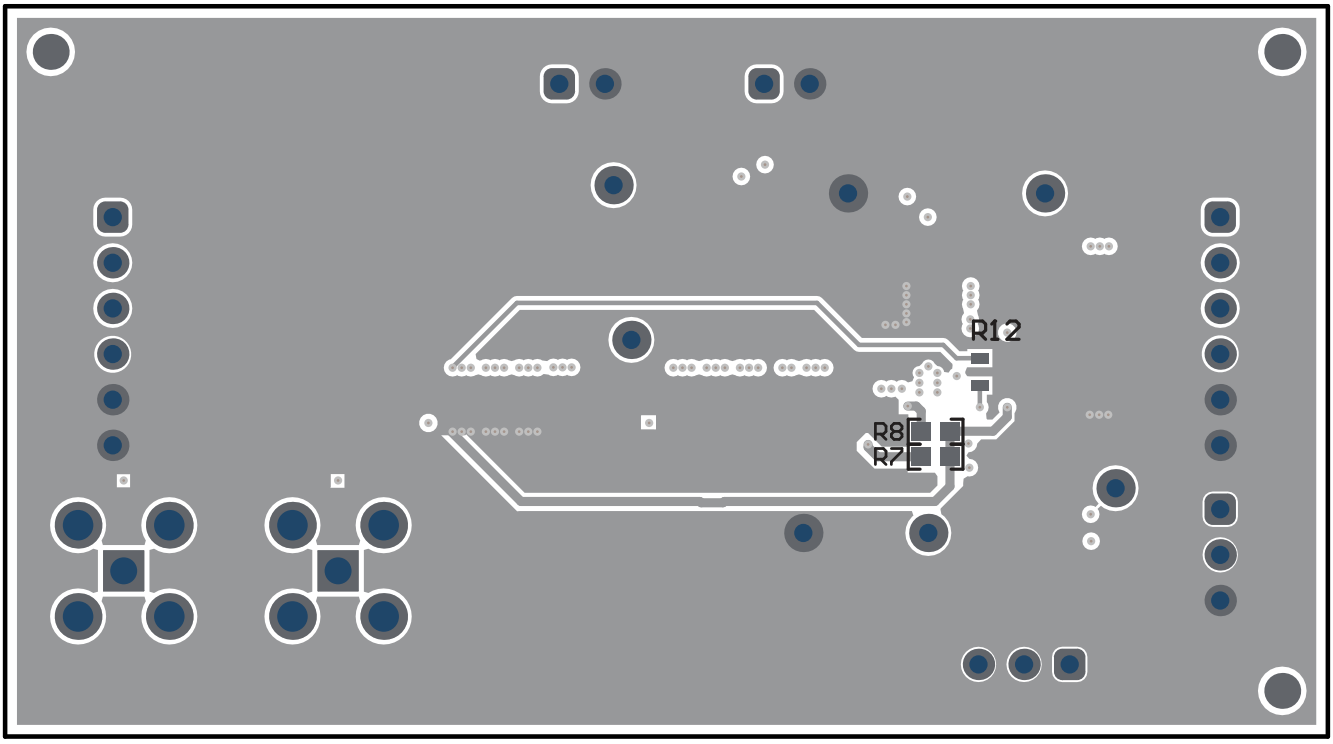


Figure 4-6. Bottom Layer (Mirrored)

5 Schematic and Bill of Materials

This section provides the EVM schematic and bill of materials (BOM).

5.1 Schematic

Figure 5-1 illustrates the EVM schematic.

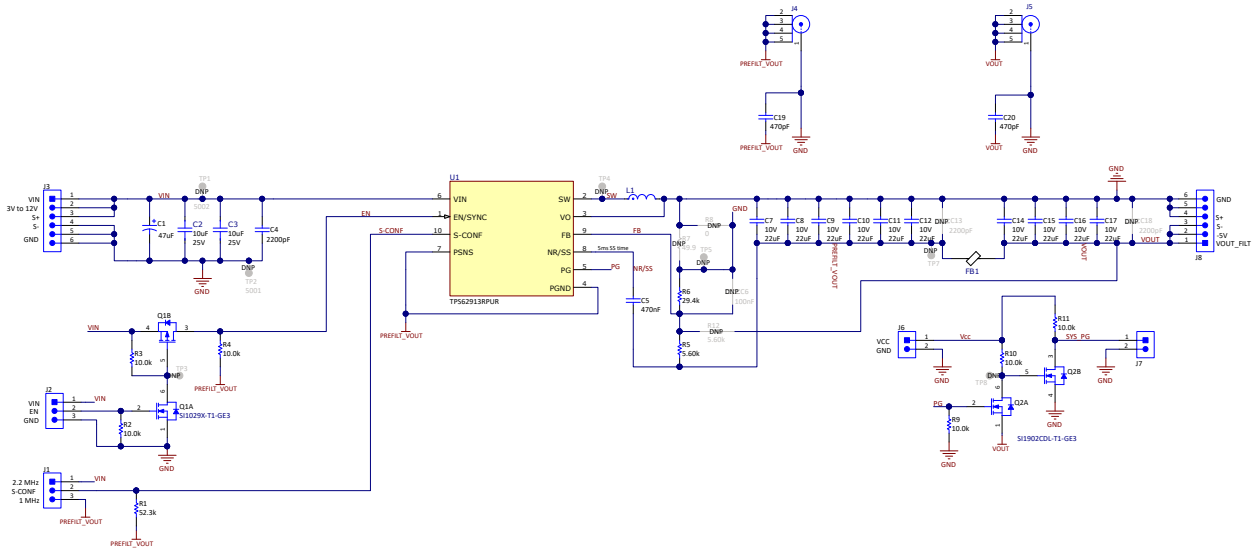


Figure 5-1. TPS62913-IBB-EVM Schematic

6 Bill of Materials

Table 6-1 lists the BOM for this EVM.

Table 6-1. TPS62913-IBB-EVM Bill of Materials

-001	Reference Designator	Description	Package	Part Number	Manufacturer
1	C4	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R	0402	GRM155R71H222KA01D	muRata
2	C2, C3	CAP, CERM, 10µF, 25 V, +/- 10%, X7S	0805	C2012X7S1E106K125AC	TDK
10	C7, C8, C9, C10, C11, C12, C14, C15, C16, C17	CAP, CERM, 22 µF, 10 V, +/- 20%, X7S	0805	C2012X7S1A226M125AC	TDK
1	C5	CAP, CERM, 0.47 µF, 25 V, +/- 10%, X7R	0603	C1608X7R1E474K080AE	TDK
1	C1	CAP, TA, 47 µF, 35 V, +/- 10%, 0.3 Ω	7343-43	T495X476K035ATE300	Kemet
2	C19, C20	CAP, CERM, 470 pF, 50 V, +/- 5%, C0G/NP0	0402	GRM1555C1H471JA01D	muRata
1	FB1	Ferrite bead, 8.5-Ω at 100 MHz, 4mΩ DCR, 8A	0603	BLE18PS080SN1	muRata
1	L1	Inductor Power Shielded Wirewound 2.2µH 20% Composite 8.7A 19.5mΩ DCR	4 x 4 mm	XGL4020-222MEC	Coilcraft
1	R1	RES, 52.3 kΩ, 1%, 0.1 W	0603	Std	Std
1	R5	RES, 5.60 kΩ, 1%, 0.1 W	0603	Std	Std
1	R2, R3, R4, R9, R10, R11	RES, 10.0 kΩ, 1%, 0.1 W	0603	Std	Std
1	R6	RES, 29.4 kΩ, 1%, 0.1 W	0603	Std	Std
1	U1	3 V to 17 V, 3 A Low Noise (20 μV_{RMS}) and Low Ripple (200 μV_{PP}) buck converter	2 x 2 mm	TPS62913RPUR	Texas Instruments

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