User's Guide

TPSM416x5 Power Module Evaluation Module User's Guide

ABSTRACT

The TPSM41625 and TPSM41615 evaluation module (EVM) is designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the TPSM416x5 power module. This guide provides information on the correct usage of the EVM and an explanation of the numerous test points on the board.

Note

This EVM user's guide applies to both devices. The only difference between the two EVMs are the U1 IC and the silk screen labeling.

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1 Description

This EVM features the TPSM41625 and TPSM41615 synchronous buck power module configured for operation with a 4-V to 16-V input voltage range. The output voltage can be set to several popular values by using configuration jumpers. Similarly, the switching frequency can be set to one of five values with a jumper. The full output current rating of the device can be supplied by the EVM. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Control test points and component footprints are provided for use of the EN, POWER GOOD, and SYNC features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

2 Getting Started

Figure 2-1 highlights the user interface items associated with the EVM. The PVIN and PGND terminal blocks (TB1 and TB2) are used for connection to the host input supply and the VOUT and PGND terminal blocks (TB3 and TB4) are used for connection to the load. These terminal blocks can accept up to 16-AWG wire.

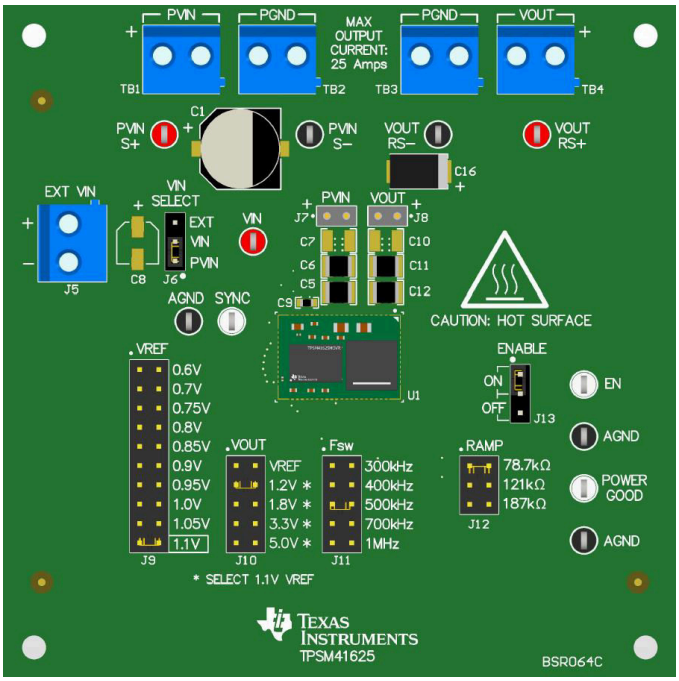

Figure 2-1. EVM User Interface

The PVIN S+ and PVIN S- input voltage test points as well as the RS+ and RS- output voltage test points, located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure PVIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.

The PVIN Scope (J7) and VOUT Scope (J8) sockets can be used to monitor PVIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low-inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. The scope probe tip should be inserted into the socket marked with a "+" sign, and the scope ground lead should be inserted into the other socket.

The control test points located around the device are made available to test the features of the device. Refer to the *Test Point Description* section for more information on the individual control test points. Other features, such as UVLO (R2, R3), ILIM (R23), SS (R24) and MODE (R25) can be altered by manually adding or changing the value on the associated footprints for each component located on the bottom-side of the EVM.

The VREF jumper (J9), VOUT jumper (J10), FSW jumper (J11), and the RAMP jumper (J12) are provided for selecting the internal reference voltage, switching frequency, desired output voltage, and appropriate RAMP setting. Before applying power to the EVM, make sure that the jumpers are present and properly positioned for the intended output voltage. Ensure to set the internal reference voltage prior to selecting the desired output voltage (selecting the highest reference voltage will result in the most accurate output voltage set point). Refer to Table 2-1 for the recommended jumper settings.

Table 2-1. PVIN = 5 V Recommended Jumper Settings

OUTPUT VOLTAGE	VREF SELECT (J9)	VOUT SELECT (J10)	F_{SW} SELECT (J11)(1)	RAMP (J12)
0.6 V - 0.75 V	0.6 V - 0.75 V	V_{REF}	500 kHz - 700 kHz	187 kΩ
0.8 V - 0.95 V	0.8 V - 0.95 V	V_{REF}	500 kHz - 1 MHz	78.7 kΩ
1 V - 1.1 V	1 - 1.1 V	V_{REF}	400 kHz - 1 MHz	187 kΩ
1.2 V	1.1 V	1.2 V	400 kHz - 1 MHz	187 kΩ
1.8 V	1.1 V	1.8 V	400 kHz - 1 MHz	187 kΩ
3.3 V	1.1 V	3.3 V	400 kHz - 1 MHz	78.7 kΩ

Table 2-2. PVIN = 12 V Recommended Jumper Settings

OUTPUT VOLTAGE	VREF SELECT (J9)	VOUT SELECT (J10)	F_{SW} SELECT (J11)(1)	RAMP (J12)
0.6 V - 0.95 V	0.6 V - 0.95 V	V_{REF}	500 kHz - 700 kHz	78.7 kΩ
1 V - 1.1 V	1 - 1.1 V	V_{REF}	700 kHz - 1 MHz	78.7 kΩ
1.2 V	1.1 V	1.2 V	500 kHz - 1 MHz	121 kΩ
1.8 V	1.1 V	1.8 V	500 kHz - 700 kHz	187 kΩ
3.3 V	1.1 V	3.3 V	700 kHz - 1 MHz	187 kΩ
5.0 V	1.1 V	5.0 V	700 kHz - 1 MHz	187 kΩ

(1) Refer to the product data sheet for more information on the recommended switching frequency.

For example, if an output voltage of 1.8 V is desired and is supplied by a 12-V input, then a proper configuration is as follows:

1. Set VREF (J9) as 1.1 V.
2. Set VOUT (J10) as 1.8 V.
3. Select FSW (J11).
4. Set RAMP (J12) as 187 kΩ.

Another example, if an output voltage of 1.0 V is desired and is supplied by a 12-V input, then a proper configuration is as follows:

1. Set VREF (J9) as 1.0 V.
2. Set VOUT (J10) as VREF.
3. Select FSW (J11).
4. Set RAMP (J12) as 78.7 kΩ

3 Test Point Description

Wire-loop test points and two scope probe test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A description of each test point(1) follows:

Table 3-1. Test Point Descriptions

Test Point	Description
PVIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
PVIN S-	Input voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
RS+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
RS-	Output voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
AGND	Analog ground test point.
PGND	Power ground test point.
PVIN Scope (J7)	Input voltage scope monitor. Connect an oscilloscope probe to this set of points to measure input ripple voltage.
VOUT Scope (J8)	Output voltage scope monitor. Connect an oscilloscope probe to this set of points to measure output ripple voltage and transient response.
ENABLE (J13)	Enable test point. This test point can be used to monitor the EN voltage or to connect the EN pin to AGND to disable the device using a jumper wire. Additionally, for ease of use, J13 can be set in the ON position to enable the device or in the OFF position to disable the device.
POWER GOOD	Monitors the power good signal of the device. This is an open drain signal.
SYNC	Frequency synchronization pin. Connect the clock signal to the SYNC and AGND test points when synchronizing to an external clock.

(1) Refer to the product data sheet for absolute maximum ratings associated with above features.

4 Performance Data

Figure 4-1 and Figure 4-2 demonstrate the enable ON/OFF performance of the EVM. See Figure 4-3 through Figure 4-5 for transient response waveforms (5-A, 10-A and 15-A load with a scale of 10 A/uS) associated with the default populated EVM. Figure 4-6 shows the typical output voltage ripple with a 15-A load. Additional output capacitor footprints are available on the EVM if an improved load transient response or output voltage ripple is needed. See the data sheet for more information on the respective devices.

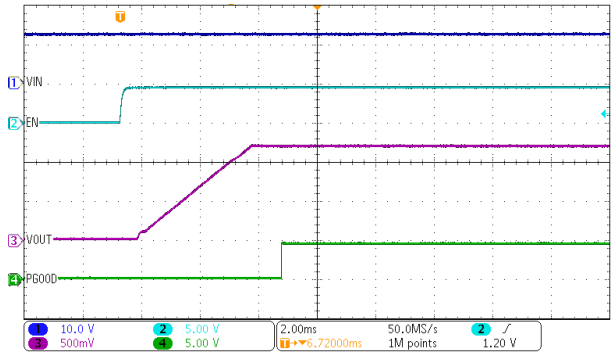

Figure 4-1. ENABLE Start-Up Waveform

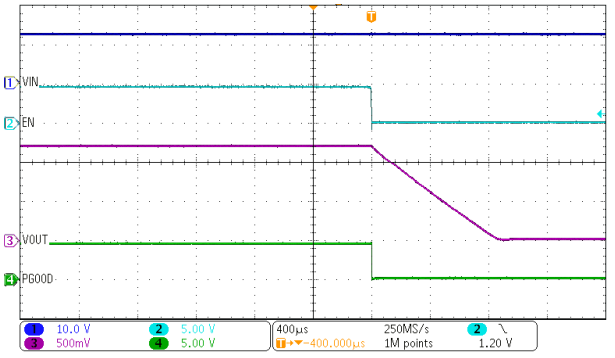

Figure 4-2. ENABLE Shutdown Waveform

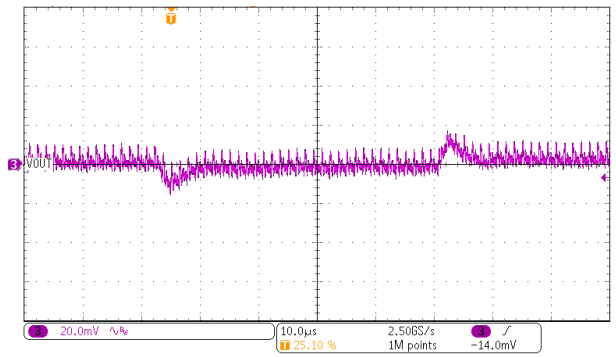

Figure 4-3. 5-A Transient Performance

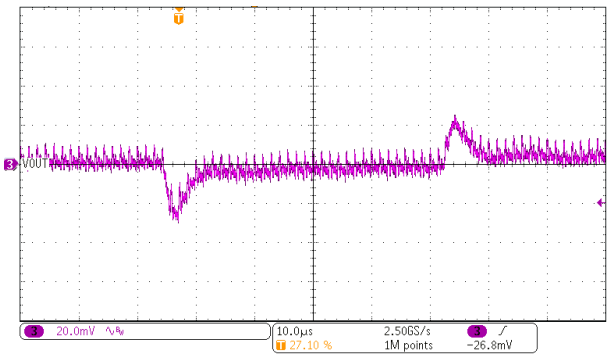

Figure 4-4. 10-A Transient Performance

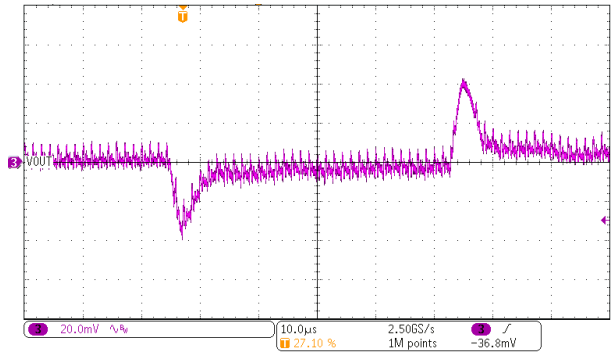

Figure 4-5. 15-A Transient Performance

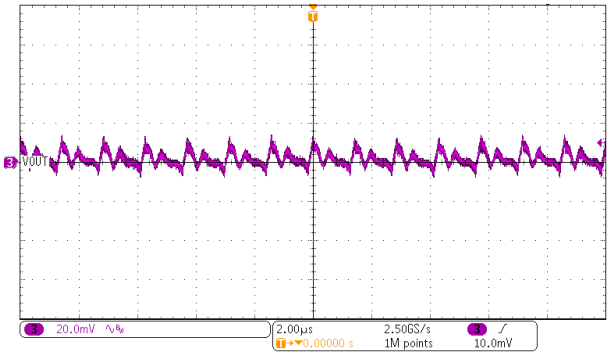

Figure 4-6. 15-A Output Voltage Ripple

5 Schematic

The schematic for both the TPSM41625EVM and TPSM41615EVM are identical with the only difference being the U1 IC. Figure 5-1 shows the TPSM41625 device.

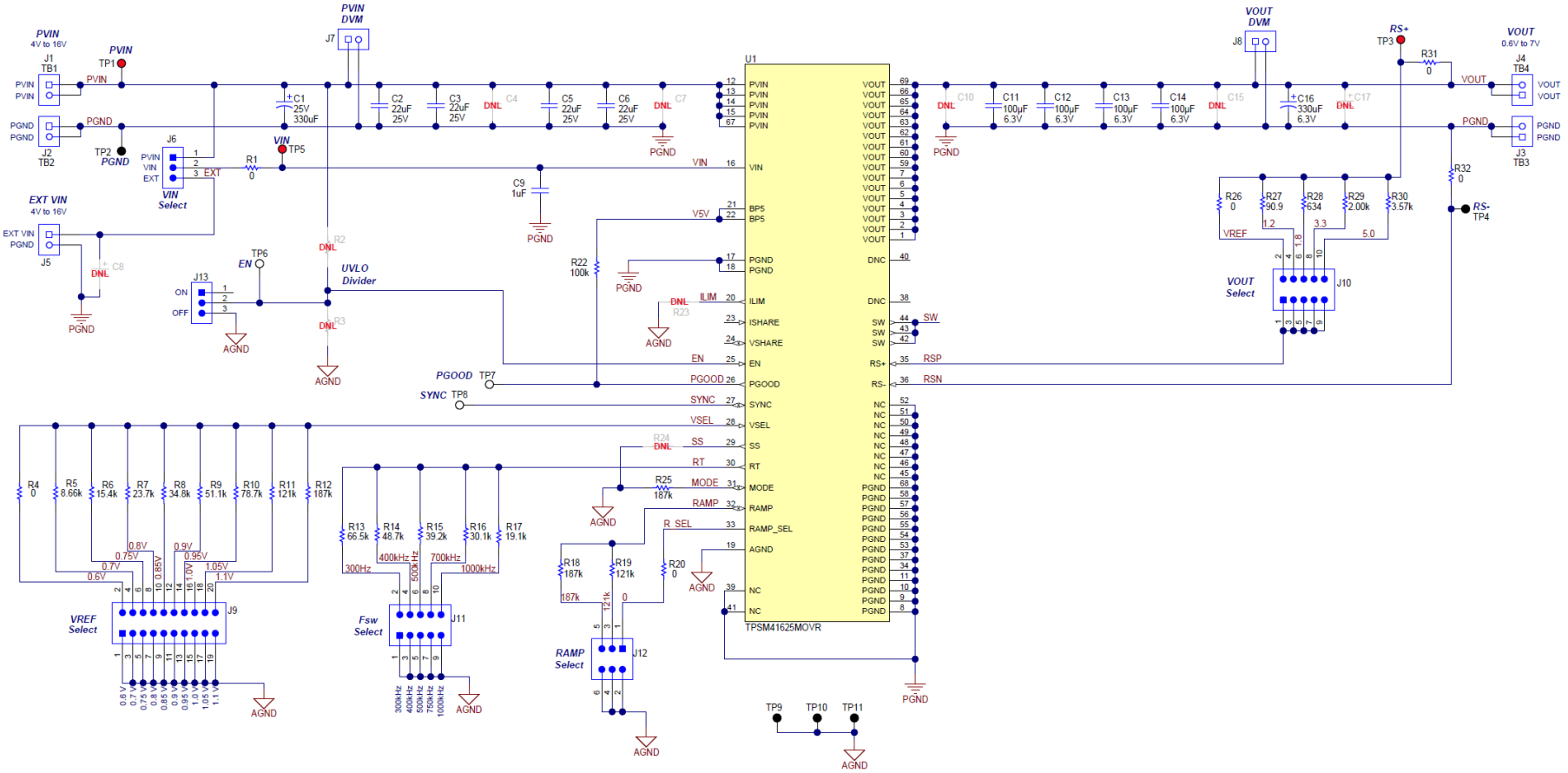

Figure 5-1. TPSM41625EVM Schematic

6 Bill of Materials (BOM)

Table 6-1. EVM Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER
C1	1	300 µF	CAP, AL, 330 µF, 25 V, 0.15 Ω	SMI Radial G	EEE-FC1E331P
C2, C3, C5, C6	4	22 µF	CAP, CERM, 22 µF, 25 V	1210	GRM32ER71E226KE15L
C9	1	1 µF	CAP, CERM, 1 µF, 50 V	0603	UMK107AB7105KA-T
C11, C12, C13, C14	4	100 µF	CAP, CERM, 100 µF, 6.3 V	0603	GRM32EC70J107ME15L
C16	1	330 µF	CAP, Tantalum, Polymer, 330 µF, 6.3 V, 0.01 Ω	2917	6TPE330MAA
J1, J2, J3, J4, J5	5		Terminal Block, 5.08 mm, 2x1	2x1, 5.08 mm	ED120/2DS
J6, J13	2		Header, 100 mil, 3x1	3x1, 100 mil	PEC03SAAN
J7, J8	2		Socket Strip, 2x1, 100 mil	2x1, 100 mil	310-43-102-41-001000
J9	1		Header, 100 mil, 10x2	10x2, 100 mil	TSW-110-07-G-D
J10, J11	2		Header, 100 mil, 5x2	5x2, 100 mil	TSW-105-07-G-D
J12	1		Header, 100 mil, 3x2	3x2, 100 mil	TSW-103-07-G-D
R1, R4, R20, R26, R31, R32	6	0	RES, 0, 5%, 0.1 W	0603	CRCW06030000Z0EA
R5	1	8.66 k	RES, 8.66 k, 1%, 0.1 W	0603	CRCW06038K66FKEA
R6	1	15.4 k	RES, 15.4 k, 1%, 0.1 W	0603	CRCW060315K4FKEA
R7	1	23.7 k	RES, 23.7 k, 1%, 0.1 W	0603	CRCW060323K7FKEA
R8	1	34.8 k	RES, 34.8 k, 1%, 0.1 W	0603	CRCW060334K8FKEA
R9	1	51.1 k	RES, 51.1 k, 1%, 0.1 W	0603	CRCW060351K1FKEA
R10	1	78.7 k	RES, 78.7 k, 1%, 0.1 W	0603	CRCW060378K7FKEA
R11, R19	2	121 k	RES, 121 k, 1%, 0.1 W	0603	CRCW0603121KFKEA
R12, R18, R25	3	187 k	RES, 187 k, 1%, 0.1 W	0603	CRCW0603187KFKEA
R13	1	66.5 k	RES, 66.5 k, 1%, 0.1 W	0603	RC0603FR-0766K5L
R14	1	48.7 k	RES, 48.7 k, 1%, 0.1 W	0603	CRCW060348K7FKEA
R15	1	39.2 k	RES, 39.2 k, 1%, 0.1 W	0603	CRCW060339K2FKEA
R16	1	30.1 k	RES, 30.1 k, 1%, 0.1 W	0603	CRCW060330K1FKEA
R17	1	19.1 k	RES, 19.1 k, 1%, 0.1 W	0603	CRCW060319K1FKEA
R22	1	100 k	RES, 100 k, 1%, 0.1 W	0603	CRCW0603100KFKEA
R27	1	90.9 k	RES, 90.9 k, 1%, 0.1 W	0603	CRCW060390R9FKEA
R28	1	634	RES, 634, 1%, 0.1 W	0603	CRCW0603634RFKEA
R29	1	2.00 k	RES, 2.00 k, 1%, 0.1 W	0603	CRCW06032K00FKEA
R30	1	3.57 k	RES, 3.57 k, 1%, 0.1 W	0603	CRCW06033K57FKEA
TP1, TP3, TP5	3		Test Point, Multipurpose, Red	Testpoint	5010
TP2, TP4, TP9, TP10, TP11	5		Test Point, Multipurpose, Black	Testpoint	5011
TP6, TP7, TP8	3		Test Point, Multipurpose, White	Testpoint	5012

Table 6-1. EVM Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	SIZE	PART NUMBER
U1	1		16-V, 25-A Power Module	MOVR0069A	TPSM41625MOVR
			16-V, 15-A Power Module		TPSM41615MOVR
Not loaded					
C4, C7, C10, C15	0			1210	
C8	0			SMT Radial C	
C17	0			2917	
R2, R3, R23, R24	0			0603	

7 PCB Layout

Figure 7-1 through Figure 7-8 show the PCB layers for both the TPSM41625EVM and TPSM41615EVM.

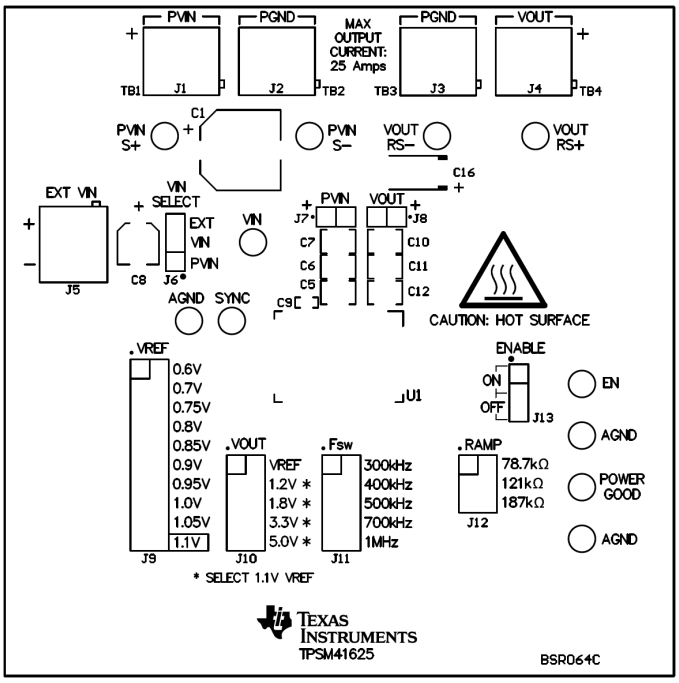

Figure 7-1. Topside Component Layout (Top View)

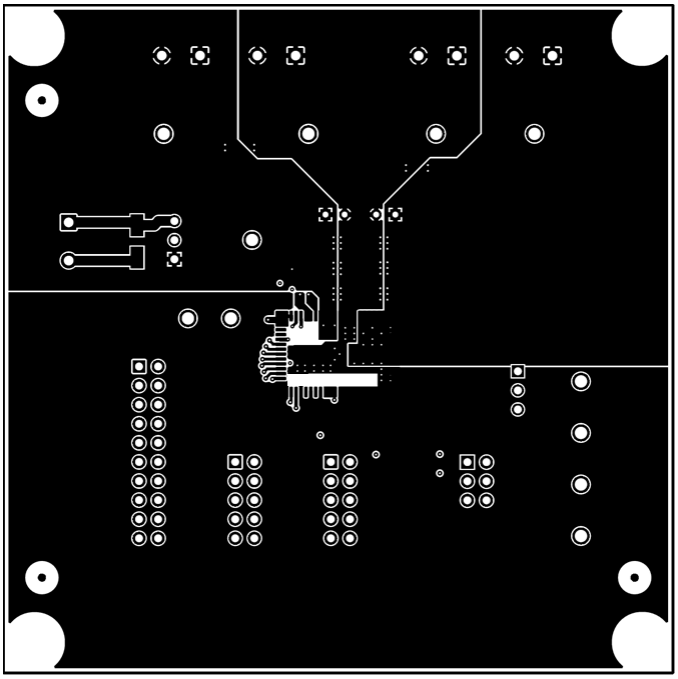

Figure 7-2. Layer 1 (Top View)

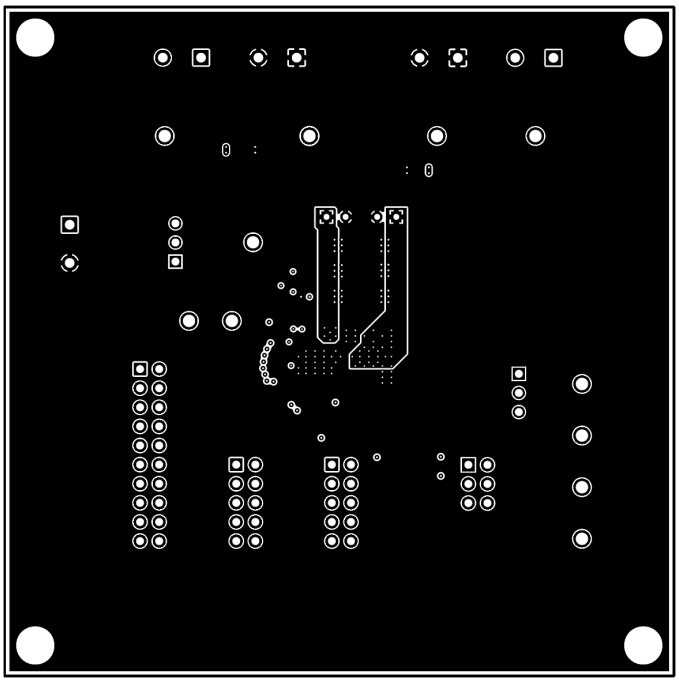

Figure 7-3. Layer 2 (Top View)

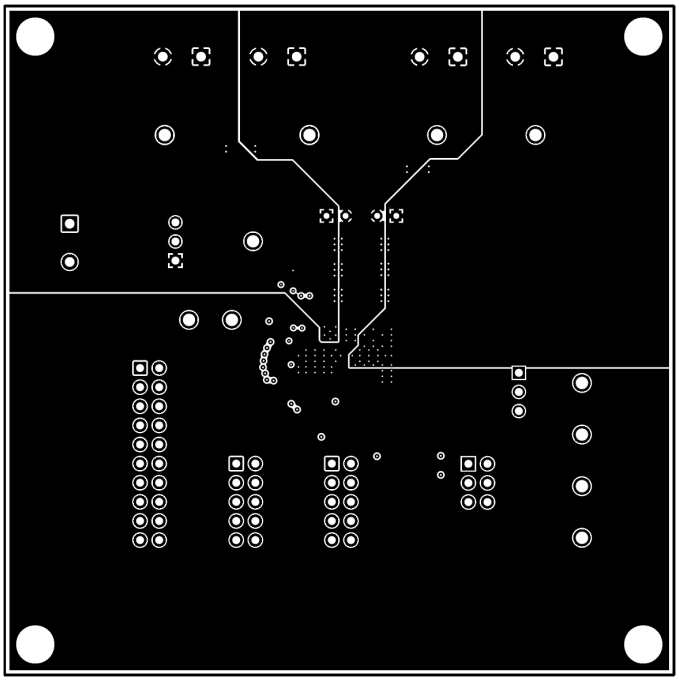

Figure 7-4. Layer 3 (Top View)

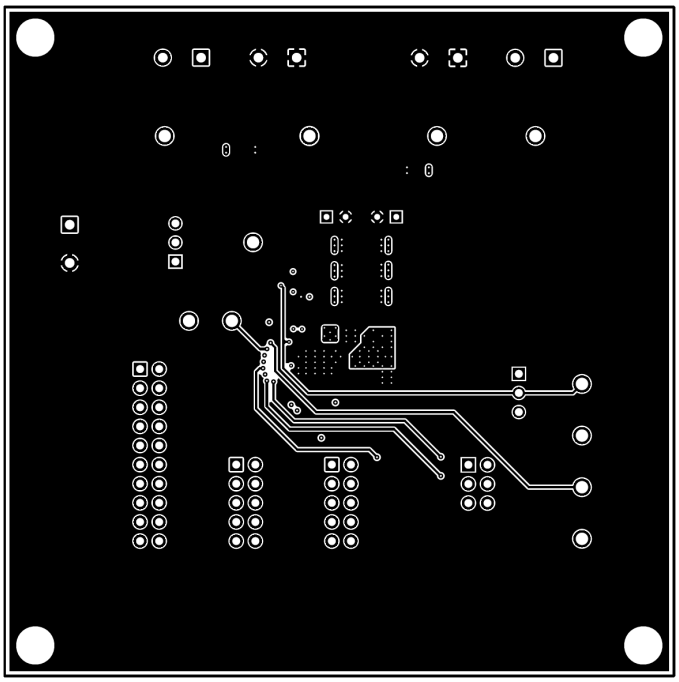

Figure 7-5. Layer 4 (Top View)

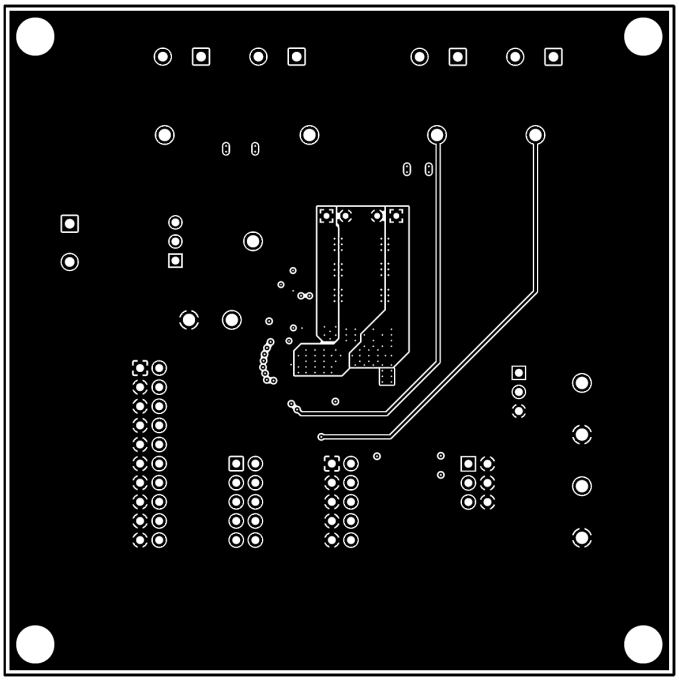

Figure 7-6. Layer 5 (Top View)

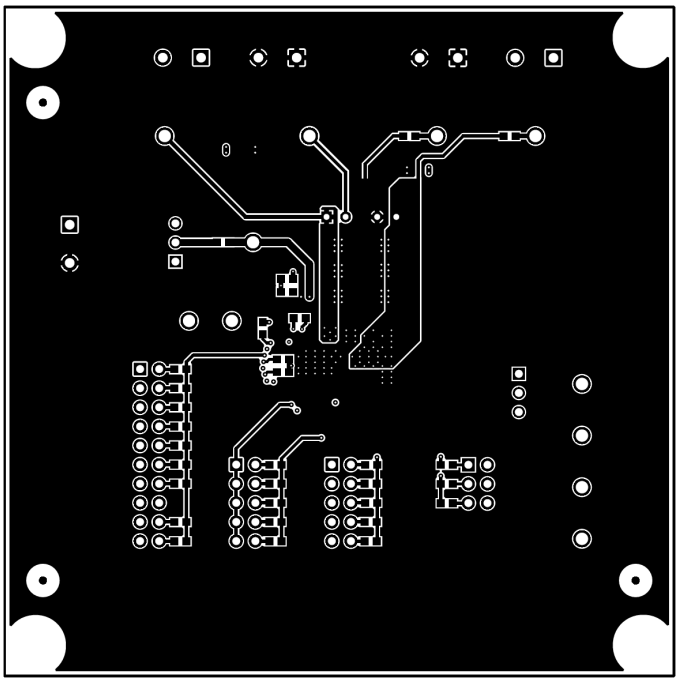

Figure 7-7. Layer 6 (Top View)

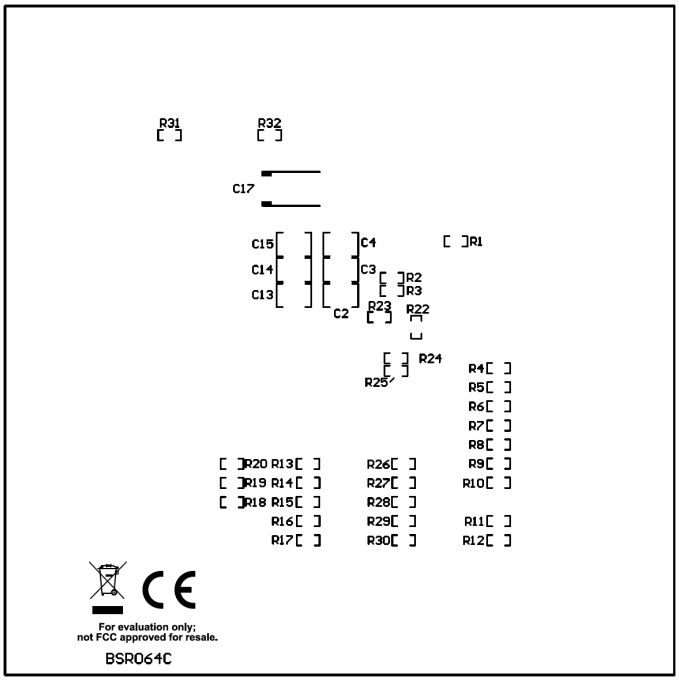

Figure 7-8. Bottom-Side Component Layout (Bottom View)

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2020) to Revision B (May 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2

Changes from Revision * (September 2020) to Revision A (October 2020)	Page
• Added waveforms to *Performance Data*	6

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