User's Guide

TPS37AQ1EVM User's Guide

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ABSTRACT

This user's guide describes the operational use of the TPS37AQ1EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS37x-Q1/TPS38x-Q1, a low-power, wide input voltage, overvoltage and undervoltage monitor. Included in this user's guide are setup instructions, a schematic diagram, printed-circuit board (PCB) layout drawings, and a bill of materials for the EVM.

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Trademarks

1 Introduction

The TPS37AQ1EVM helps design engineers to evaluate the operation and performance of the TPS37x-Q1/TPS38x-Q1 family of overvoltage and undervoltage monitors for possible use in their own circuit applications. This particular EVM configuration contains the TPS37A010122DSKRQ1, an overvoltage and undervoltage supervisor designed to monitor an adjustable rail with support for voltage dividers down to a 0.8V threshold voltage. The family of TPS37x-Q1/TPS38x-Q1 provides variable thresholds from 2.7 V to 36V and hysteresis options from 2% to 13% in a small 10-pin WSON package with both open-drain output and push-pull outputs. The TPS37x-Q1/TPS38x-Q1 family includes adjustable capacitor pins for tying capacitors to adjust delays on both the rising and falling edges of the RESET outputs. Separately available SENSE input pins allow the redundancy sought by safety-critical and high-reliability systems. Lastly, the device provides an optional manual reset that allows a hard reset and a latch feature for certain desired applications. Section 2 provides schematics, a BOM, and layout information on the board. Section 3 describes the connectors, jumpers, and test points for the device. Section 4 describes the setup and operation of the EVM.

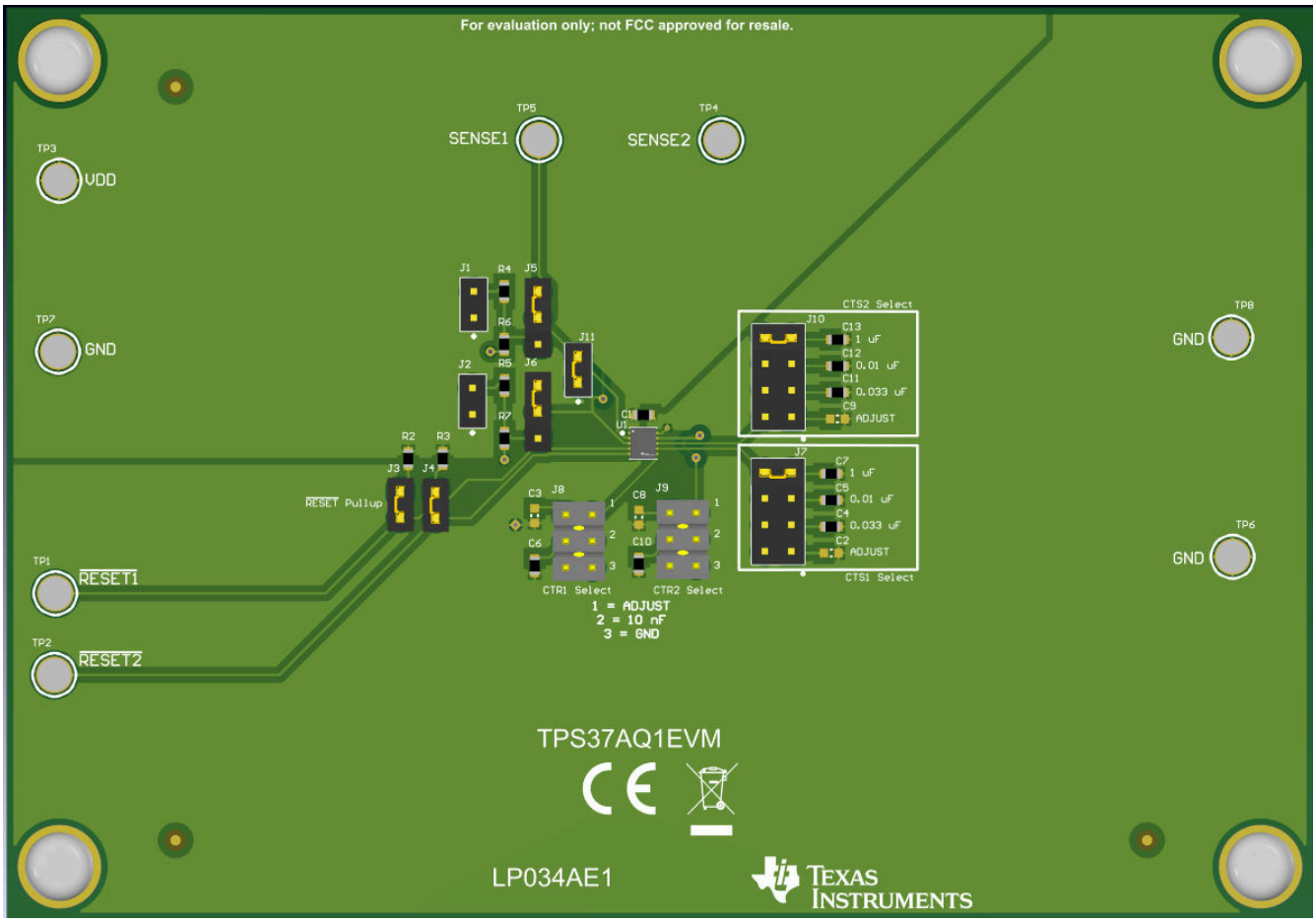

Figure 1-1. TPS37AQ1EVM Board - Top

1.1 Related Documentation

TPS37x-Q1 (65 V & 2uA) Over & Under Voltage Detector with Delay Function, SNVSBD9

Please see the TPS37x-Q1 datasheet for more detailed specifications, pin descriptions, applications, and other information related to the devices. This user guide provides information related to using the EVM.

2 Schematics, Bill of Materials, and Layout

This section provides a detailed description of the TPS37AQ1EVM schematic, bill of materials (BOM), and layout.

2.1 TPS37AQ1EVM Schematic

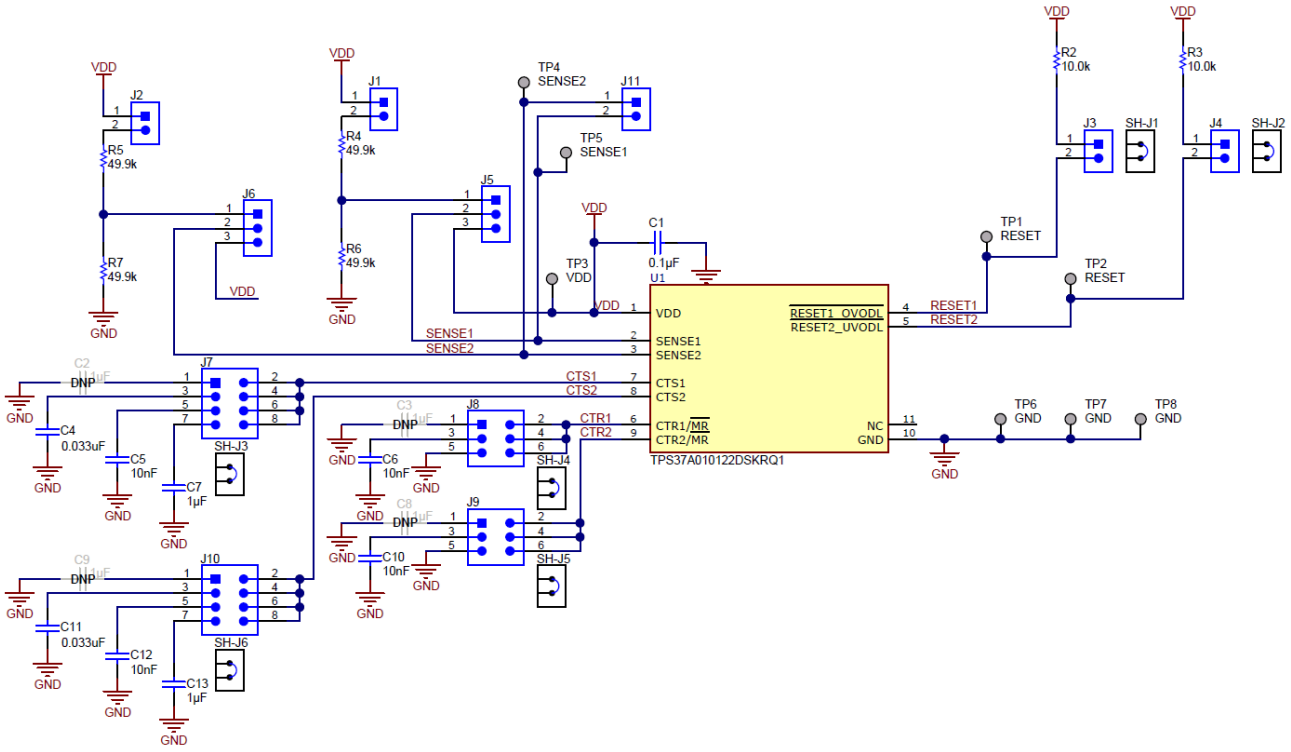

Figure 2-1. TPS37AQ1EVM Schematic

2.2 TPS37AQ1EVM Bill of Materials

Table 2-1. BOM

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		LP034A	Any
C1	1	0.1uF	CAP, CERM, 0.1 µF, 100 V,+/- 10%, X8L, AEC-Q200 Grade 0, 0603	0603	GCJ188L8EL104KA07D	MuRata
C4, C11	2	0.033uF	CAP, CERM, 0.033 uF, 100 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7S2A333K080 AB	TDK
C5, C6, C10, C12	4	0.01uF	CAP, CERM, 0.01 uF, 6.3 V, +/- 10%, X7R, 0603	0603	GRM188R70J103KA01D	MuRata
C7, C13	2	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden
FID1, FID2, FID3	3		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A

Table 2-1. BOM (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4, J11	5		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec
J5, J6	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J7, J10	2		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec
J8, J9	2		Header, 2.54mm, 3x2, Gold, TH	Header, 2.54mm, 3x2, TH	TSW-103-08-G-D	Samtec
R2, R3	2	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710KL	Yageo
R4, R5, R6, R7	4	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9	9	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	8		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone
U1	1		Over & Under Voltage Detector with Delay Function	WSON10	TPS37A010122DSKRQ1	Texas Instruments
C2, C3, C8, C9	0	1uF	CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0603	0603	UMK107AB7105KA-T	Taiyo Yuden

2.3 Layout and Component Placement

Figure 2-2 and Figure 2-3 are the top overlay and bottom overlay of the printed circuit board (PCB) and shows the component placement on the EVM. Figure 2-4 shows the top layout, Figure 2-5 and Figure 2-6 show the top and bottom layers, and Figure 2-7 and Figure 2-8 show the top and bottom solder masks of the EVM.

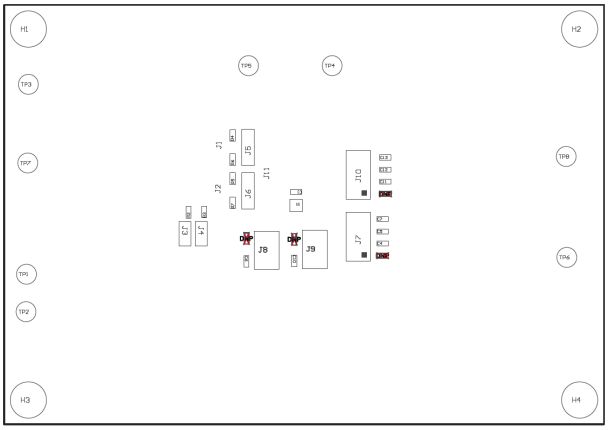

Figure 2-2. Component Placement - Top Overlay

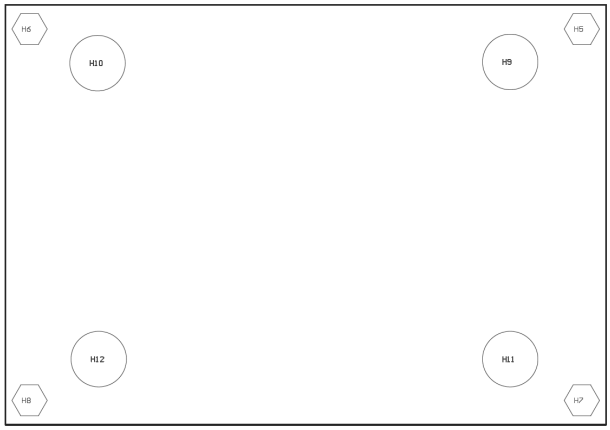

Figure 2-3. Component Placement - Bottom Overlay

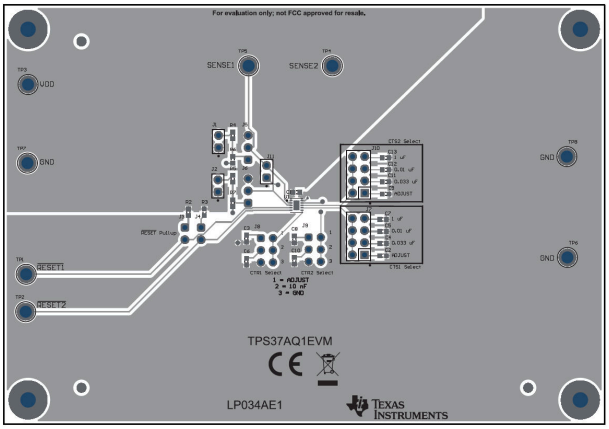

Figure 2-4. Layout - Top

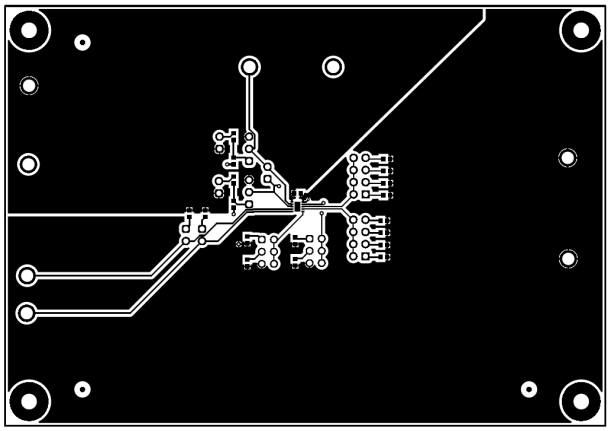

Figure 2-5. Top Layer

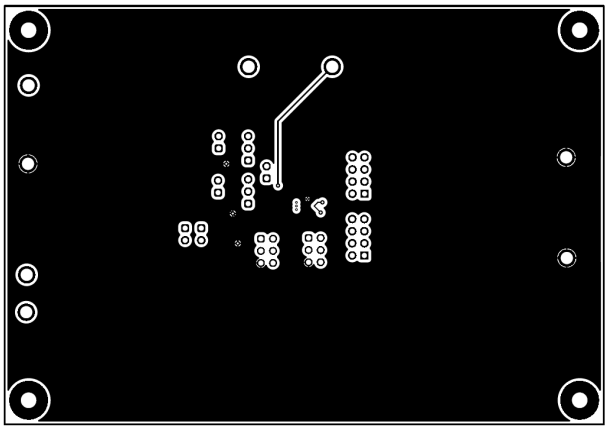

Figure 2-6. Bottom Layer

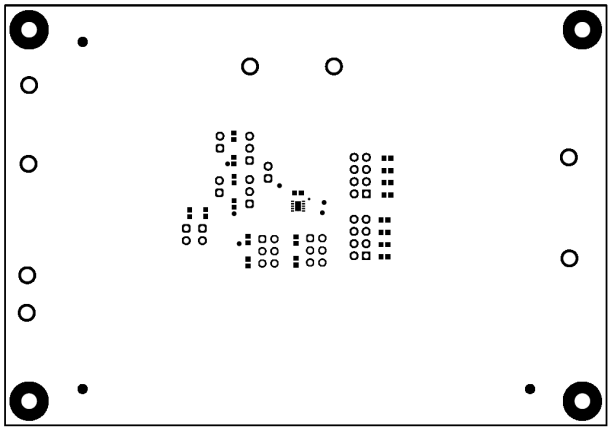

Figure 2-7. Top Solder Mask

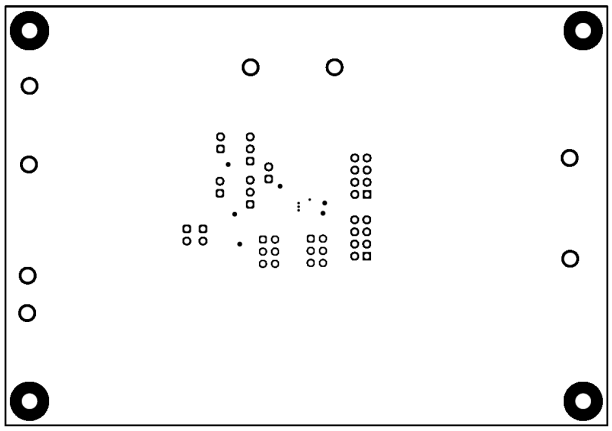

Figure 2-8. Bottom Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 3-1 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 3-1. Test Points

Test Point Number	Test Point Silkscreen Label	Function	Description
TP1	$\overline{\text{RESET1}}$	Connects to the output of RESET1 (for default configuration: $\overline{\text{RESET1}}$_OVODL	Allows user to monitor output signal at pin 4 of the device
TP2	$\overline{\text{RESET2}}$	Connects to the output of RESET2 (for default configuration: $\overline{\text{RESET2}}$_UVODL	Allows user to monitor output signal at pin 5 of the device
TP3	VDD	Connects to VDD pin	Allows user to measure the VDD pin
TP4	SENSE2	Connects to the input of SENSE2	Allows user to apply desired voltage to SENSE2 pin (pin 3)
TP5	SENSE1	Connects to the input of SENSE1	Allows user to apply desired voltage to SENSE1 pin (pin 2)
TP6	GND	Connects to ground	Allows user to use ground connections from multiple points.
TP7	GND	Connects to ground	Allows user to use ground connections from multiple points.
TP8	GND	Connects to ground	Allows user to use ground connections from multiple points.

3.2 EVM Jumpers

Table 3-2 lists the jumpers on the TPS37AQ1EVM. As ordered, the EVM will have seven jumpers installed.

Table 3-2. Jumpers

Jumper	Default Connection	Description
J1	Open	SENSE1 voltage divider jumper. Connects VDD to a halving voltage divider which feeds into SENSE1 if populated. (R_1 = R_2 = 49.9kΩ)
J2	Open	SENSE2 voltage divider jumper. Connects VDD to a halving voltage divider which feeds into SENSE2 if populated. (R_1 = R_2 = 49.9kΩ)
J3	Closed	Pullup jumper to connect RESET1 via a 10.0kΩ resistor to VDD (disconnect for push-pull configuration devices or to pullup to different voltage)
J4	Closed	Pullup jumper to connect RESET2 via a 10.0kΩ resistor to VDD (disconnect for push-pull configuration devices or to pullup to different voltage)
J5	Closed on top 2 pins	Selectable jumper to pick between halving voltage divider connection and direct VDD connection to SENSE1 (top 2 pins = voltage divider; bottom 2 pins: SENSE1 = VDD)
J6	Closed on top 2 pins	Selectable jumper to pick between halving voltage divider connection and direct VDD connection to SENSE2 (top 2 pins = voltage divider; bottom 2 pins: SENSE2 = VDD)
J7	Closed on position 1	Selectable jumper to pick between 4 options for terminating CTS1 (pin 7). Position 1 = 1uF, Position 2 = 0.01uF, Position 3 = 0.033uF, Position 4 = non stuffed to customize
J8	Open	Selectable jumper to pick between 3 options for terminating CTR1/MR (pin 6). Position 1 = non stuffed to customize, Position 2 = 10nF, Position 3 = GND (force Manual Reset)
J9	Open	Selectable jumper to pick between 3 options for terminating CTR2/MR (pin 9). Position 1 = non stuffed to customize, Position 2 = 10nF, Position 3 = GND (force Manual Reset)
J10	Closed on position 1	Selectable jumper to pick between 4 options for terminating CTS2 (pin 8). Position 1 = 1uF, Position 2 = 0.01uF, Position 3 = 0.033uF, Position 4 = non stuffed to customize
J11	Closed	Connects both SENSE1 and SENSE2 together to allow for single channel undervoltage and overvoltage monitoring. Disconnect to operate inputs/outputs separately.

4 EVM Setup and Operation

This section describes the functionality and operation of the TPS37AQ1EVM. The user should read the TPS37A-Q1 datasheet for electrical characteristics of the device.

4.1 Input Power (VDD)

The VDD supply is connected through the TP3 test point on board or via the proper jumpers that have a connection to VDD. TP3 is connected to the VDD pin of the TPS37A-Q1 device and TP7 is connected to the board common GND. The supply voltage range is 2.7V to 65V and a 0.1µF decoupling capacitor is recommended at the input for reducing noise that can propagate through the device (included on the EVM board at C1). Table 4-1 details the nominal supply voltage and typical input decoupling capacitor.

Table 4-1. Nominal Supply Parameters

Device	Nominal Supply Voltage (V)	Typical Decoupling Capacitor at Input
TPS37x-Q1, TPS38x-Q1	2.7V to 65V	0.1 µF

4.2 SENSE1/SENSE2 Inputs

The SENSE1 and SENSE2 inputs allow for any voltage rails to be monitored divided down through resistors. The default option of the TPS37AQ1EVM is populated with a TPS37A010122DSKRQ1 device, which has adjustable 0.8V thresholds. The resistors R4 and R6 (both 49.9kΩ) control the voltage divider for SENSE1. The resistors R5 and R7 (both 49.9kΩ) control the voltage divider for SENSE2. These 0603 resistors can be replaced with any values to form a voltage divider that can then divide down to trip at the 0.8V threshold. This behavior and instructions on selecting these resistors can be found described in the TPS37A-Q1 datasheet in the 'Adjustable Voltage Thresholds' section. To use the voltage divider located on-board, make sure to populate a jumper on J5 (shorting the first two pins) for SENSE1 and J6 (shorting the first two pins) for SENSE2 and connect the desired voltage rails to the header J1 for SENSE1 and J2 for SENSE2. Conversely, to monitor VDD on either SENSE1 or SENSE2 or both, populate a jumper on J5 (shorting the second two pins) for SENSE1 and J6 (shorting the second two pins) for SENSE2. If you wish to operate SENSE1 and SENSE2 as one input, you can tie these two together by populating a jumper on J11. The adjustable delays on the sense inputs can be found detailed in Section 4.5.

4.3 RESET1/RESET2 Outputs

The RESET1 and RESET2 outputs on the device represent the effect of the voltage monitoring after operating on the inputs SENSE1 and SENSE2, respectively. The device on the TPS37AQ1EVM is the TPS37A010122DSKRQ1, which represents an overvoltage active-low open-drain output on RESET1 and an undervoltage active-low open-drain output on RESET2. If using the EVM with another part in the TPS37x-Q1/TPS38x-Q1 family, adjustments need to be made to the default configuration to the EVM. For parts that use a push-pull topology instead of open-drain, you should depopulate the jumpers on J3 (pull-up to VDD for RESET1) or J4 (pull-up to VDD for RESET2). Additionally, if you want to use a different sized pull-up resistor on the reset pullups, either 10.0kΩ resistor at R2 or R3 can be replaced with another 0603 resistor. The RESET1 and RESET2 outputs can be pulled up to any voltage by depopulating the jumper on J3/J4 and connecting the top pin of the headers to any voltage lower than VDD.

4.4 Capacitor Time Delay Reset/$\overline{\text{MR}}$

The TPS37x-Q1 and TPS38x-Q1 family of devices contain two adjustable reset time delay pins that control the time with which the reset pins de-assert after they reach their valid condition. These pins also serve a dual purpose and act as a manual reset ($\overline{\text{MR}}$) when connected to logic ground. The user can adjust the configuration of these pins via the jumpers located at J8 and J9. Header J8 serves as the selectable option for CTR1/$\overline{\text{MR}}$ and header J9 serves as the selectable option for CTR2/$\overline{\text{MR}}$. Position 1 of the header (indicated by a 1) connects the pin to a unstuffed 0603 capacitor pad for the user to solder on a capacitor of choice. Position 2 of the header connects the pin to a 10 nF capacitor tied to ground. Position 3 of the header connects the pin to GND directly, shorting and creating a manual reset. Please see the adjustable Reset Time Delay Configuration on the TPS37x-Q1 datasheet for more detailed information on user programming.

4.5 Capacitor Time Delay Sense/$\overline{MR}$

The TPS37x-Q1 and TPS38x-Q1 family of devices contain two adjustable sense time delay pins that control the time with which the reset pins assert after they reach their invalid condition. The user can adjust the configuration of these pins via the jumpers located at J10 and J7. Header J10 serves as the selectable option for CTS1 and header J7 serves as the selectable option for CTS2. Position 1 of the header (located next to capacitor C7) connects the pin to a 1 µF capacitor tied to ground. Position 2 of the header (located next to capacitor C5) connects the pin to a 0.01 µF capacitor tied to ground. Position 3 of the header (located next to capacitor C4) connects the pin to a 0.033 µF capacitor tied to ground. Position 4 of the header (located next to capacitor pad C2) connects the pin to a unstuffed 0603 capacitor pad tied to ground which allows the user to solder on a capacitor of their choosing. Please see the Time Delay Configuration section on the TPS37x-Q1 datasheet for more detailed information on user programming.

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