User's Guide

TPS63802HDKEVM - Hardware Development Kit

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ABSTRACT

The TPS63802HDKEVM is a universal development tool designed to help you to easily and quickly evaluate and test the most common buck-boost converter use cases. The use cases include backup power, input current limit, LED driver, digital voltage scaling, bypass mode, and precise enable. You can easily select between the different use cases by changing jumpers and dip-switches. No soldering is required.

The TPS63802HDKEVM uses the TPS63802, the default output voltage is set to 3.3 V. The EVM operates from 1.8 V to 5.5 V input voltage. Output currents can go up to and above 2 A in buck and boost mode.

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1 Introduction

The Texas Instruments TPS63802 is a highly efficient, single-inductor, internally compensated, buck-boost converter in a 10-pin, 3-mm × 2-mm HodRod™ QFN package.

This special Hardware Development Kit highlights different use cases for this device family. Available use cases are:

- Standard operation (Section 4.1)
- Backup power supply (Section 4.2)
- High-side LED driver (Section 4.3)
- High-side LED driver with dimming option (Section 4.4)
- Input current limit (Section 4.5)
- Extended soft start or limit inrush current limitation (Section 4.6)
- Digital voltage scaling (Section 4.7)
- Output voltage tracking (Section 4.8)
- Bypass mode (Section 4.9)
- Precise enable and start-up delay (Section 4.10)

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2 Safety Instructions

CAUTION

Do not stare at operating lamp. May be harmful to the eyes.
Intense light sources have a high secondary exposure potential due to their blinding effect. A temporary reduction in visual acuity and afterimages can occur, leading to irritation, annoyance, visual impairment, and even accidents, depending on the situation. Always consider the use of light filtering/darkening protective eyewear and be fully aware of surrounding laboratory type set-ups when viewing intense light sources to minimize/eliminate such risks in order to avoid accidents related to temporary blindness.

CAUTION

RISK GROUP 2. Possible hazardous optical radiation emitted from this product. Do not stare at operating lamp. May be harmful to eyes.

- Do not stare at operating LEDs (Risk Group 2 (RG2) at 0.75 m).
- Per IEC 62471 ed 1.0: 2006-07 (“Photobiological Safety of Lamps and Lamp Systems”), this product has been classified in Risk Group 2. Products classified as Risk Group 2 do not pose a hazard due to the aversion response to very bright light sources or due to thermal discomfort.
- It should be noted that INTENTIONALLY staring at the lamp for extended lengths of time from short distances could lead to a potential risk of eye damage due to a retinal blue-light hazard. In order to reduce the potential of exposure to a retinal blue-light hazard, the operator must avoid any direct view of the LEDs while in operation, from a distance of 0.75 m, or closer.

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3 Setup

This section describes how to properly use the TPS63802HDKEVM.

3.1 Connector and Jumper Description

Table 3-1. Connector and Jumper Description

DESIGNATOR	PIN	SILKSCREEN NAME	DESCRIPTION
J1	1, 2	VIN	Positive input connection of the input supply
	3, 4	S+, S-	Input voltage sense connections. Measure the input voltage at this point.
	5, 6	GND	Vin GND return connection of the input supply. Common with other pins with “GND” label
J2	1, 2	VOUT	Output voltage connection
	3, 4	S+, S-	Vout and GND Sense lines for measuring the output voltage at the output capacitor
	5, 6	GND	Vout GND return connection for the output voltage. Common with other pins with “GND” label
J3	1, 2	VIN_MAIN	Positive input connection of the input supply. Used for backup power use case only
	3	ON	Active-low open-drain output, pulled low when U4 (LM66100) is disabled. Hi-Z when the chip is enabled.
	4	CE	Active-low IC enable of U4. Connected to VOUT for reverse current protection.
	5, 6	GND	Vin GND return connection of the input supply for backup power function. Common with other pins with “GND” label
J4	1, 2	VINLIM	Positive input connection of the input supply. Used for input current limit use case only.
J5	1	GND	Test point for GND. Common with other pins with “GND” label
	2	L1	Test point for L1 pin of the TPS63802
J6	1	GND	Test point for GND. Common with other pin with “GND” label
	2	L2	Test point for L2 pin of the TPS63802
JP1	1, 2, 3	PFM, MODE, PWM	PFM/PWM mode selection. Short pin 1 and 2 for power save mode. Short pin 2 and 3 for forced-PWM mode. It must not be left floating.
JP3	1	BPM	Connect short between JP3 pin3 and JP1 pin 2 to use bypass mode use case.
JP2	1, 2, 3	OFF, EN, ON	Short jumper between the center pin EN and ON to turn on TPS63802. Short jumper between the center pin EN and OFF to turn TPS63802 off
JP4	1, 2, 3	EN, BYP, VIN	Short jumper between the center pin EN and BYP to turn on U9. Short jumper between the center pin BYP and VIN to turn U9 off
JP5	1, 2, 3	CS, VOUT, DM	Short jumper between the center pin Vout and CS (constant current) to enable the LED driver with high-side sensing function. Short jumper between the center pin Vout and Dimming to enable Voltage Controlled Current Source function
JP6	1, 2	GND, VSEL	GND connection and 2-level output voltage selection signal
JP7	1, 2		Short jumper to connect the power supply for output voltage tracking function
JP8	1, 2	GND, VCTRL	GND connection and external voltage reference connection
JP9	1, 2	GND, VTRACK	GND connection and external voltage reference connection

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Table 3-1. Connector and Jumper Description (continued)

DESIGNATOR	PIN	SILKSCREEN NAME	DESCRIPTION
JP10	1, 2		Short jumper to connect the VIN with the output pin of ideal diode U4
JP11	1, 2		Short jumper to connect the VOUT with the input pin of ideal diode U4
JP12	1, 2		Short jumper to connect the power supply for high-side load current sense circuit, U2
JP13	1, 2		Short jumper to connect the power supply for input current sense circuit, U3
JP14	1, 2		Short jumper to connect the cathode of D4 to VIN. For backup power, pre-charge function
JP15	1, 2		Short jumper to connect the power supply for LED dimming function op amp, U5
JP16	1, 2		Short jumper to connect the positive of super cap to VIN pin
JP17	1, 2		Short jumper to connect the power supply to super capacitor voltage monitor, U6
JP18	1	GND	Test point for GND. Common with other pins with “GND” label
	2	VREF	Connect to a adjustable voltage source to dim LED the brightness
TP1	1		Feedback node test point connection
TP2	1	PG	Power Good (PG) test point connection. Place R4 = 100 kΩ if this function needed.
S1	Pos 1		Connects high-side resistor to FB pin
	Pos 2	FB_LED_ADJ	Enables LED dimming function
	Pos 3	FB_LED_CONST	Enables high-side LED driver function
	Pos 4	FB_SOFT_START	Enables soft start and inrush current limit function
	Pos 5	FB_INPUT_LIM	Enables input current limit function
	Pos 6	FB_DVS	Enables digital voltage scaling function
	Pos 7	FB_VTRACK	Enables output voltage tracking function
	Pos 8		Connects low-side resistor to FB pin

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4 Use Case Description

This chapter describes the different board functions. It provides quick setups with a standard connection picture and standard jumper configuration table for each function. Furthermore, most use cases contain a design modification guide and typical performance images.

4.1 Standard Operation

This chapter describes the standard buck-boost operation and has similar performance and features like the TPS63802EVM. It is suitable for testing the current capability, efficiency, and other basic performance.

Set the jumpers and multi-switch of the EVM according to Figure 4-1 or Table 4-1. It configures the EVM to 3.3-V output voltage with PFM enabled. It is recommended to do efficiency tests with the standard TPS63802EVM.

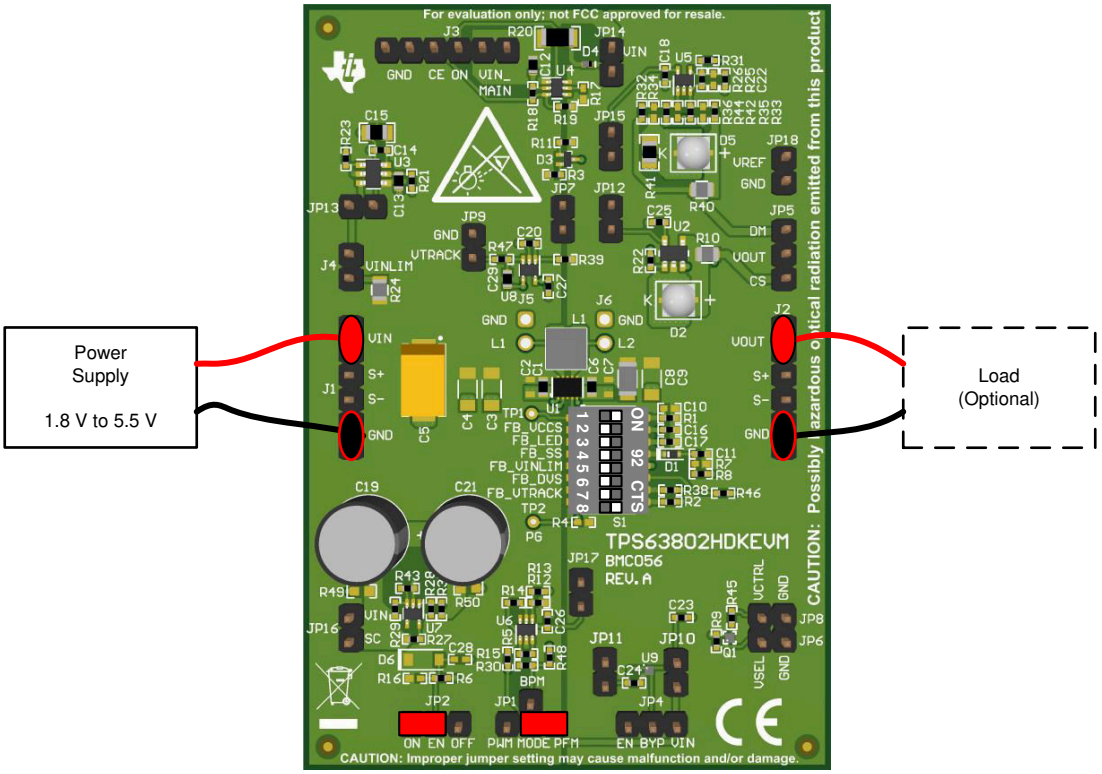

Figure 4-1. Quick Start Connection for Standard Operation

Table 4-1. Configuration of the Jumpers for Standard Operation

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 to select PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
All other JPx and Jx			Do not connect.
S1	Pos 1 and Pos 8		Set to ON.
	All other		Set to OFF.

4.1.1 Further Information

Check the *TPS63802 2-A, High-efficient, Low IQ Buck-boost Converter with Small Solution Data Sheet* and *TPS63802 EVM User's Guide* for more information.

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4.2 Backup Power

A backup power supply is an electrical system that provides emergency power to a load when the main power source fails. An appropriate backup power supply provides instantaneous protection from main power interruptions without glitches, by supplying energy which is stored in backup capacitors or batteries. Such backup power supplies are typically used to protect equipment such as solid state drives (SSDs), on board diagnosis (OBD), storage systems, where an unexpected power disruption can cause malfunction or data loss.

Figure 4-2 shows the block diagram and operation. The TPS63802 buck-boost converter operates bidirectionally. It supports energy transfer from the input to the output, as well as from the output to the input. Therefore, during standard operation, the main power directly supplies the load, and the backup capacitor is charged using the reverse current through the TPS63802 buck-boost converter. During backup operation, the buck-boost converter supplies the system from the backup capacitors.

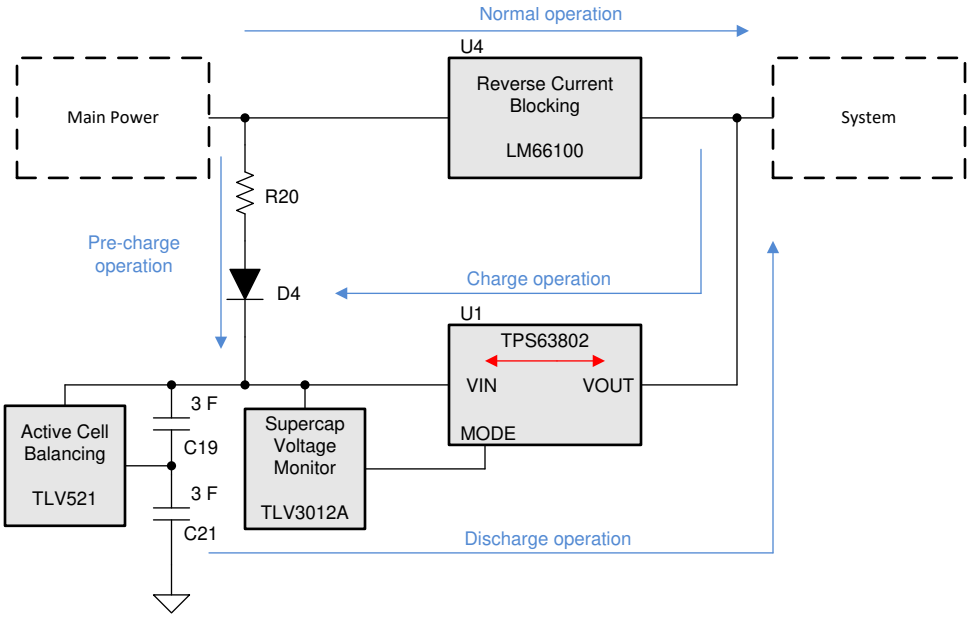

Figure 4-2. Block Diagram for Backup Power

4.2.1 Setup

Figure 4-3 and Table 4-2 show the jumper and dip switch configuration. Follow these configurations and the EVM can be used to verify backup power supply function.

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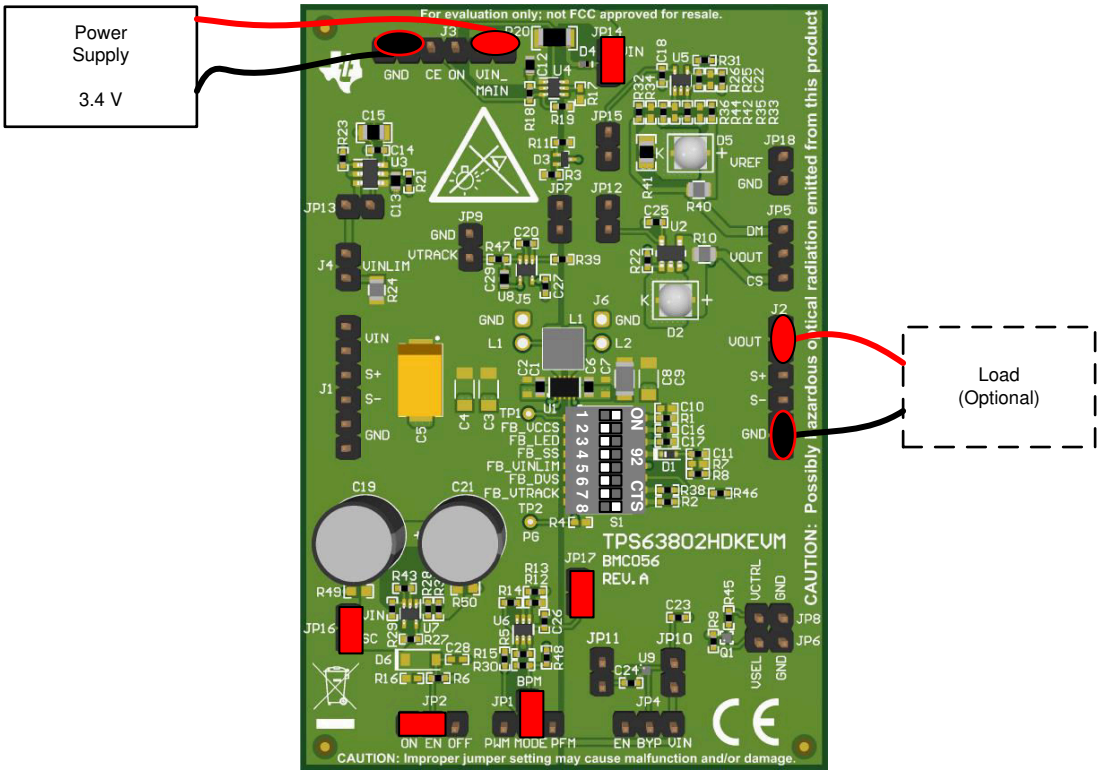

Figure 4-3. Quick Start Connection for Backup Power

Table 4-2. Configuration of the Jumpers for Backup Power

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the load.
J3	1, 2	VIN_MAIN	Connect the positive terminal of the power supply set to 3.4 V.
	5, 6	GND	Connect the GND terminal of the power supply.
JP1	JP1-2, JP3-1	BPM, MODE	Place short between JP1 pin 2 (MODE) and JP3 pin 1 (BPM).
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
JP14	1, 2		Place short to connect pre-charge path to Vin.
JP16	1, 2		Place short to connect the backup capacitors to Vin.
JP17	1, 2		Place short to connect power supply to backup capacitor voltage monitor.
All other JPx and Jx			Do not connect.
S1	Pos 1 and Pos 8		Set to ON.
	All other		Set to OFF.

4.2.2 Typical Performance

Figure 4-4 shows the pre-charging and charging of the backup capacitor. Figure 4-5 shows the backup operation.

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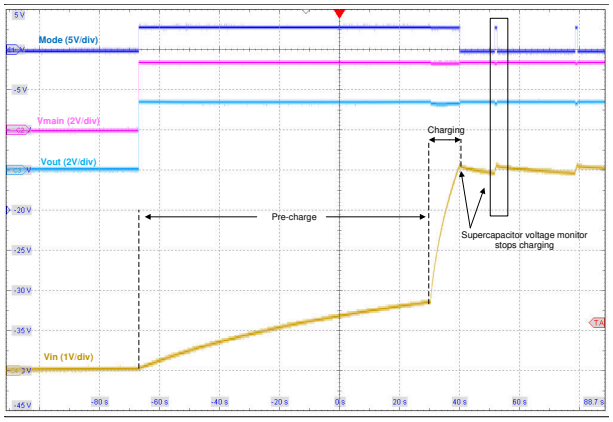

Figure 4-4. Pre-charge Waveform

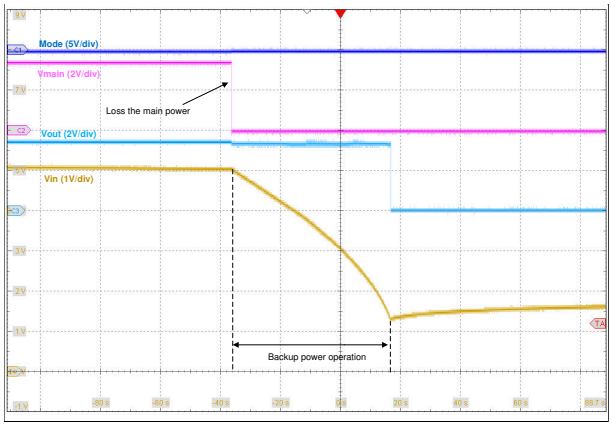

Figure 4-5. Discharge Waveform

4.2.3 Design Guidance

This section shows how to modify the EVM components to support different pre-charge currents or maximum supercapacitor charging voltages.

4.2.3.1 Change the VIN_MAIN Supply

The TPS63802 starts up at low 1.8 V Vin and operates down to 1.3 V during standard operation, but considering the voltage drop of the pre-charge diode, it is recommended to keep VIN_MAIN above 2.2 V. If VIN_MAIN is changed, the output voltage target of the TPS63802 needs to be changed as well.

The default setup of this EVM is optimized for VIN_MAIN = 3.4 V. During backup operation, the TPS63802 output is set to 3.3 V.

With a combination with the digital voltage scaling feature described in Section 4.7, the output voltage can be set equal to VIN_MAIN during backup operation.

4.2.3.2 Change the Pre-charge Current

The pre-charge current can be calculated as:

$$I_{pre} = \frac{VIN_{MAIN} - VIN - V_d}{R_{limit}} \quad (1)$$

The current changes during VIN rise. If VIN rises high enough, the charge current through this path is stopped. At initial start-up, the supercapacitor is empty and VIN equals to zero. So, the maximum pre-charge current is:

$$I_{pre} = \frac{VIN_{MAIN} - V_d}{R_{limit}} \quad (2)$$

4.2.3.3 Change the Maximum Supercapacitor Voltage

Modifying R12, R13 changes the maximum supercapacitor voltage (V_{SC}) as:

$$V_{SC} = V_{ref} \frac{R12 + R13}{R13} \quad (3)$$

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Here, V_{ref} is the integrated voltage reference of 1.242 V, and the default value for V_{SC} is 5 V. Modifying R14 and R15 changes the charging/discharging hysteresis (V_{hyst}).

$$V_{hyst} = V_{+} \frac{R14}{R14 + R15} \tag{4}$$

Here, V_{+} is the supply voltage for the TLV3012. Assuming V_{+} = 3.4 V, V_{hyst} equals to 59 mV.

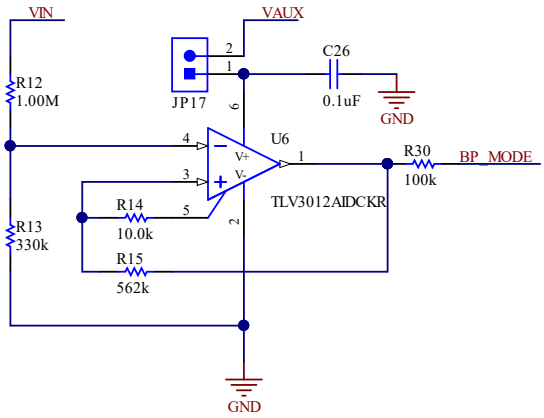

Figure 4-6. Supercapacitor Voltage Monitor

4.2.4 Further Information

Further information on the specific application is available in the following application reports:

- *Smart Electricity Meter Supercapacitor Backup Power Supply With Current Limit*
- *Supercapacitor Backup Power Supply with the TPS63802*
- *High-Efficiency Backup Power Supply*

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4.3 High-side LED Driver - Constant Current

This chapter shows a high-side LED driver solution with a current sense amplifier that achieves a regulated and constant current to drive the LED.

With this solution, the cathode of the LED is directly connected to ground. Since most LEDs use the cathode for sinking heat, no isolation to ground is needed. This makes the design of heat sinks for the LED is much easier.

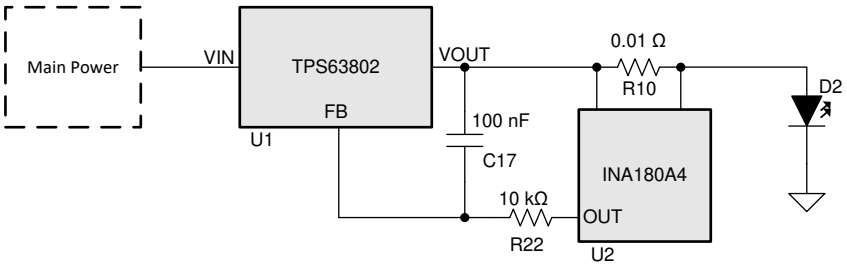

Figure 4-7. Block Diagram for High-side LED Driver -- Constant Current

4.3.1 Setup

CAUTION

RISK GROUP 2. Possible hazardous optical radiation emitted from this product. Do not stare at operating lamp. May be harmful to eyes.

Figure 4-8 and Table 4-3 show the jumper and dip switch configuration.

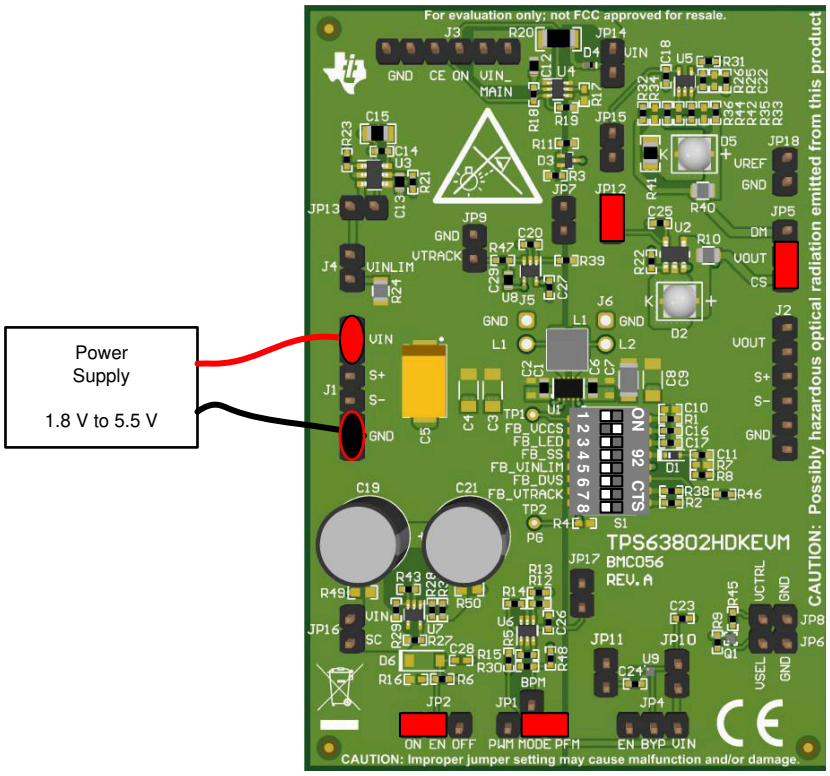

Figure 4-8. Quick Start Connection for High-side LED Driver -- Constant Current

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Table 4-3. Configuration of the Jumpers for High-side LED Driver -- Constant Current

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 to select PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
JP5	1, 2	CS, VOUT	Place short between pin 1 and pin 2 to connect VOUT to D2
JP12	1, 2		Place short to connect the power supply to U2.
All other JPx and Jx			Do not connect.
S1	Pos 2		Set to ON.
	All other		Set to OFF.

4.3.2 Typical Performance

Table 4-4. Recommendation for High-side LED Driver-- Constant Current Function

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN		1.8	3.3	5.5	V
I_{LED}			0.25		A

4.3.3 Design Guidance

This section shows how to modify the EVM to support a different LED current.

4.3.3.1 Change the Current of LED

The main principle of this design is to make the output voltage of the INA180 reach the reference value of TPS63802 FB pin. The output voltage of INA180 ($V_{OUT;INA180A}$) can be calculated as:

$$V_{OUT;INA180} = V_{FB} = I_{LED} \times R10 \times Gain \quad (5)$$

While the gain of the INA180A4 is 200, R10 is 0.01 Ω, V_{FB} = 0.5 V, and the default value for I_{LED} is 0.25 A. For the target current value (I_{target}), the simplest way is to change the sense resistance (R10) as:

$$R10 = \frac{V_{FB}}{Gain \times I_{target}} \quad (6)$$

Changing the gain is another solution. The INA180 has four gain options that are described in the data sheet.

4.3.4 Further Information

Further information on the specific application is available in the following documents:

- *Different Methods to Drive LEDs Using TPS63xxx Buck-Boost Converters Application Report*
- *INAx180 Low- and High-Side Voltage Output, Current-Sense Amplifiers Data Sheet*

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4.4 High-side LED Driver with Dimming

Some applications need to adjust the LED brightness. For example, in security cameras, the LED needs to be dimmed by changing the DC current to avoid the rolling shutter effect that can occur if PWM dimming is used. The rolling shutter effect can be seen as a flicker in the camera image. For this purpose, this solution controls the current through the LED with a signal from an MCU or processor. A popular way is to use a reference voltage to control the LED current to achieve the dimming function.

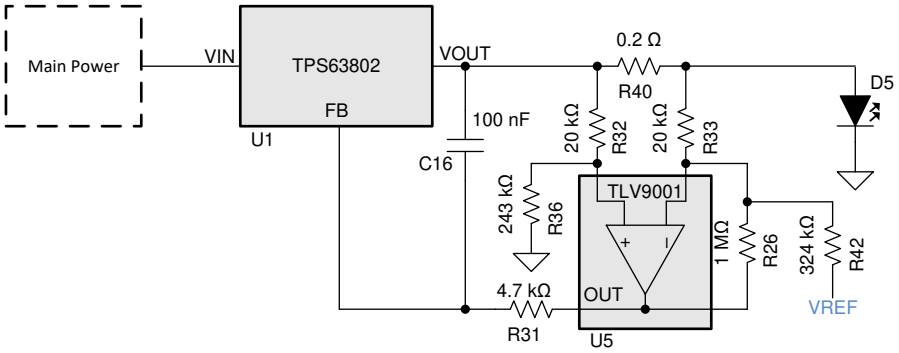

Figure 4-9. Block Diagram for High-side LED Driver with Dimming

4.4.1 Setup

CAUTION

RISK GROUP 2. Possible hazardous optical radiation emitted from this product. Do not stare at operating lamp. May be harmful to eyes.

Figure 4-10 and Table 4-5 show the jumper and dip switch configuration.

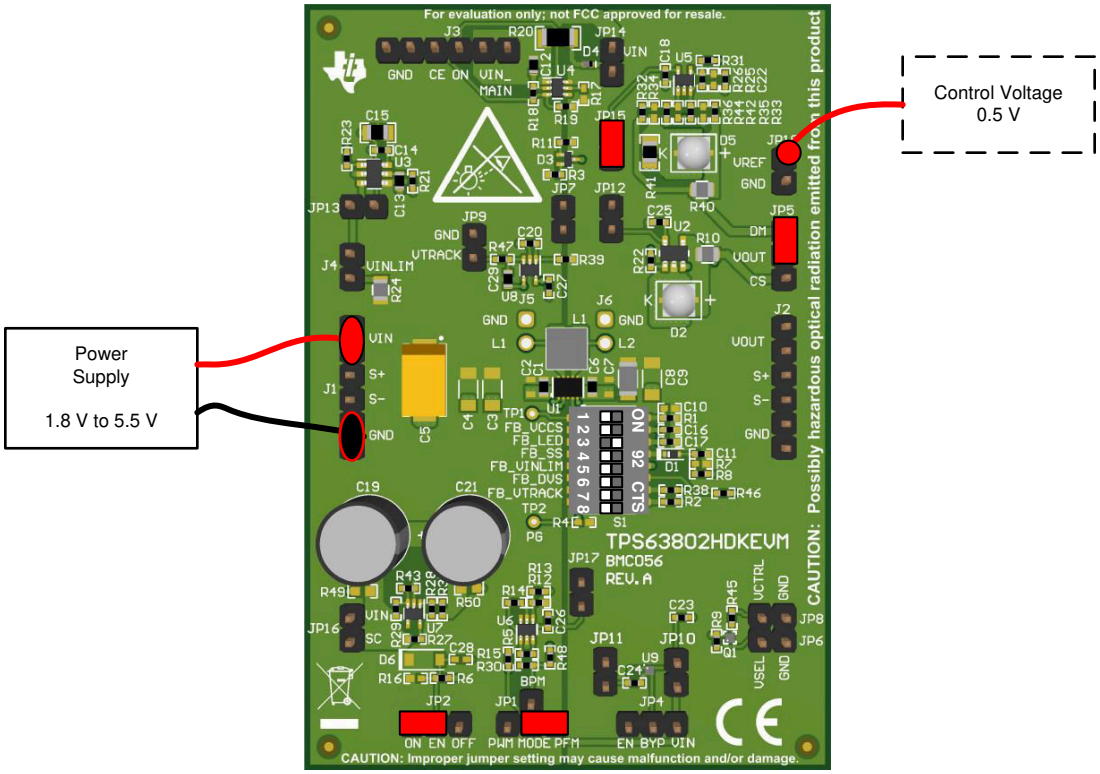

Figure 4-10. Quick Start Connection for High-side LED Driver--Dimming

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Table 4-5. Configuration of the Jumpers for High-side LED Driver with Dimming

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 to select PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
JP5	2, 3	VOUT, DM	Place short between pin 3 and pin 2 to connect VOUT to D5.
JP15	1, 2		Place short connects the power supply to U5.
JP18	1, 2	GND, VREF	Connect control voltage supply set to 0.5 V. Connect the positive terminal to pin 2 and the GND terminal to pin 1.
All other JPx and Jx			Do not connect.
S1	Pos 3		Set to ON.
	All other		Set to OFF.

4.4.2 Typical Performance

Figure 4-11 shows the LED current (pink), output voltage (dark blue), and the feedback voltage (light blue) in respect to the control voltage VREF (yellow).

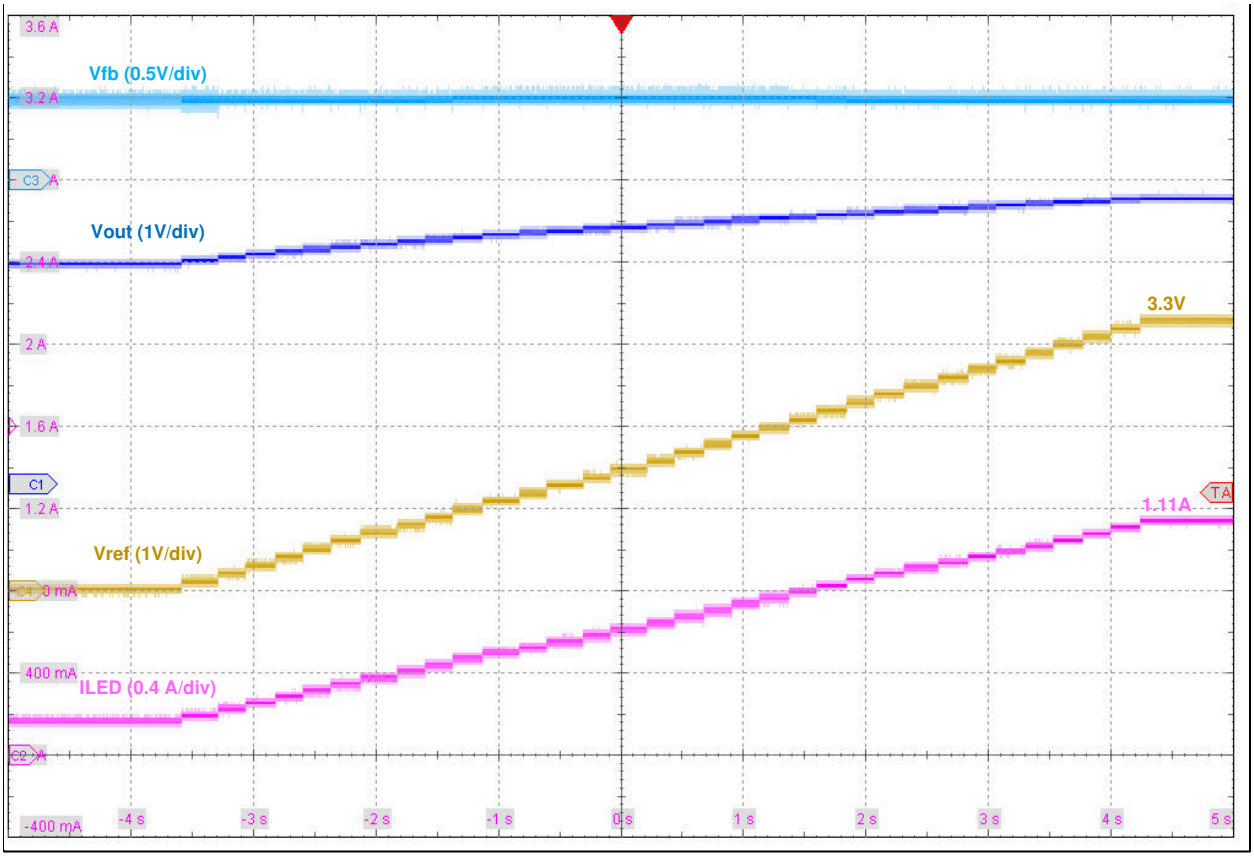

Figure 4-11. Typical Waveform Showing the LED Current in Respect to VREF

Table 4-6. Recommendation for High-side LED Driver with Dimming Function

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN		1.8	3.3	5.5	V

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Table 4-6. Recommendation for High-side LED Driver with Dimming Function (continued)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LED}	V_{REF} = 0 V		0.05		A
	V_{REF} = 3 V		1		A

4.4.3 Design Guidance

This section shows how to modify the EVM to support a different LED current.

4.4.3.1 Change the Current of the LED

For this solution, you can control the current of the LED with a DC voltage reference signal called V_{Ref}. There is a lower and upper limit for the adjustable current value. According to the *Different Methods to Drive LEDs Using TPS63xxx Buck-Boost Converters Application Report*, the relationship of V_{Rsense} with other parameters is:

$$V_{Rsense} = \frac{R33}{R26} \times V_{FB} + \frac{R33}{R42} \times V_{REF} = I_{LED} \times R_{Sense} \quad (7)$$

where

- R_{Sense} = R40

The lower limit of I_{LED} can be calculated as:

$$I_{LED\_min} = \frac{R33}{R26 \cdot R_{Sense}} \cdot V_{FB} + \frac{R33}{R42 \cdot R_{Sense}} \cdot V_{REF\_Min} \quad (8)$$

The upper limit of I_{Led} can be calculated as:

$$I_{LED\_max} = \frac{R33}{R26 \cdot R_{Sense}} \cdot V_{FB} + \frac{R33}{R42 \cdot R_{Sense}} \cdot V_{REF\_Max} \quad (9)$$

The combination of the resistors R26, R33, R40, and R42 is flexible. The lower R_{Sense}, the lower the power loss, but smaller R_{Sense} reduces the accuracy. There is a tradeoff and it depends on detailed requirements.

4.4.4 Further Information

Further information on the specific application is available in the following application report:

- *Different Methods to Drive LEDs Using TPS63xxx Buck-Boost Converters*

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4.5 Input Current Limit

The TPS63802 has an integrated peak current limit of typically 5 A in buck-boost mode. In some cases, the current limit is beyond the capability of the power supply. This is especially true for primary batteries. Therefore, the supply voltage can drop when loaded with large currents. This can cause malfunction in other parts of the system or block the TPS63802 to start up.

This chapter shows how to use a current sense amplifier to limit the input current.

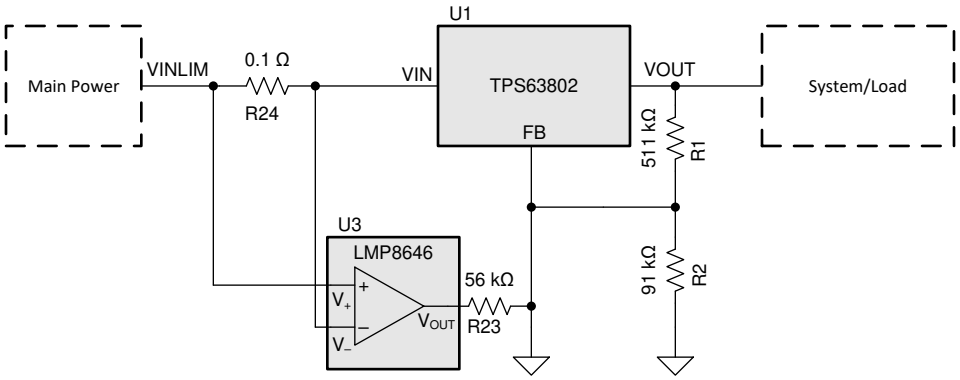

Figure 4-12. Block Diagram for Input Current Limitation

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4.5.1 Setup

Figure 4-13 and Table 4-7 show the jumper and dip switch configuration.

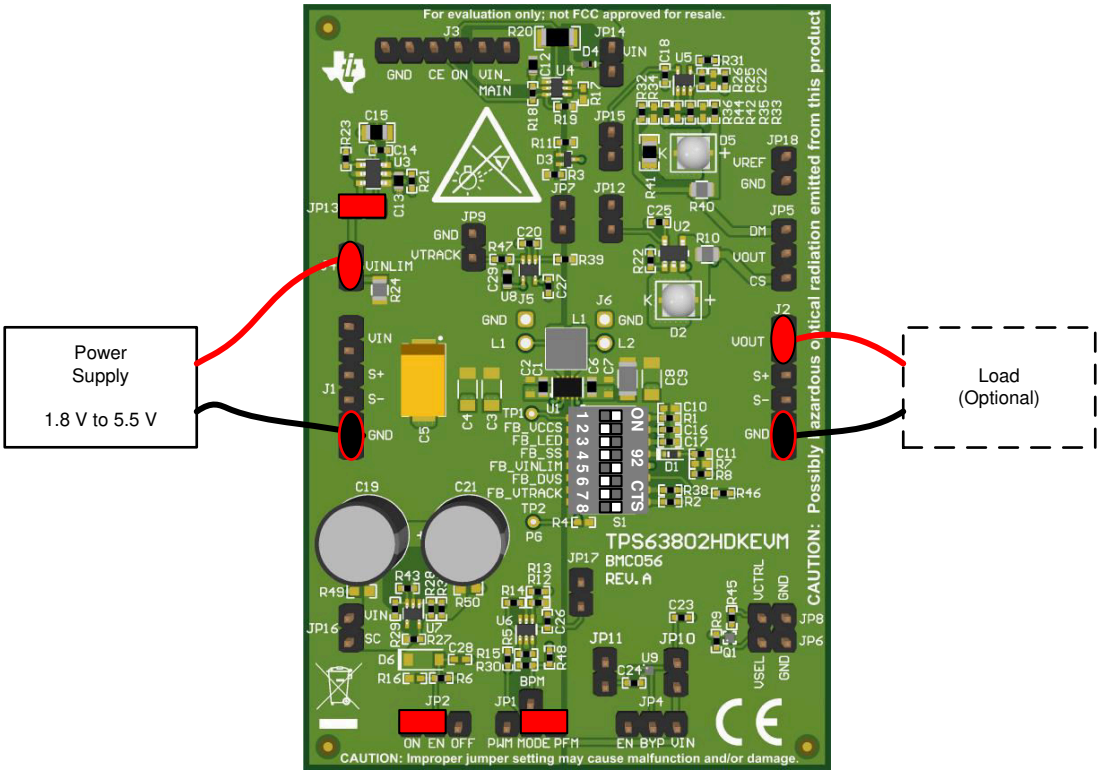

Figure 4-13. Quick Start Connection for Input Current Limitation

Table 4-7. Configuration of the Jumpers for input Current Limitation

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Do not connect.
	5, 6	GND	Connect the GND terminal of the power supply.
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.
J4	1, 2	VINLIM	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 to select PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
JP13	1, 2		Place short to connect the power supply to U3.
All other JPx and Jx			Do not connect.
S1	Pos 1, Pos 5, and Pos 8		Set to ON.
	All other		Set to OFF.

4.5.2 Typical Performance

Table 4-8. Recommendation for Input Current Limitation Function

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN		1.8	3.3	5.5	V
VOUT	Input current < 0.1 A		3.3		V
Input current	Depends on external load	0		0.1	A

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4.5.3 Design Guidance

This section shows how to modify the EVM components to change the input current limit.

4.5.3.1 Change the Limitation of Input Current

According to the data sheet of the LMP8646 current limiter, the output voltage of the LMP8646 can be calculated with:

$$V_{OUT\_LMP} = (R_{Sense} \times I_{Sense}) \times Gain \quad (10)$$

where

- R_{Sense} = R24
- Gain = R21 / R_{in}
- R_{in} is integrated in the LMP8646 as 5 K Ω

When the current reaches I_{limit}, the Vout_LMP reaches the target value of 0.5 V for the TPS63802.

$$I_{limit} = \frac{0.5\,V \times 5\,k\Omega}{R24 \times R21} \quad (11)$$

For most applications, the best performance is obtained with an R_{Sense} value that provides a V_{Sense} of 100 mV to 200 mV.

4.5.4 Further Information

Further information on the specific application can be found in the following application report or data sheet:

- *Extending the Soft-Start Time Without a Soft-Start Pin Application Report*
- *LMP8646 Precision Current Limiter Data Sheet*

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4.6 Inrush Current Limitation by Extending Soft-start Time

As described in the previous chapter, some power supplies are not capable of delivering high currents. Start-up is especially a problem if the DC/DC converter needs to load a high output capacitance, the inrush current can exceed the limits of the power supply. This can cause voltage drops that lead to possible system malfunctions.

This circuit limits the inrush current by extending the soft-start time, while not limiting the DC output current. With this, circuit peak currents at start-up can be reduced while still allowing higher DC output currents.

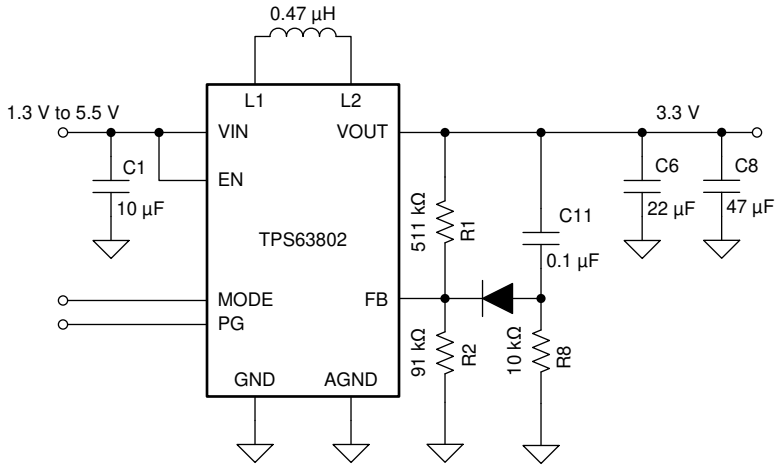

Figure 4-14. Block Diagram for Inrush Current Limitation

4.6.1 Setup

Figure 4-15 and Table 4-9 show the jumper and dip switch configuration.

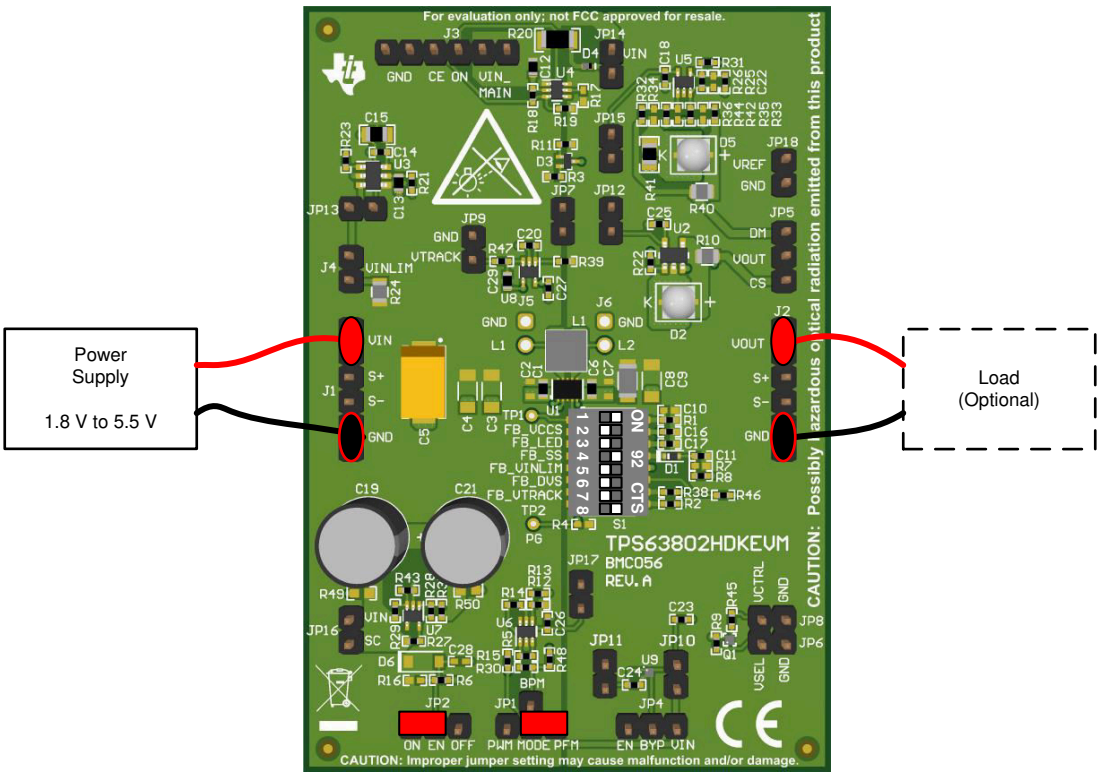

Figure 4-15. Quick Start Connection for Extending Soft Start or Inrush Rurrent Limitation

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Table 4-9. Configuration of the Jumpers for Extending Soft Start or Inrush Current Limitation

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 to select PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enablesTPS63802.
All other JPx and Jx			Do not connect.
S1	Pos 1, Pos 4, and Pos 8		Set to ON.
	All other		Set to OFF.

4.6.2 Typical Performance

This section shows the difference between the standard operation at start-up and with additional passive inrush current limit circuit.

Table 4-10 summarizes the typical performance of this EVM in the two operating modes with a 30-Ω load.

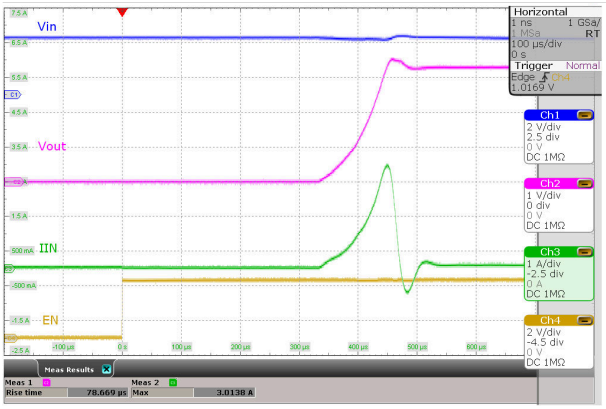

Figure 4-16. Typical Start-up Standard Operation

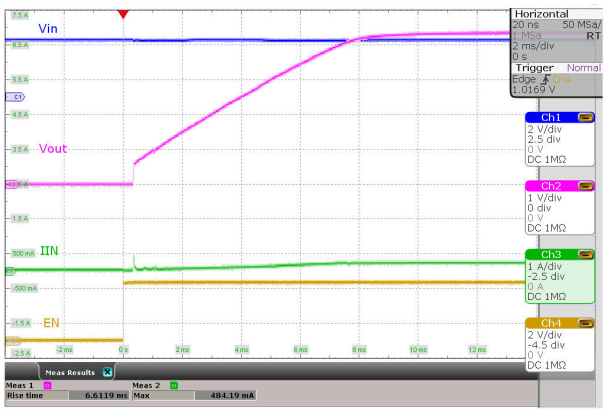

Figure 4-17. Typical Start-up with Inrush Current Limit and Extended Soft Start

Table 4-10. Recommendation for Extending Soft-start Time or Limiting Inrush Current

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN		1.8	3.3	5.5	V
VOUT	Standard operation, C6 = 22 µF, C8 = 47 µF, R_{Load} = 30 Ω		3.3		V
Inrush current			3.0		A
Soft start time			78		µs
VOUT	Soft start operation, C6 = 22 µF, C8 = 47 µF, R_{Load} = 30 Ω R8 = 10 kΩ, C11 = 100 nF		4.3		V
Inrush current			0.48		A
Soft-start time			6612		µs

4.6.3 Design Guidance

The soft-start time is roughly proportional to the product of R8 and C11. As this product goes up, the soft-start time increases and the inrush current is reduced. If the product is too low, hardly any soft-start time is added.

Laboratory verification is necessary to ensure a particular soft-start time for a given system with a given output capacitance and load in the midst of component variation over tolerance and temperature.

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4.6.4 Further Information

Further information on the specific application can be found in this application report:

- *Extending the Soft Start Time Without a Soft-start Pin*

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4.7 Dynamic Voltage Scaling

In this chapter, two solutions are discussed. One is two-level voltage selection and the other one is analog signal control. Both of them are aimed to achieve dynamic change of the output voltage target during operation.

The difference is that "two-level voltage selection" uses a digital signal to control a FET, and only has two target selections. "Analog signal control" on the other hand, uses a DAC or another analog reference voltage. It can control the output voltage with multiple target values within the available range.

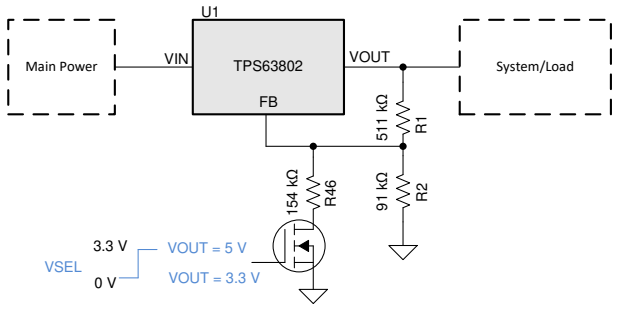

Figure 4-18. Block Diagram for Two Level Dynamic Voltage Scaling

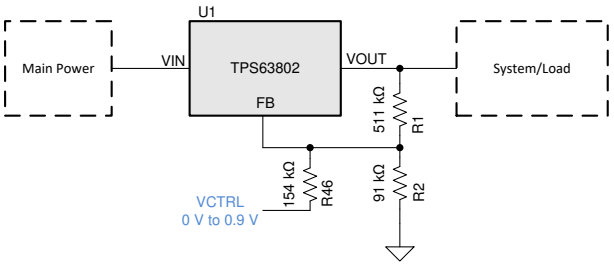

Figure 4-19. Block Diagram for Analog Dynamic Voltage Scaling

4.7.1 Setup

Figure 4-20 and Table 4-11 show the jumper and dip switch configuration.

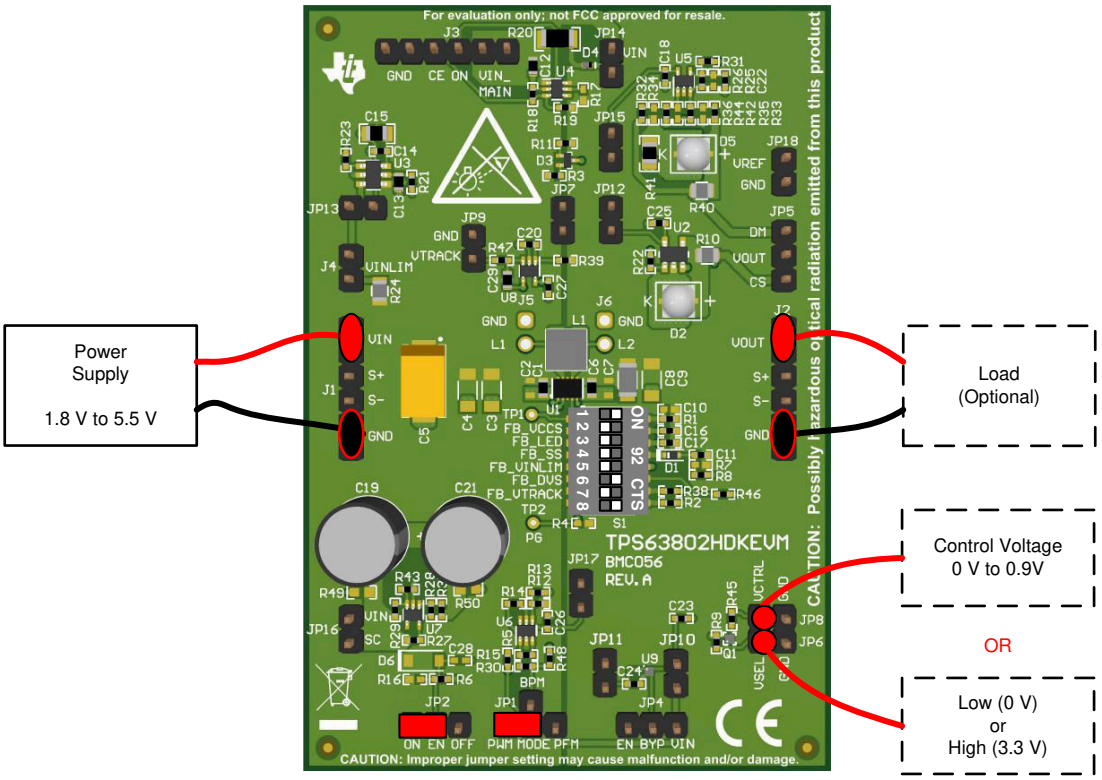

Figure 4-20. Quick Start Connection for Dynamic Voltage Scaling

Table 4-11. Configuration of the Jumpers for Dynamic Voltage Scaling

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set to 3.3 V.
	5, 6	GND	Connect the GND terminal of the power supply.

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Table 4-11. Configuration of the Jumpers for Dynamic Voltage Scaling (continued)

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.
JP1	2, 3	MODE, PWM	Place short between pin 2 and 3 to set TPS63802 to forced-PWM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
JP6	1, 2	GND, VSEL	2-level voltage selection: Connect a high (3.3 V) or low level (0 V) signal to pin 2. Do not connect JP8.(1)
JP8	1, 2	GND, VCTRL	Analog voltage control: Connect an analog control voltage between 0 V to 0.9 V. Do not connect JP6.(1)
All other JPx and Jx			Do not connect.
S1	Pos 1, Pos 6, and Pos 8		Set to ON.
	All other		Set to OFF.

(1) Use only one of the two functions and do not connect to the other Jumper.

4.7.2 Typical Performance

Figure 4-21 shows the typical performance of two-level voltage scaling. VOUT is equal to 3.3 V when VSEL is low and 5 V when VSEL is high.

Figure 4-22 shows the typical performance of analog dynamic voltage scaling. VOUT follows the external VCTRL signal with a certain factor.

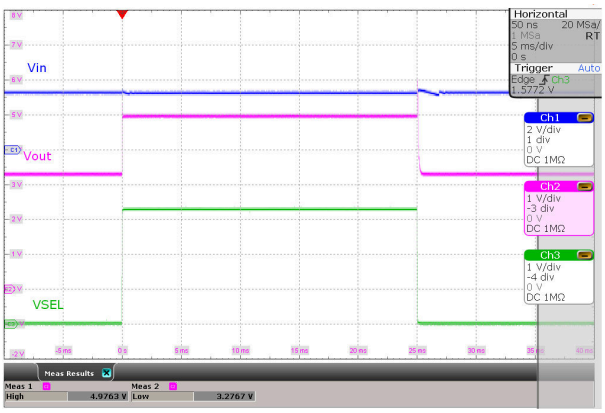

Figure 4-21. Typical Waveform of Two-level Voltage Scaling

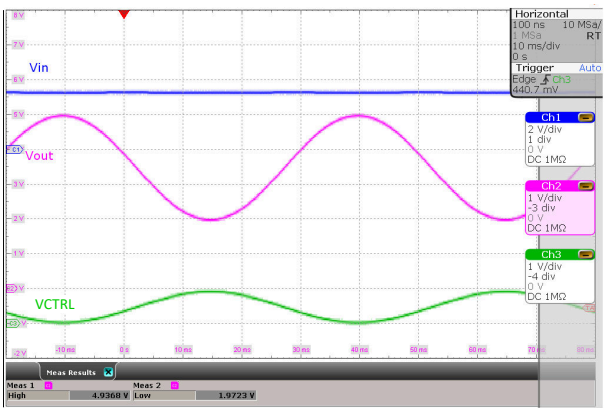

Figure 4-22. Typical Waveform of Analog Dynamic Voltage Scaling

Table 4-12. Recommendation for Dynamic Voltage Scaling Function

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
VIN		1.8	3.3	5.5	V
VOUT	Two-level voltage scaling VSEL = low		3.3		V
VOUT	Two-level voltage scaling VSEL = high		5.0		V
VCTRL	Analog dynamic voltage scaling	0		0.9	V

4.7.3 Design Guidance

This section shows how to modify the EVM components to support different output voltage levels.

4.7.3.1 Change the Vout Target for 2-Level Selection

In this case, there is a higher target and a lower target for output voltage.

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$$V_{LOW} = V_{FB} \times \frac{R1 + R2}{R2} \quad (12)$$

$$V_{High} = V_{FB} \times \frac{R1 + R_p}{R_p} \quad (13)$$

where

- R_p = R2 || R46

It is easier to design first the lower target voltage with R1 and R2. Then the high target can be calculated depending on R46.

4.7.3.2 Change the Vout Target for Analog Signal Control

In this case, the target of VOUT is determined by R1, R2, R46, and VCTRL.

$$R2 = -V_{FB} \times R1 \times \frac{V_{CTRLLOW} - V_{CTRLHI}}{(V_{OUTLOW} - V_{OUTHI} + V_{CTRLLOW} - V_{CTRLLHI}) \times V_{FB} - (V_{CTRLLOW} \times V_{OUTLOW}) + (V_{CTRLHI} \times V_{OUTHI})} \quad (14)$$

$$R46 = R2 \times R1 \times \frac{V_{CTRLHI} - V_{FB}}{(R2 \times V_{FB}) + (R1 \times V_{FB}) - (R2 \times V_{OUTLOW})} \quad (15)$$

A tool for calculating values of the resistor can be downloaded here: *Design Tool for Output Voltage Adjustment using a DAC*

4.7.4 Further Information

Further information on the specific application can be found in the following application reports:

- *Dynamically Adjustable Output Using TPS63000*
- *Methods of Output-voltage Adjustment for DC/DC Converters*
- *Design Tool for Output Voltage Adjustment using a DAC*

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4.8 Output Voltage Tracking

For some off-board sensors and modules, systems must take special consideration for their power supplies on both protection and output accuracy. In these systems, the power supply runs through a long cable from the main board. The system needs to implement a protection mechanism to protect on-board components from being damaged, while keeping the low voltage-tracking tolerance between the off-board and the main power supply. Figure 4-23 shows the block diagram for voltage tracking use case.

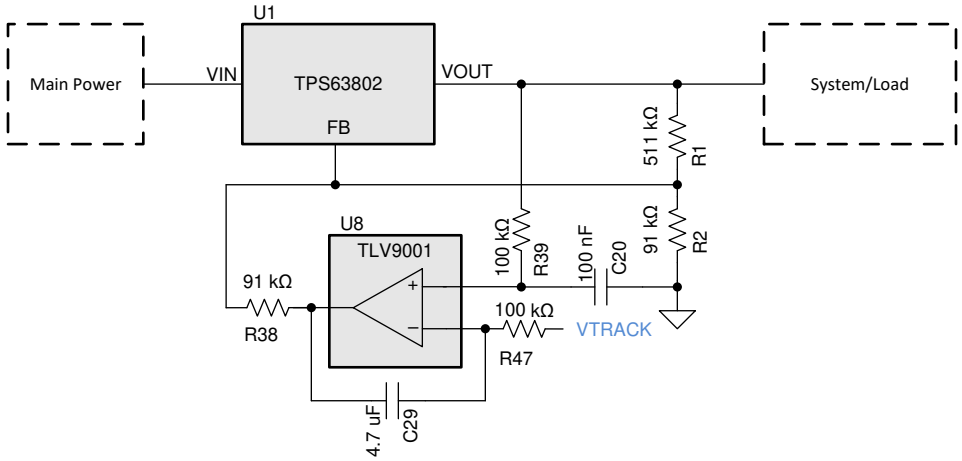

Figure 4-23. Block Diagram for Output Voltage Tracking

4.8.1 Setup

Figure 4-24 and Table 4-13 show the jumper and dip switch configuration.

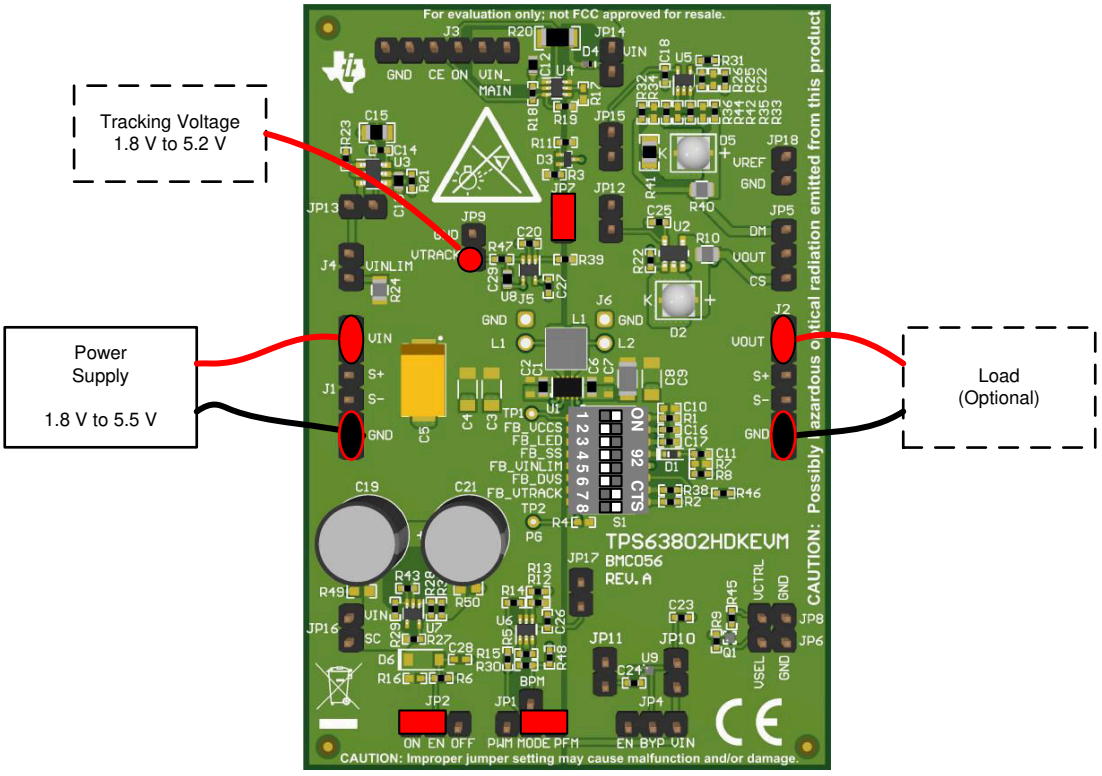

Figure 4-24. Quick Start Connection for Output Voltage Tracking

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Table 4-13. Configuration of the Jumpers for Output Voltage Tracking

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 selects PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 enables TPS63802.
JP7	1, 2		Place short to connect the power supply to U8.
JP9	1, 2	GND, VTRACK	Connect tracking voltage (1.8 V to 5.2 V) to set the output voltage.
All other JPx and Jx			Do not connect.
S1	Pos 1, Pos 7, and Pos 8		Set to ON.
	All other		Set to OFF.

4.8.2 Typical Performance

Figure 4-25 shows the default EVM performance of output voltage tracking. Here, VTRACK (green signal) is a sine wave with 2-V amplitude, 3-V offset, and 10-s period. The output voltage follows VTRACK with a slight phase shift.

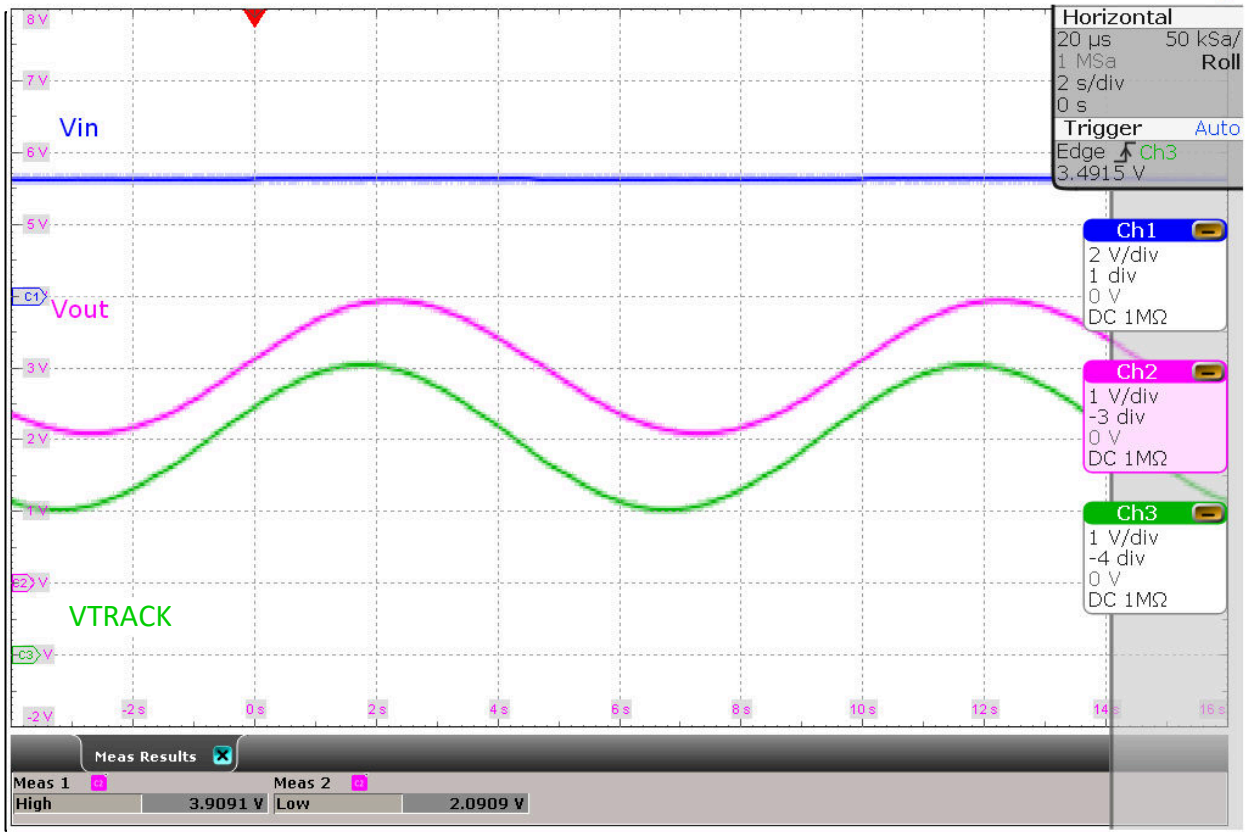

Figure 4-25. Typical Waveform for Output Voltage Tracking

4.8.3 Design Guidance

This section shows how to modify the EVM components to support different tracking speeds.

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4.8.3.1 Adjusting the Reaction Time

The operational amplifier U8 forms an integrator together with R47 and C29. Any difference between the output voltage of the TPS63802 and the reference voltage VTRACK is integrated and fed into the feedback node of the TPS63802 via R38. This is similar to dynamic voltage scaling, the difference is that there is an active feedback making sure that the output voltage is equal to VTRACK. Additionally, with an accurate reference voltage, the output voltage accuracy can be increased beyond the capabilities of the TPS63802.

To adjust the speed of the tracking, the integration constant can be changed by adjusting the values of R47 and C29. If necessary, the values of R39 and C20 that filter the VOUT must also be readjusted.

4.8.4 Further Information

Further information on the specific application can be found in this application report:

- *Various Applications for Voltage-Tracking LDO*

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4.9 Bypass Mode

With the high efficiency and the low Iq of 11 µA, the TPS63802 is suitable for energy saving applications. Some applications have an even lower standby current requirement that requires even lower Iq. This can be achieved by using a low Iq load switch in parallel to the TPS63802. The TPS63802 can then be shutdown during low load conditions. With the below parts, the shutdown current is only 45 nA. The system is supplied by the main power directly through the load switch at this time. This reduces the power loss and increases the system efficiency and runtime.

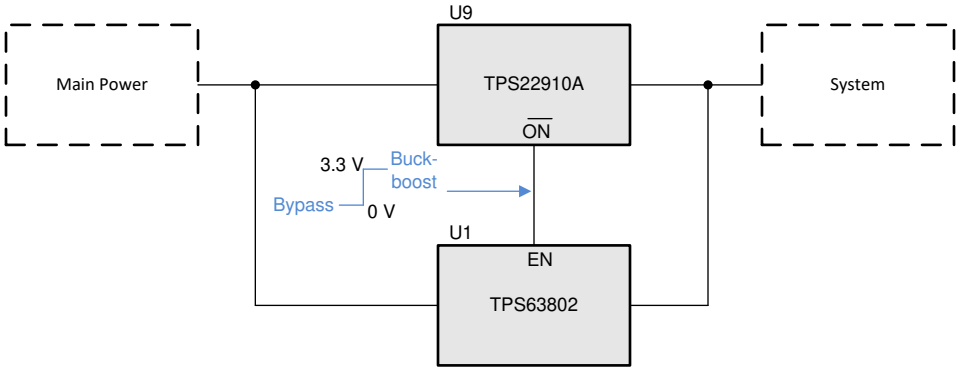

Figure 4-26. Block Diagram for Bypass Mode

4.9.1 Setup

Figure 4-27 and Table 4-14 show the jumper and dip switch configuration.

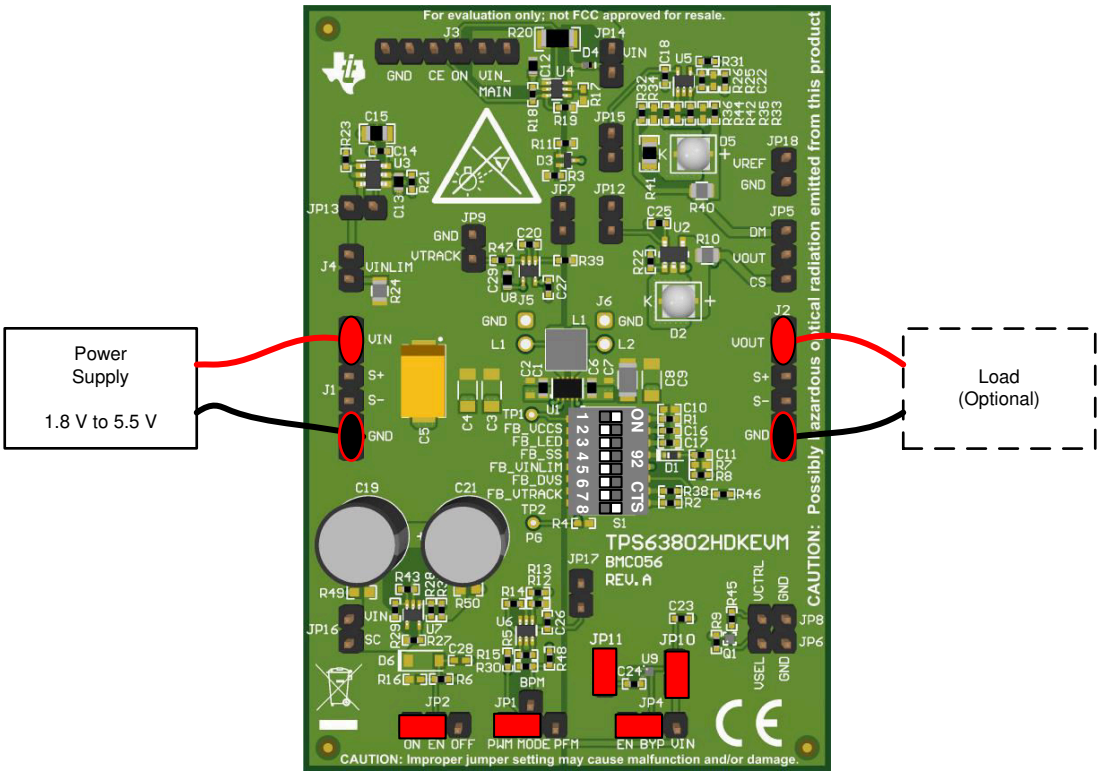

Figure 4-27. Quick Start Connection for Bypass Mode

Table 4-14. Configuration of the Jumpers for Bypass Mode

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.

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Table 4-14. Configuration of the Jumpers for Bypass Mode (continued)

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.
JP1	2, 3	MODE, PWM	Place short between pin 2 and 3 enables forced-PWM mode.
JP2	1, 2 or 2, 3	OFF, EN or EN, ON	Place short between pin 1 and 2 to enable bypass function (TPS63802 disabled). Place short between pin 2 and 3 to enable TPS63802.
JP4	1, 2	EN, BYP	Place short between pin 1 and 2 to enable U9.
JP10	1, 2		Place short to connect VIN to U9.
JP11	1, 2		Place short to connect U9 to VOUT.
All other JPx and Jx			Do not connect.
S1	Pos 1 and Pos 8		Set to ON.
	All other		Set to OFF.

4.9.2 Typical Performance

Figure 4-28 shows the transition from active to bypass mode when VIN is set to 2.5 V.

Figure 4-29 shows the transition from bypass to active mode.

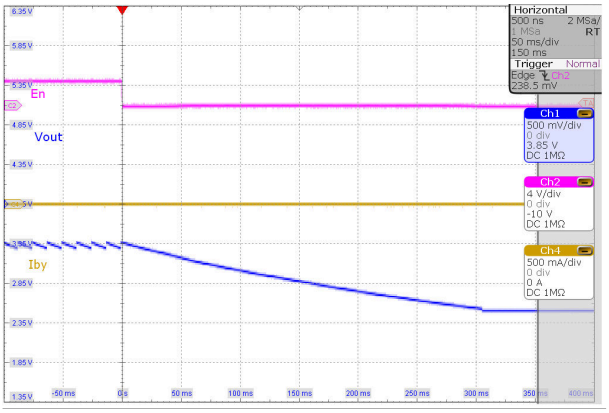

Figure 4-28. Typical Waveform for Bypass Entry

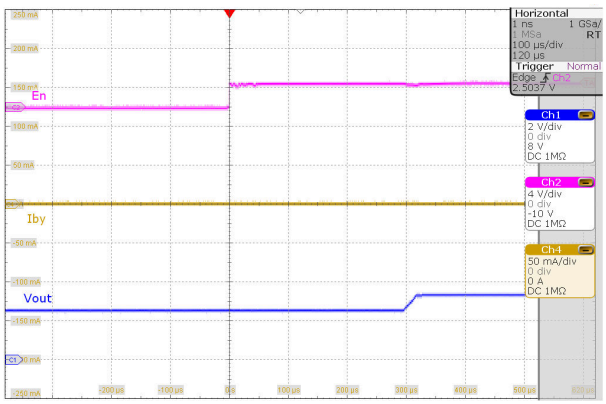

Figure 4-29. Typical Waveform for Bypass Exit

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4.10 Precise Start-up and Start-up Delay

Sometimes, a DC/DC converter needs to be started with a certain delay after the input voltage supply is provided. For example, some processors require specific power-up sequencing of different voltage domains. Another reason to use delayed start-up is to spread the inrush current peaks due to the start-up of multiple DC/DC converters.

In some battery applications, a precise undervoltage lockout is desirable to prevent damaging the battery by over discharge.

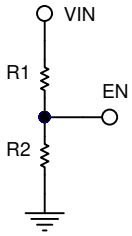

Figure 4-30. Block Diagram for Precise Start-up

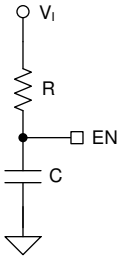

Figure 4-31. Block Diagram for Start-up Delay

4.10.1 Setup

Figure 4-32 and Table 4-15 show the jumper and dip switch configuration.

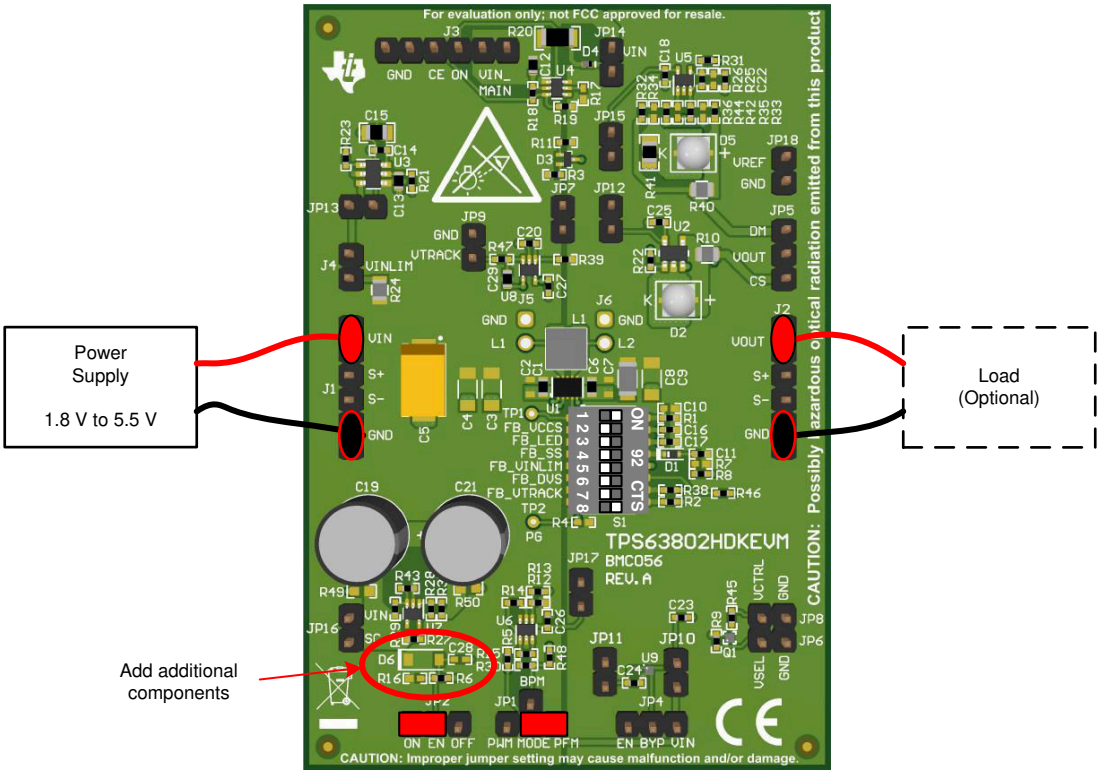

Figure 4-32. Quick Start Connection for Precise Start-up Delay

Table 4-15. Configuration of the Jumpers for Precise Start-up Delay

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
J1	1, 2	VIN	Connect the positive terminal of the power supply set between 1.8 V and 5.5 V.
	5, 6	GND	Connect the GND terminal of the power supply.
J2	1, 2	VOUT	Connect the positive terminal of the load.
	5, 6	GND	Connect the GND terminal of the Load.

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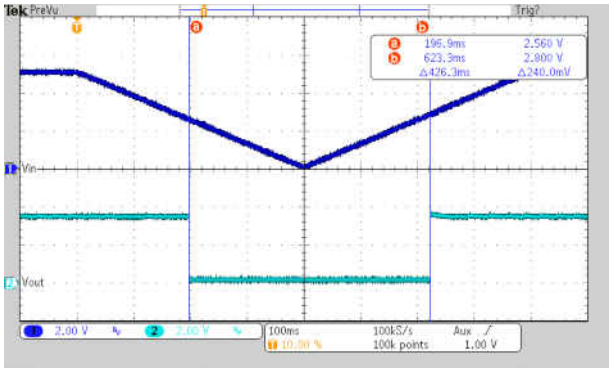
Table 4-15. Configuration of the Jumpers for Precise Start-up Delay (continued)

DESIGNATOR	PIN	PIN NAME	DESCRIPTION
JP1	1, 2	PFM, MODE	Place short between pin 1 and 2 to select PFM mode.
JP2	2, 3	EN, ON	Place short between pin 2 and 3 to enable TPS63802.
All other JPx and Jx			Do not connect.
S1	Pos 1 and Pos 8		Set to ON.
	All other		Set to OFF.
R6, R16, C28, D6			Additional components needs to be soldered.

4.10.2 Typical Performance

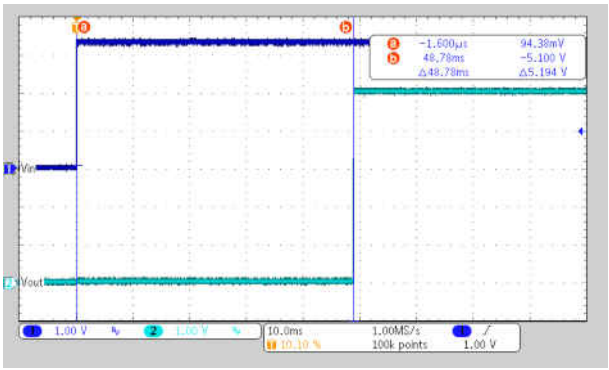
Figure 4-33 shows a precise disable and enable programmed to a specific level. The disable voltage level is at 2.5 V and the enable level is at 2.8 V for the given components.

Figure 4-34 shows a 48-ms delayed start-up.



A. R1 = 75 kΩ, R2 = 49.9 kΩ

Figure 4-33. Typical Waveform: Precise Start-up



A. R = 1.2 MΩ, C = 100 nF

Figure 4-34. Typical waveform: Start-up Delay

4.10.3 Design Guidance

This section shows how to modify the EVM components to support different cutoff values and delay times.

4.10.3.1 Change the Cutoff Value

Equation 16 calculates the falling threshold supply voltage where the converter is turned off:

$$V_{IT-} = V_{IT-(EN)} \left(1 + \frac{R1}{R2}\right) \quad (16)$$

Equation 17 calculates the rising threshold supply voltage where the converter is turned on:

$$V_{IT+} = V_{IT+(EN)} \left(1 + \frac{R1}{R2}\right) \quad (17)$$

4.10.3.2 Change the Delay Time

If the threshold voltage of the EN pin $V_{TH;EN}$ is known for the device, use Equation 18 to calculate the start-up delay t_d.

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$$t_d = R \cdot C \cdot \ln\left(\frac{V_I}{V_I - V_{TH;EN}}\right) \quad (18)$$

4.10.4 Further Information

Further information on the specific application can be found in these application reports:

- *Precise Start-Up Delay Using Enable Pin with Precise Voltage Threshold*
- *Prevent Battery Over discharge with Precise Threshold Enable Pin*

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5 Board Layout

This section provides the TPS63802HDKEVM board layout.

5.1 Layout

Figure 5-1 through Figure 5-4 show the board layout for the TPS63802HDKEVM printed circuit board (PCB).

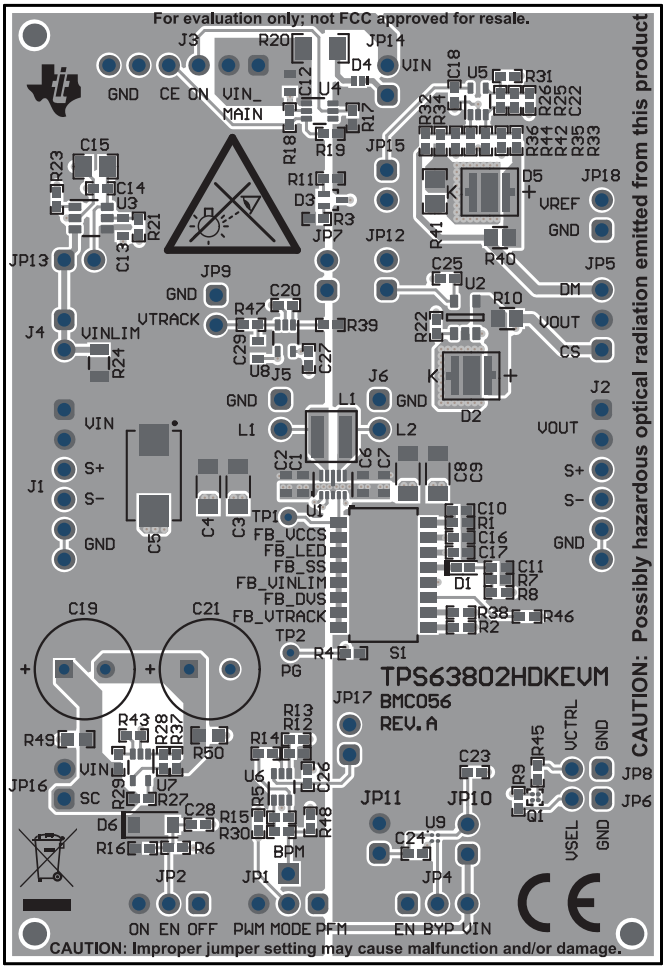

Figure 5-1. Assembly Layer

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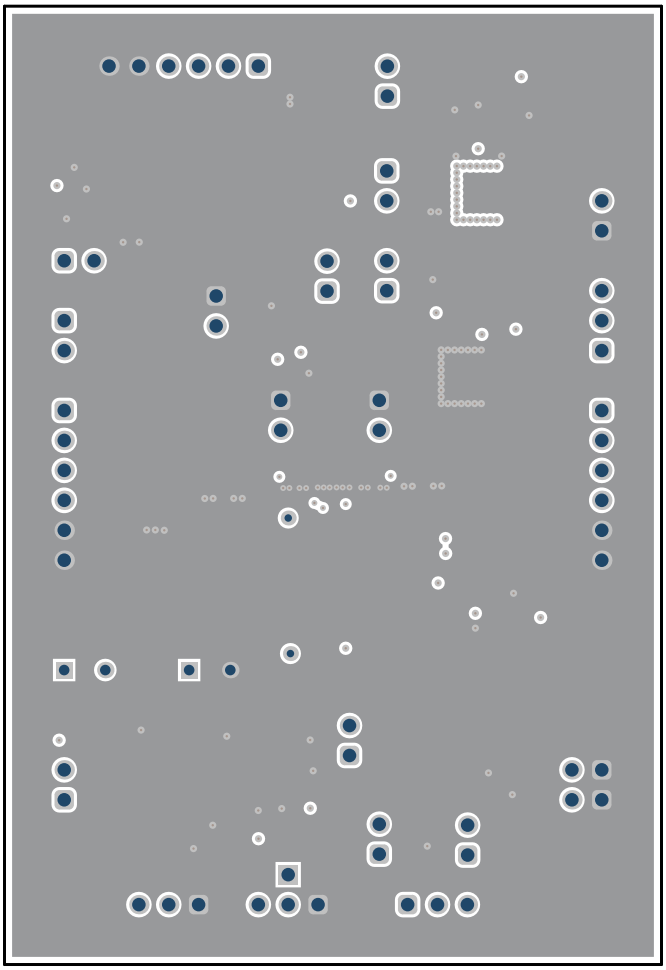

Figure 5-2. Signal Layer 1

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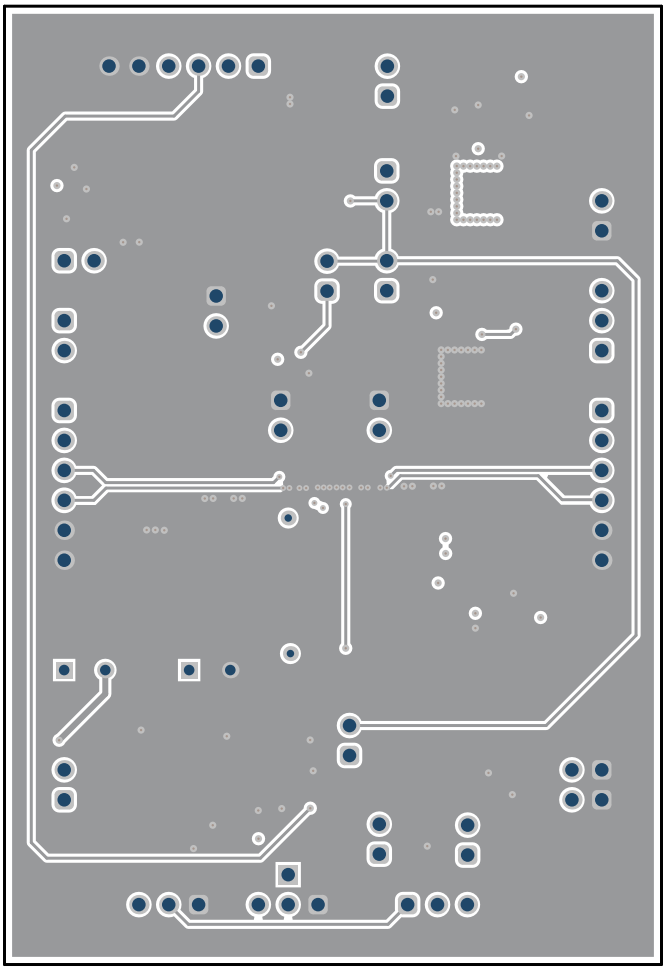

Figure 5-3. Signal Layer 2

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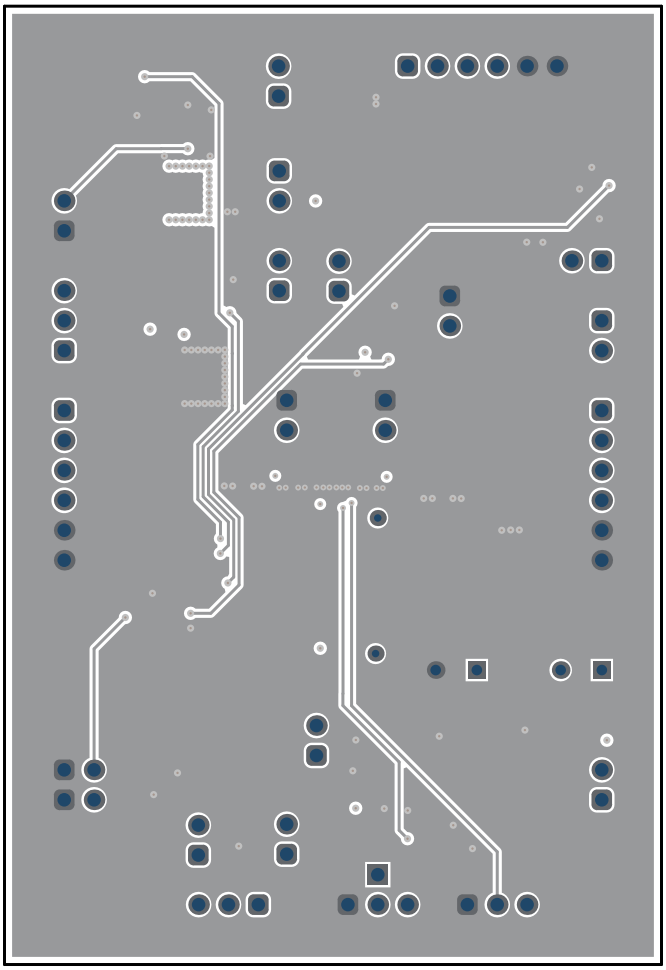

Figure 5-4. Bottom Layer Routing (Mirrored)

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6 Schematic and Bill of Materials

This section provides the TPS63802HDKEVM schematic and bill of materials.

6.1 Schematic

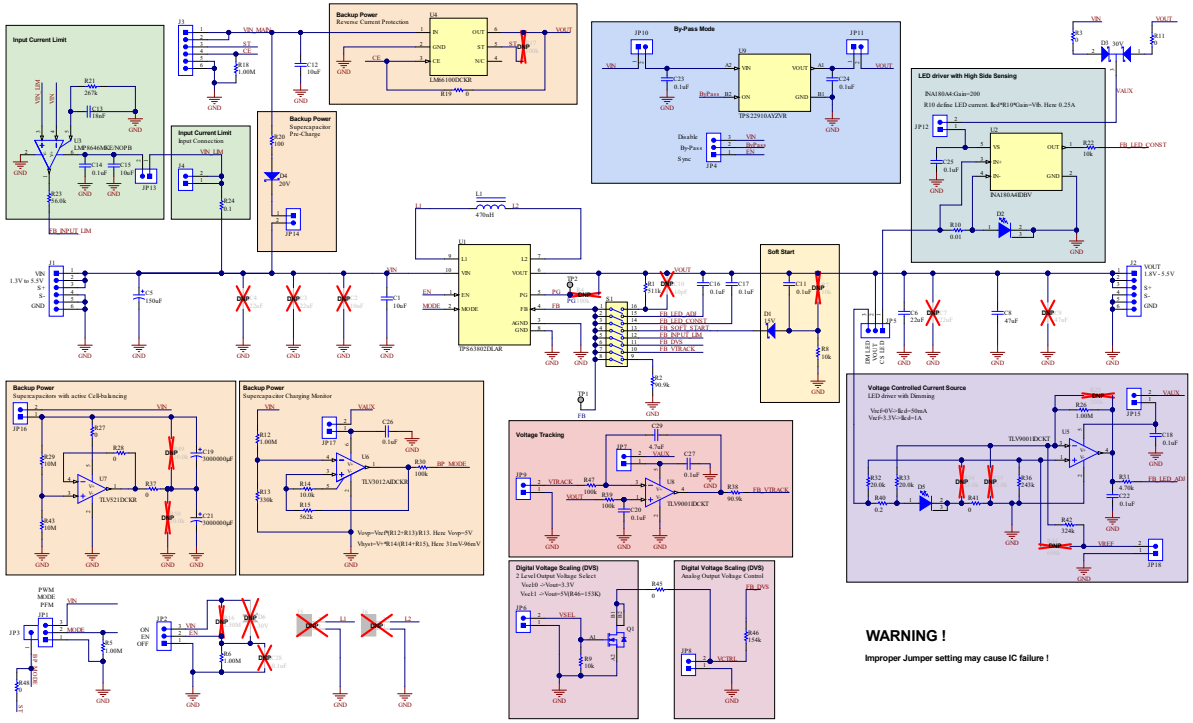

Figure 6-1. Schematic

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6.2 Bill of Materials

Table 6-1. Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1	1	10 µF	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J106ME47D	MuRata
C5	1	150 µF	CAP, Tantalum Polymer, 150 µF, 10 V, ±20%, 0.005 Ω, 7343-31 SMD	7343-31	T530D157M010ATE005	Kemet
C6	1	22 µF	CAP, CERM, 22 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J226MEA0D	MuRata
C8	1	47 µF	CAP, CERM, 47 µF, 10 V, ±20%, X5R, 1206_190	1206_190	LMK316ABJ476ML-T	Taiyo Yuden
C11, C14, C16, C17, C18, C20, C22, C23, C24, C25, C26, C27	12	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0402	0402	GCM155R71H104KE02D	MuRata
C12	1	10 µF	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J106ME84	MuRata
C13	1	0.018 µF	CAP, CERM, 0.018 µF, 100 V, ±10%, X7R, 0603	0603	C0603C183K1RACTU	Kemet
C15	1	10 µF	CAP, CERM, 10 µF, 25 V, ±20%, X7S, 0805	0805	GRM21BC71E106ME11L	MuRata
C19, C21	2	3000000 µF	CAP, Electric Double Layer, 3000000 µF, 2.7 V, +20/-10%, 0.07 Ω, AEC-Q200 Grade 4, TH	TH, 2-Leads, 8mm Dia, 20 mm Height	BCAP0003 P270 S01	Maxwell Technologies
C29	1	4.7 µF	CAP, CERM, 4.7 µF, 16 V, ±10%, X5R, 0603	0603	GRM188R61C475KAAJ	MuRata
D1	1	15 V	Diode, Schottky, 15 V, 0.2 A, SOD-523	SOD-523	DB2S20500L	Panasonic
D2, D5	2	White	LED, White, SMD	LED, 3.45x3.45 mm	XPLAWT-00-0000-000BV20E3	Cree
D3	1	30 V	Diode, Schottky, 30 V, 0.2 A, SOT-523	SOT-523	BAT54CT-7-F	Diodes Inc.
D4	1	20 V	Diode, Schottky, 20 V, 0.5 A, SOD882	SOD882	PMEG2005EL,315	Nexperia
J1, J2, J3	3		Header, 2.54 mm, 6x1, Gold, TH	Header, 2.54 mm, 6x1, TH	61300611121	Wurth Elektronik
J4, JP6, JP7, JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18	14		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54 mm, 2x1, TH	61300211121	Wurth Elektronik
JP1, JP2, JP4, JP5	4		Header, 2.54 mm, 3x1, Gold, TH	Header, 2.54 mm, 3x1, TH	61300311121	Wurth Elektronik
JP3	1		Header, 2.54 mm, 1x1, Gold, TH	Header, 2.54 mm, 1x1, TH	61300111121	Wurth Elektronik
L1	1	470 nH	Inductor, Shielded, Composite, 470 nH, 3.5 A, 0.0076 Ω, SMD	SMD, 4x4x1.5 mm	XFL4015-471MEC	Coilcraft
Q1	1	12 V	MOSFET, N-CH, 12 V, 1.6 A, YZB0004AEAE (DSBGA-4)	YZB0004AEAE	CSD13302W	Texas Instruments
R1	1	511 k	RES, 511 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402511KFKED	Vishay-Dale
R2, R38	2	90.9 k	RES, 90.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF9092X	Panasonic
R3, R11, R19, R27, R28, R37, R45, R48	8	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R5, R6, R18, R26	4	1.00 Meg	RES, 1.00 M, 1%, 0.063 W, 0402	0402	RC0402FR-071ML	Yageo America
R8, R9	2	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R10	1	0.01	RES, 0.01, 1%, 0.25 W, AEC-Q200 Grade 0, 0805	0805	WSL0805R0100FEA18	Vishay-Dale
R12	1	1.00 Meg	RES, 1.00 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021M00FKED	Vishay-Dale
R13	1	330 k	RES, 330 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07330KL	Yageo America
R14	1	10.0 k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RMCF0402FT10K0	Stackpole Electronics Inc
R15	1	562 k	RES, 562 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402562KFKED	Vishay-Dale
R20	1	100	RES, 100, 1%, 0.5 W, AEC-Q200 Grade 0, 1206	1206	CRCW1206100RFKEAHP	Vishay-Dale
R21	1	267 k	RES, 267 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF2673X	Panasonic
R22	1	10 k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R23	1	56.0 k	RES, 56.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	RK73H1ETTP5602F	KOA Speer
R24	1	0.1	RES, 0.1, 1%, .5 W, AEC-Q200 Grade 0, 0805	0805	KRL1220E-M-R100-F-T5	Susumu Co Lentry
R29, R43	2	10 Meg	RES, 10 M, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210M0JNED	Vishay-Dale
R30, R39, R47	3	100 k	RES, 100 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1003X	Panasonic
R31	1	4.70 k	RES, 4.70 k, 1%, 0.063 W, 0402	0402	CRG0402F4K7	TE Connectivity
R32, R33	2	20.0 k	RES, 20.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040220K0FKED	Vishay-Dale
R36	1	243 k	RES, 243 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF2433X	Panasonic
R40	1	0.2	RES, 0.2, 1%, 0.25 W, AEC-Q200 Grade 0, 0805	0805	WSL0805R2000FEA18	Vishay-Dale
R41	1	0	RES, 0, 5%, 0.333 W, AEC-Q200 Grade 0, 0805	0805	CRCW08050000Z0EAHP	Vishay-Dale

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Table 6-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R42	1	324 k	RES, 324 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402324KFKED	Vishay-Dale
R46	1	154 k	RES, 154 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1543X	Panasonic
S1	1		Switch, SPST, 8 Pos, 25 mA, 24VDC, SMD	11.33x5.8 mm	218-8LPST	CTS Electrocomponents
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5	5	1x2	Shunt, 100 mil, Flash Gold, Black	Closed Top 100 mil Shunt	SPC02SYAN	Sullins Connector Solutions
U1	1		High Current, High Efficiency Single Inductor Buck-Boost Converter, DLA0010A (VSON-HR-10)	DLA0010A	TPS63802DLAR	Texas Instruments
U2	1		Low- and High-Side Measurement, Multichannel, Voltage Output, Current-Sense Amplifier, DBV0005A (SOT-5)	DBV0005A	INA180A4IDBV	Texas Instruments
U3	1		76-V, Configurable Gain and Bandwidth, Low- or High-Side, High-Speed, Current Limiter, DDC0006A (SOT-23-T-6)	DDC0006A	LMP8646MKE/NOPB	Texas Instruments
U4	1		±6 V, Low IQ Ideal Diode with Input Polarity Protection, DCK0006A (SOT-SC70-6)	DCK0006A	LM66100DCKR	Texas Instruments
U5, U8	2		Low-Power, Rail-to-Rail In and Out, 1-MHz Operational Amplifier, DCK0005A (SOT-SC70-5)	DCK0005A	TLV9001IDCKT	Texas Instruments
U6	1		Nanopower, 1.8 V, SOT23 Push-Pull Comparator with Voltage Reference, DCK0006A (SOT-SC70-6)	DCK0006A	TLV3012AIDCKR	Texas Instruments
U7	1		350-nA Nanopower, Single, RRIO, CMOS Input, Operational Amplifier for Cost-Sensitive Systems, DCK0005A (SOT-SC70-5)	DCK0005A	TLV521DCKR	Texas Instruments
U9	1		5.5 V, 2 A, 61 mΩ Active-Low Load Switch With Reverse Current Protection, YZV0004ADAD (DSBGA-4)	YZV0004ADAD	TPS22910AYZVR	Texas Instruments
C2	0	10 µF	CAP, CERM, 10 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J106ME84	MuRata
C3, C4	0	22 µF	CAP, CERM, 22 µF, 25 V, ±20%, X5R, 1206_190	1206_190	TMK316BBJ226ML-T	Taiyo Yuden
C7	0	22 µF	CAP, CERM, 22 µF, 6.3 V, ±20%, X5R, 0603	0603	GRM188R60J226MEA0D	MuRata
C9	0	47 µF	CAP, CERM, 47 µF, 10 V, ±20%, X5R, 1206_190	1206_190	LMK316ABJ476ML-T	Taiyo Yuden
C10	0	10 pF	CAP, CERM, 10 pF, 16 V, ±10%, C0G, 0402	0402	C0402C100K4GACTU	Kemet
C28	0	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0402	0402	GCM155R71H104KE02D	MuRata
D6	0	30 V	Diode, Schottky, 30 V, 0.2 A, SOD-123	SOD-123	BAT54T1G	ON Semiconductor
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J5, J6	0		Header, 2.54 mm, 2x1, Gold, TH	Header, 2.54mm, 2x1, TH	61300211121	Wurth Elektronik
R4, R17	0	100 k	RES, 100 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1003X	Panasonic
R7	0	10 k	RES, 10.0 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF1002X	Panasonic
R16	0	1.50 Meg	RES, 1.50 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021M50FKED	Vishay-Dale
R25	0	200 k	RES, 200 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402200KFKED	Vishay-Dale
R34, R35	0	33.0 k	RES, 33.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0733KL	Yageo America
R44	0	698 k	RES, 698 k, 1%, .1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF6983X	Panasonic
R49, R50	0	10.0 k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2020) to Revision A (June 2021) **Page**

- Updated the numbering format for tables, figures and cross-references throughout the document.....3

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