

DRV8343x-Q1EVM Independent Mode User's Guide

This document is provided with the DRV8343x-Q1EVM customer evaluation module (EVM) as a supplement to the *DRV8343-Q1 Automotive 5.5 to 60-V Three-Phase Smart Gate Driver With Three Integrated Current-Shunt Amplifiers* data sheet and the *DRV8343H-Q1EVM and DRV8343S-Q1EVM User's Guide* to describe the functionality of the independent mode settings used on the DRV8343x-Q1EVM. This user's guide details how to configure the DRV8343x-Q1EVM board according to the independent mode selected and how the GUI operates under the selected mode.

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TEXAS INSTRUMENTS

Overview

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1 Overview

The DRV8343x-Q1EVM is highly configurable, featuring five different independent inputs modes to drive one phase BDC motors, multiple loads such as solenoids, or both. The five different modes are listed as follows:

- All phases are in independent half-bridge PWM mode
- Phase A and phase B are in independent half-bridge mode and phase C is in independent FET mode (SPI version only)
- Phase B and phase C are in independent half-bridge mode and phase A is in independent FET mode
- Phase A is in independent half-bridge mode, phase B and phase C are in independent FET mode
- All phases are in independent MOSFET drive mode

For more information on these modes, refer to the *DRV8343-Q1 Automotive 5.5 to 60-V Three-Phase Smart Gate Driver With Three Integrated Current-Shunt Amplifiers* data sheet.

2 Multiple Board Configurations

2.1 Half Bridge Configuration

For independent half-bridge mode, two different configurations can be made for the each half-bridge. Both the high-side and low-side switches are complimentary in this mode and each half-bridge can be configured as either an active-high load or an active-low load.

2.1.1 Active-High Side Driver

In active-high side driver configuration, the load is connected across the low-side FET for active current recirculation as shown in Figure 1. In this mode the voltage across the load is controlled by modulating the duty cycle of the high-side FET. Current flows from the supply to the load when the high-side FET is ON. When the high-side FET is OFF, the low-side FET is turned ON and current recirculates through the low-side FET.



Figure 1. Half-Bridge Active-High Configuration

If the half-bridge is used as previously described, no EVM modifications are required. Considering the load in use, an external diode might be required to recirculate the current. Depending on the half-bridge being configured, the D10, D11, or D12 diode can be populated.



Multiple Board Configurations

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2.1.2 Active-Low Side Driver

In active-low side driver configuration, the load is connected across the high-side FET for active current recirculation as shown in Figure 2. In this mode the voltage across the load is controlled by modulating the duty cycle of the low-side FET. Current flows from the supply to the load when the low-side FET is ON. When the low-side FET is OFF, the high-side FET is turned ON and current recirculates through the high-side FET.



Figure 2. Half-Bridge Active-Low Configuration

If the half-bridge is used as previously described, no EVM modifications are required. Considering the load in use, an external diode might be required to recirculate the current. Depending on the half-bridge being configured, the D13, D14, or D15 diode can be populated.

2.2 Independent FET Configuration

For independent FET mode, three different configurations can be made, which are high-side load, low-side load, and load between the FETs.

2.2.1 High Side

In this configuration, the load is connected between the source of the high-side FET and the ground with a diode across the load for current recirculation as shown in Figure 3. In this mode the voltage across the load is controlled by modulating the duty cycle of the high-side FET. The current flows through the load only when the high-side FET is ON.



Figure 3. Independent FET—High Side



- To use the configuration in Figure 3, follow these steps:
 - Step 1. Install the D10, D11, D12, or all three diodes, depending on which high-side FET will be driven (see Figure 4).



Figure 4. High-Side Diodes

Step 2. Remove the connector between the SHx and DLx output connections, F5, F6, F7, or all three (see Figure 5).



Figure 5. Remove Jumper Connectors



2.2.2 Low Side

In this configuration, the load is connected between the VCC supply and the drain of the low-side FET with a diode across the load for current recirculation as shown in Figure 6. In this mode the voltage across the load is controlled by modulating the duty cycle of the low-side FET. Current flows through the load only when the low-side FET is ON.



Figure 6. Independent FET—Low Side

To use the configuration in Figure 6, follow these steps:

1. Install the D13, D14, D15, or all three diodes, depending on which low-side FET will be driven (see Figure 7).



Figure 7. Low-Side Diodes

2. Remove the connector between the SHx and DLx output connections, F5, F6, F7, or all three (see Figure 8).



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Figure 8. Remove Jumper Connectors

2.2.3 Load Between FETs

In this configuration, the load is connected between the source of the high-side FET and drain of the lowside FET with a diode across the load for current recirculation as shown in Figure 9. In this mode the voltage across the load is controlled by modulating the duty cycle of both the high-side and low-side FET. Current flows through the load only when both of the FETs are ON.



Figure 9. Independent FET—Load Between FETs

To use the configuration in Figure 9, follow these steps:

Step 1. Install the D7, D8, D9, or all three middle load diodes, depending on which phase will be





Figure 10. Load Between FETs Diodes

Step 2. Remove the connector between the SHx and DLx output connections, F5, F6, F7, or all three (see Figure 11).



Figure 11. Remove Jumper Connectors



CAUTION

Verify the connections are installed as intended because having the incorrect setup when selecting a mode of operation in the EVM can permanently damage the board.

3 Customizing the Reference Code

The reference code is provided as a Code Composer Studio[™] software project and an evaluation GUI.

The DRV8343x-Q1EVM GUI is a user interface (UI) to run and tune the motor on the DRV8343x-Q1EVM with the DRV8343-Q1_EVM_BLDC_FW software.

The user must install the DRV8343x-Q1EVM GUI to run and modify the run time values of the parameters for the independent algorithm and also to select the configuration in which loads are connected across the bridges.

The user must download the Code Composer Studio software 6.1.0 or above and install the DRV8343_EVM_BLDC_FW firmware.

The user must import the DRV8343_MSP430F5529_Independent_Drive project into the Code Composer Studio integrated development environment (IDE). The *Active Build* option from the *Build Configuration* should be set as *Debug*.

To modifying some parameters for sensorless control, follow these steps:

- 1. Open the Code Composer Studio software.
- Import the project, DRV8343_MSP430F5529_Independent_Drive, from the folder where the demo software is located.
- 3. Select the file, *Independent_Parameters_Setup.h.* This folder contains most of the parameters used to run this application code. Some parameters require modifications to correctly tune for different operating conditions. The sections that follow describe the parameters and the details in which they can be modified.

3.1 Customizing the System Parameters

The code for the system parameters is as follows:

//System Parameters

/* System parameter setup */

```
#define PWM_PERIOD (1000)
                                                 /* PWM Period time , With a 25Mhz clock , PWM
will be generated at 25Khz*/
#define READ_VCC_PERIOD (100)
                                                 /* TIME INTERVAL AFTER WHICH VCC IS MONITORED
(100ms) */
#define RAMP_RATE_DELAY_HA (100)
                                                 /* How many PWM periods are between a change of
the speed */
#define RAMP_RATE_DELAY_HB (100)
                                                 /* How many PWM periods are between a change of
the speed */
#define RAMP_RATE_DELAY_HC (100)
                                                 /* How many PWM periods are between a change of
the speed */
#define RAMP_RATE_DELAY_LA (100)
                                                 /* How many PWM periods are between a change of
the speed */
#define RAMP_RATE_DELAY_LB (100)
                                                 /* How many PWM periods are between a change of
the speed */
#define RAMP_RATE_DELAY_LC (100)
                                                 /* How many PWM periods are between a change of
the speed */
```

3.1.1 PWM_PERIOD

The PWM_PERIOD value sets the frequency of the PWM pulse train used in switching the FETs. The PWM frequency is calculated as the ratio of MCLK to PWM_PERIOD. As the master clock operates at 25 MHz, if the PWM_PERIOD is 1024, then PWM frequency is approximately 25 KHz (40 μ s). This value is also the maximum comparator value that can be loaded which sets the duty cycle. This parameter can be configured using the GUI widget for the PWM switching frequency.

3.1.2 READ_VCC_PERIOD

The READ_VCC_PERIOD value sets the time in milliseconds after which the supply voltage is periodically monitored for any voltage faults. This parameter cannot be configured through the GUI widget.

3.1.3 RAMP RATE DELAY HA

The RAMP_RATE_DELAY_HA parameter sets how many PWM_PERIOD interrupts must occur before adjusting the duty cycle. Changing this value changes how fast the duty cycle is adjusted. For example, if the PWM_PERIOD is 1024 or 40.96 µs and the RAMP_RATE_DELAY is 24, the duty cycle is adjusted every 983 µs. This parameter controls the acceleration and deceleration of the motor. When phase A is configured for independent half-bridge control, this parameter controls the ramp rate of the both the high-side and low-side switches. When configured for independent FET mode, this parameter controls only the ramp rate of the phase A high side. This parameter can be configured using the GUI widget for the ramp rate in the bridge configuration tab.

3.1.4 RAMP RATE DELAY HB

The RAMP_RATE_DELAY_HB parameter sets how many PWM_PERIOD interrupts must occur before adjusting the duty cycle. Changing this value changes how fast the duty cycle is adjusted. For example, if the PWM_PERIOD is 1024 or 40.96 µs and the RAMP_RATE_DELAY is 24, the duty cycle is adjusted every 983 µs. This parameter controls the acceleration and deceleration of the motor. When phase A is configured for independent half-bridge control, this parameter controls the ramp rate of the both the high-side and low-side switches. When configured for independent FET mode, this parameter controls only the ramp rate of the phase B high side. This parameter can be configured using the GUI widget for the ramp rate in the bridge configuration tab.

3.1.5 RAMP RATE DELAY HC

The RAMP_RATE_DELAY_HC parameter sets how many PWM_PERIOD interrupts must occur before adjusting the duty cycle. Changing this value changes how fast the duty cycle is adjusted. For example, if the PWM_PERIOD is 1024 or 40.96 µs and the RAMP_RATE_DELAY is 24, the duty cycle is adjusted every 983 µs. This parameter controls the acceleration and deceleration of the motor. When phase C is configured for independent half-bridge control, this parameter controls the ramp rate of the both the high-side and low-side switches. When configured for independent FET mode, this parameter controls only the ramp rate of the phase C high side. This parameter can be configured using the GUI widget for the ramp rate in the bridge configuration tab.

3.1.6 RAMP RATE DELAY LA

The RAMP_RATE_DELAY_LA parameter sets how many PWM_PERIOD interrupts must occur before adjusting the duty cycle. Changing this value changes how fast the duty cycle is adjusted. For example, if the PWM_PERIOD is 1024 or 40.96 µs and the RAMP_RATE_DELAY is 24, the duty cycle is adjusted every 983 µs. This parameter controls the acceleration and deceleration of the motor. When phase A is configured for independent half-bridge control, this parameter does not impact the control of load. When configured for independent FET mode, this parameter controls only the ramp rate of the phase A low side. This parameter can be configured using the GUI widget for the ramp rate in the bridge configuration tab.



3.1.7 RAMP RATE DELAY LB

The RAMP_RATE_DELAY_LB parameter sets how many PWM_PERIOD interrupts must occur before adjusting the duty cycle. Changing this value changes how fast the duty cycle is adjusted. For example, if the PWM_PERIOD is 1024 or 40.96 µs and the RAMP_RATE_DELAY is 24, the duty cycle is adjusted every 983 µs. This parameter controls the acceleration and deceleration of the motor. When phase B is configured for independent half-bridge control, this parameter does not impact the control of load. When configured for independent FET mode, this parameter controls only the ramp rate of the phase B low side. This parameter can be configured using the GUI widget for the ramp rate in the bridge configuration tab.

3.1.8 RAMP RATE DELAY LC

The RAMP_RATE_DELAY_LC parameter sets how many PWM_PERIOD interrupts must occur before adjusting the duty cycle. Changing this value changes how fast the duty cycle is adjusted. For example, if the PWM_PERIOD is 1024 or 40.96 µs and the RAMP_RATE_DELAY is 24, the duty cycle is adjusted every 983 µs. This parameter controls the acceleration and deceleration of the motor. When phase C is configured for independent half-bridge control, this parameter does not impact the control of load. When configured for independent FET mode, this parameter controls only the ramp rate of the phase C low side. This parameter can be configured using the GUI widget for the ramp rate in the bridge configuration tab.

3.2 Customizing SPI REGISTER User Parameters

For the DRV8343-Q1 device, set the SPI register settings according to the *DRV8343-Q1 Automotive 5.5* to 60-V Three-Phase Smart Gate Driver With Three Integrated Current-Shunt Amplifiers data sheet. Modify the register settings using the register page found in the GUI (see Figure 12).

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حمل	IC1 Control	0x4	0x0	0	0	0	0	0	0	0	0	GDE
¥52	IC2 Control	0x5	0x40	0	1	0	0	0	0	0	0	GDF
(Z	IC3 Control	0x6	Oxff	1	1	1	1	1	1	1	1	DRV8343 / FAULT Status / CPUV
	IC4 Control	0x7	Oxff	1	1	1	1	1	1	1	1	CPIN
JE .	IC5 Control	0x8	Oxff	1	1	1	1	1	1	1	1	CFUV
÷	IC6 Control	0x9	0x99	1	0	0	1	1	0	0	1	DRV8343 / FAULT Status / UVLO
	IC7 Control	0xA	0x99	1	0	0	1	1	0	0	1	
	IC8 Control	0xB	0x99	1	0	0	1	1	0	0	1	
	IC9 Control	0xC	0x2f	0	0	1	0	1	1	1	1	DRV8343 / FAULT Status / OCP
	IC10 Control	0xD	0x61	0	1	1	0	0	0	0	1	000
	IC11 Control	0xE	0x0	-	0	0	0	0	0	0	0	- OCF
	IC12 Control	0×F	0x2a	0	0	1	0	1	0	1	0	DRV8343 / FAULT Status / OTW
	IC13 Control	0x10	0x7f	0	1	1	1	1	1	1	1	
	IC14 Control	0x11	0x0	-	-	0	0	0	0	0	0	• 01W
	IC15 Control	0x12	0x0	-	-	-	-	-	-	-	-	DRV8343 / FAULT Status / OTSD
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4 Running the Project in Code Composer Studio

To run the project in CCS, perform the steps that follow:

- 1. Install CCS software V6.1 or above.
- 2. Read through how to customize user parameters to tune the control for the specific motor.
- 3. Compile the modified project.

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