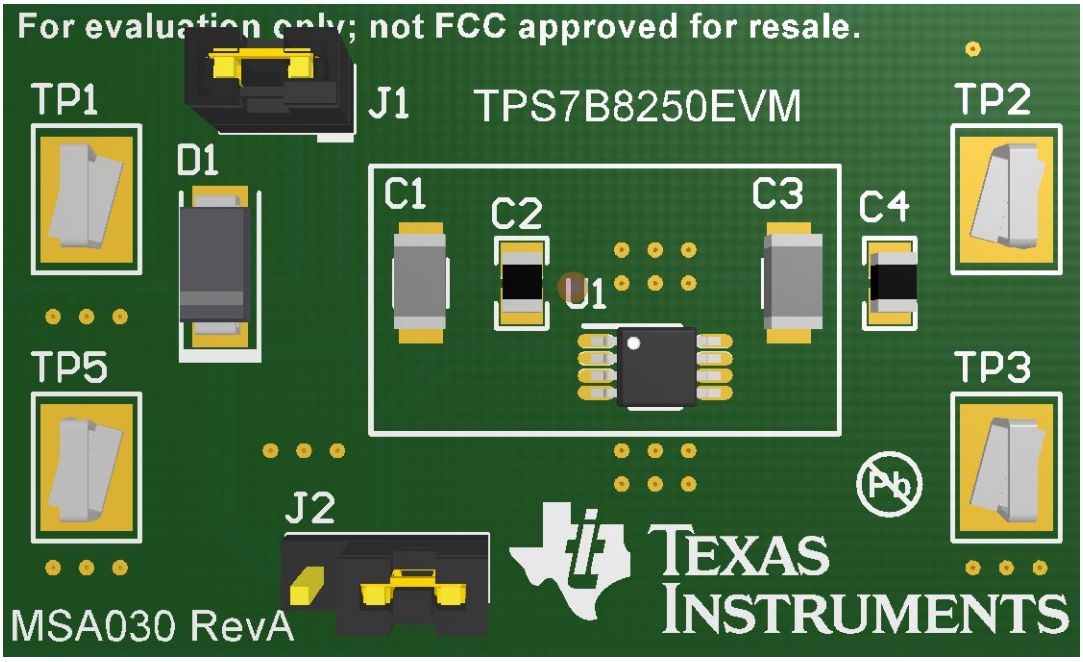
TPS7B8250EVM



This user's guide describes operational use of the TPS7B8250 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7B82-Q1 low-dropout (LDO) linear regulator. Included in this user's guide are setup instructions, a schematic diagram, printed circuit board (PCB) layout, and a bill of materials (BOM).

Throughout this document, the terms demonstration kit, evaluation board, and evaluation module are synonymous with the TPS7B8250EVM.

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1 Introduction

The TPS7B8250EVM helps engineers evaluate the operation and performance of the TPS7B82-Q1 linear regulator. The TPS7B82-Q1 device is an LDO linear regulator designed for up to a 40-V V_{IN} with a maximum 300-mA output current.

2 Hardware

2.1 Input/Output Connectors

TP1 (VIN) —This connector is the input of the EVM. TP1 allows the user to connect a power supply and measure the input voltage.

TP2 (VOUT) —This connector is the output of the EVM. TP2 allows the user to connect a load and measure the output voltage of the EVM.

TP3 (GND) and TP5 (GND) —These connectors are the ground return connector of the EVM. The EVM provides two GND test points to allow the user to power the EVM, connect the load, and link the oscilloscope ground.

2.2 Hardware Setup

The following steps show how to set up the hardware:

1. Verify that the output voltage is set from 3 V to 40 V.
2. Connect the positive voltage lead from the input power supply to VIN at the TP1 connector of the EVM.
3. Connect the ground lead from the input power supply to ground at the TP5 connector of the EVM.
4. Connect a 0-mA to 300-mA load between the TP2 (VOUT) and the TP3 (GND) connectors.
5. Turn on the input power supply.
6. Vary the respective loads and V_{IN} voltage as necessary for test purposes.

3 Schematic, PCB Layout, and Bill of Materials

3.1 Schematic

Figure 1 illustrates the EVM schematic.

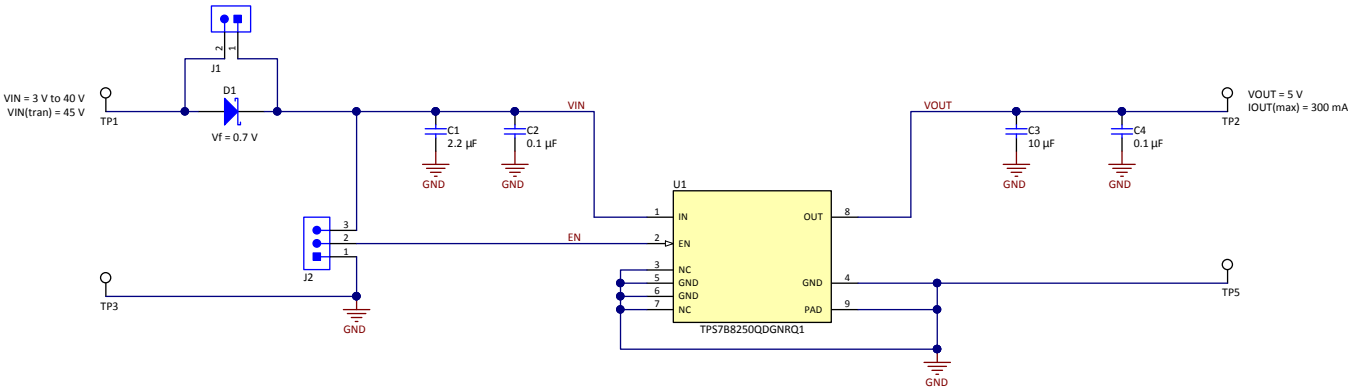

Figure 1. TPS7B8250EVM Schematic

3.2 PCB Layout

Figure 2 and Figure 3 show the PCB layout for the TPS7B8250EVM.

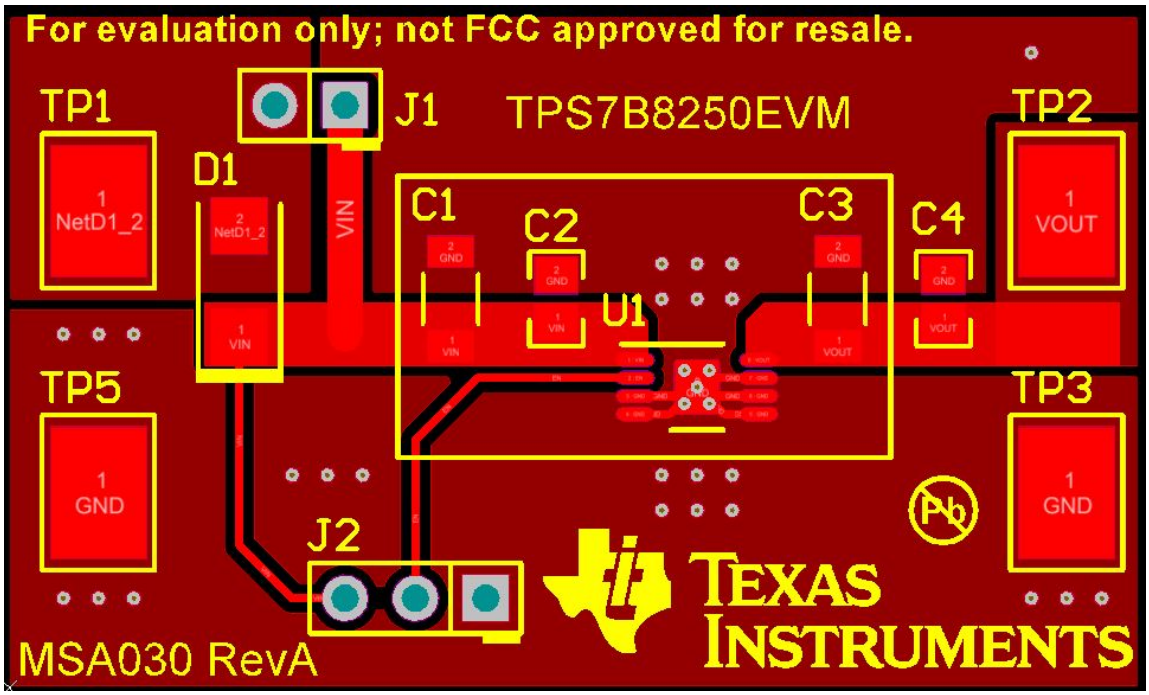

Figure 2. TPS7B8250EVM Top Layer Routing

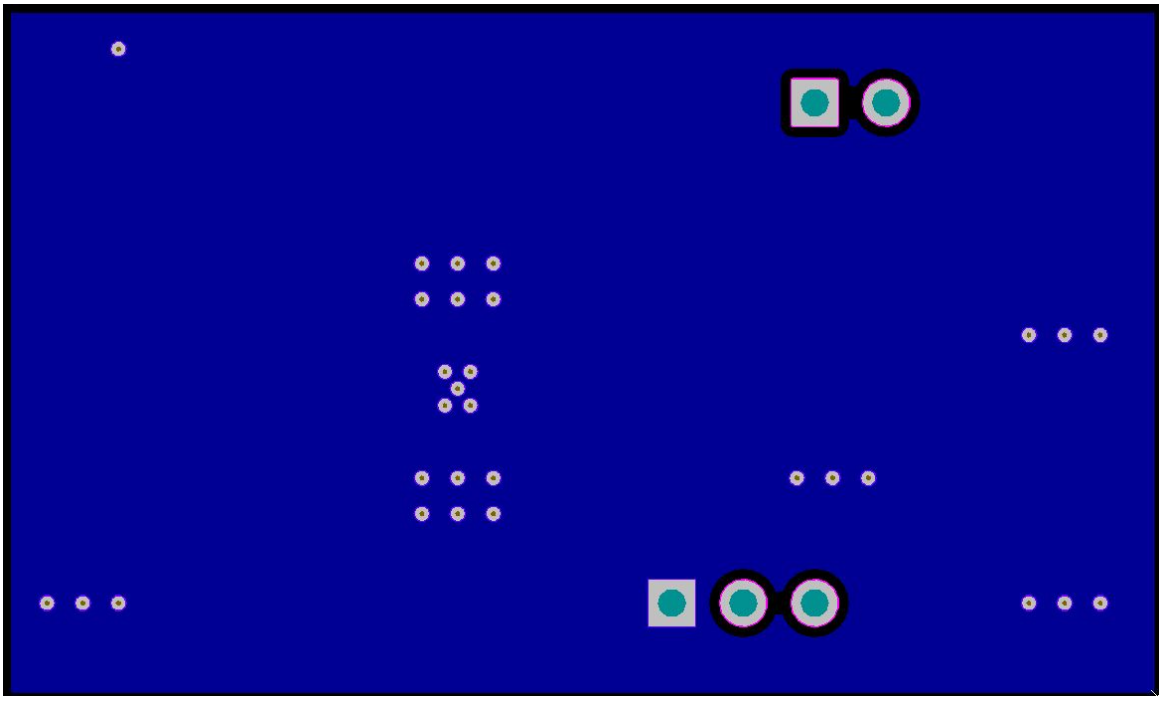

Figure 3. TPS7B8250EVM Bottom Layer Routing

3.3 Bill of Materials

Table 1 lists the EVM BOM.

Table 1. Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1	1	2.2 µF	Capacitor, ceramic, 2.2 µF, 50 V, +/- 10%, X7R, 1206	1206	GRM31CR71H225KA88L	Murata
C2	1	0.1 µF	Capacitor, ceramic, 0.1 µF, 50 V, +/- 10%, X7R, 0805	0805	GRM21BR71H104KA01L	Murata
C3	1	10 µF	Capacitor, ceramic, 10 µF, 25 V,+/- 10%, X7R, 1206	1206	GRM31CR71E106KA12L	Murata
D1	1	SMA	Diode, Schottky, 60 V, 2 A, SMA	SMA	B260A-13-F	Diodes Inc.
J1	1	TH	Header, 100mil, 2x1, Gold, TH	TSW-102-07-G-S	TSW-102-07-G-S	Samtec
J2	1	TH	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	TSW-103-07-G-S	Samtec
SH-J1, SH-J2	2		Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	969102-0000-DA	3M
TP1, TP2, TP3, TP5	4	SMT	Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone
U1	1		300mA High Voltage Ultra-Low I Q Low-Dropout Regulator	DGN0008D	TPS7B825050QDGNRQ1	Texas Instruments

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265