User's Guide

TPS65218EVM

ABSTRACT

This user's guide describes the characteristics, operation, and use of the TPS65218 evaluation module (EVM). The TPS65218EVM is a fully assembled platform for evaluating the performance of the TPS65218 power management device. This document includes schematic diagrams, a printed-circuit-board (PCB) layout, and bill of materials (BOM).

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1 Introduction

The TPS65218 is a highly-integrated power management solution for ARM Cortex® Microprocessors. Features of the TPS65218 include:

- 2 battery backup supplies
- 3 Buck converters
- 1 Buck-Boost converter
- USB load switch
- General purpose LDO
- Low-voltage load switch
- High-voltage load switch

2 Requirements

2.1 Software

The EVM will power-up and operate without use of software. A GUI is supplied to provide a simple way to communicate to the device via I^2C. The GUI can be downloaded from IPG-UI EVM GUI.

2.2 Host Computer

A computer with an available USB port is required to make use of the EVM software. The EVM software runs on the computer and communicates with the EVM via the USB2ANY interface.

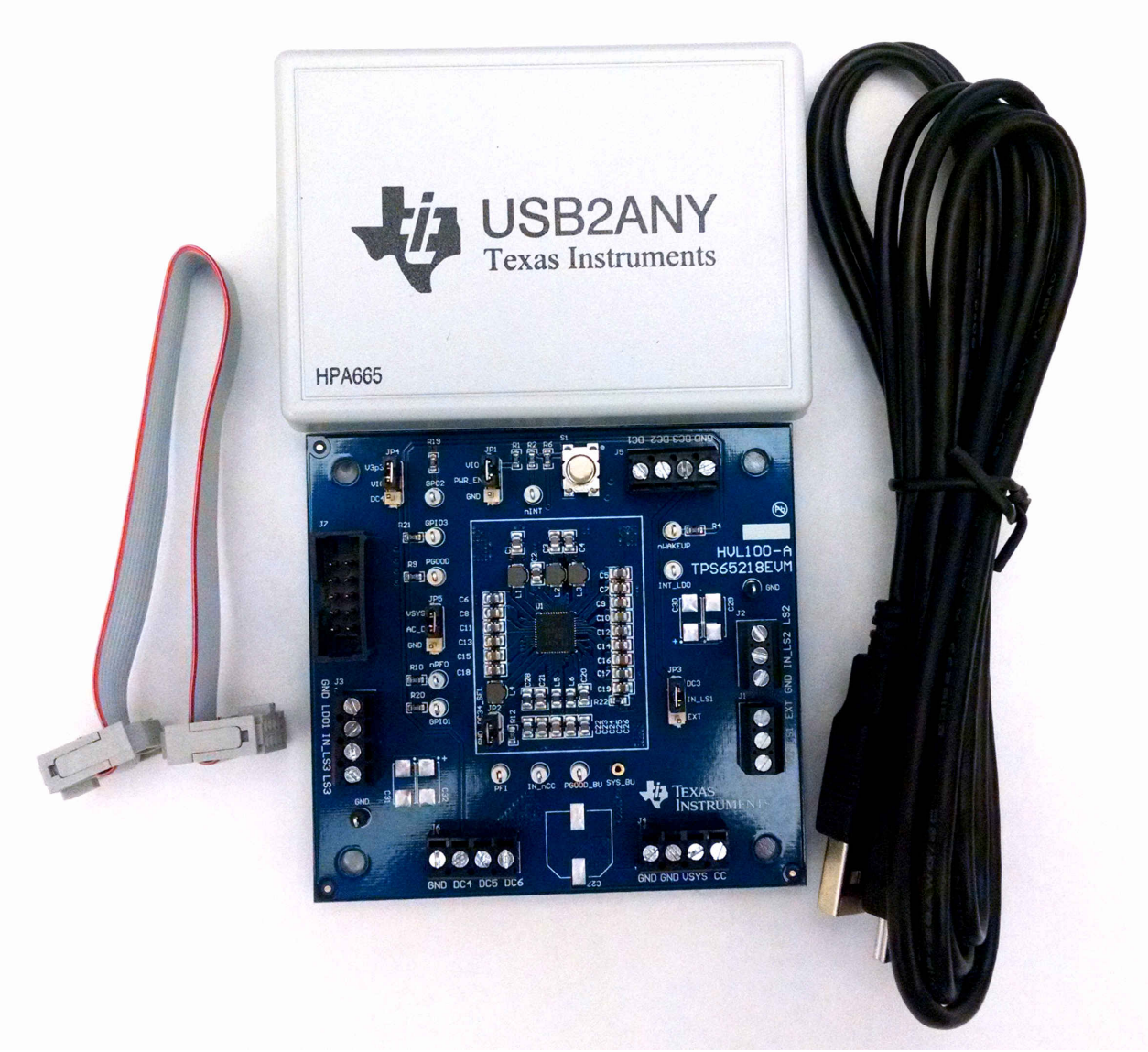
2.3 Power Supply

A DC power supply capable of delivering up to 5 V and 3 A, and a coin cell battery or separate 3-V power supply for the backup supplies.

3 EVM Kit

The EVM kit (Figure 3-1) contains the following items:

- TPS65218 evaluation board
- USB2ANY adapter
- USB to USB micro cable
- 10-pin ribbon cable
- 30-pin ribbon cable



The 30-pin ribbon cable is not required for the TPS65218EVM.

Figure 3-1. TPS65218 EVM Kit

4 Schematic

Figure 4-1 illustrates the schematic for this EVM.

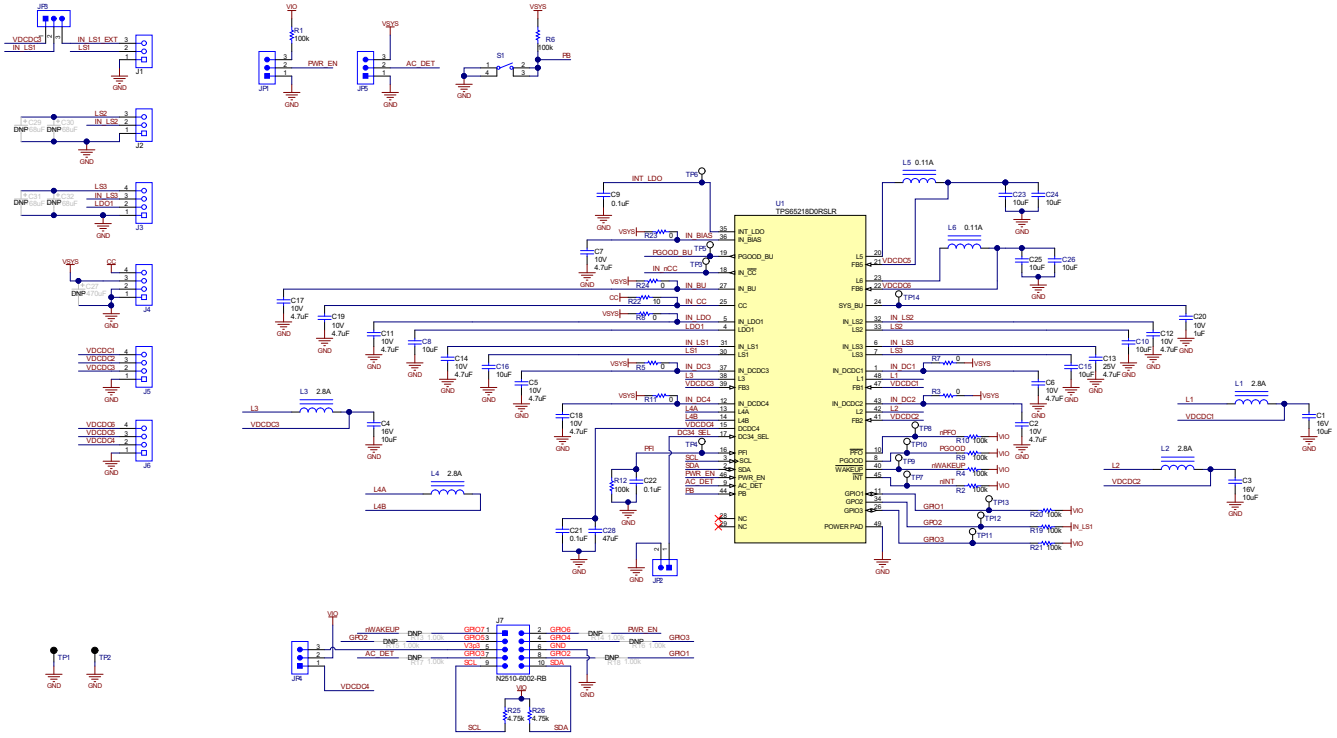


Figure 4-1. TPS65218 EVM Schematic

5 Terminal Block, Test Point, and Jumper Descriptions

Table 5-1. Terminal Block Descriptions

Connector	Pin	Description	Note
J1	GND	Ground	—
	LS1	LS1 Output	—
	EXT	External supply to LS1	Power Input (1.2 V – 3.3 V)
J2	GND	Ground	—
	IN_LS2	LS2 Input	Power Input (3.0 V – 5.5 V)
	LS2	LS2 Output	—
J3	GND	Ground	—
	LDO1	LDO1 Output	Default 1.8 V
	IN_LS3	LS3 Input	Power Input (1.8 V – 9.9 V)
	LS3	LS3 Output	—
J4	GND	Ground	—
	GND	Ground	—
	VSYS	DC Input	Power Input (2.7 V – 5.5 V)
	CC	Coin Cell Battery Input	Power Input (2.2 V – 3.3 V)
J5	GND	Ground	—
	DC3	Buck 3 Output (DCDC3)	Default 1.2 V Output
	DC2	Buck 2 Output (DCDC2)	Default 1.1 V Output
	DC1	Buck 1 Output (DCDC1)	Default 1.1 V Output
J6	GND	Ground	—
	DC4	Buck-Boost Output (DCDC4)	Default 3.3 V Output
	DC5	Battery Backup Supply Output (DCDC5)	1.0 V Output
	DC6	Battery Backup Supply Output (DCDC6)	1.8 V Output
J7	10-pin EVM connector for USB2ANY cable (I^2C communication)		

Table 5-2. Test Point Descriptions(1)

Test Point	Description
GND	Ground
INT_LDO	Internal bias voltage
nWAKEUP	Wakeup output signal
nINT	Interrupt output
nPFO	Power-fail comparator output
GPO2	General purpose output 2 or DDR reset output
GPIO3	General purpose output 3 or warm reset input
PGOOD	Power good
GPIO1	General purpose output 1
SYS_BU	Battery back-up power path output
PFI	Power-fail comparator input
IN_nCC	Output indicating power source for battery backup supplies
PGOOD_BU	Power good for backup supplies

(1) Test points are not designed to carry current, they are intended for measuring voltage.

Table 5-3. Jumper Descriptions

Jumper	Description	Default Position
JP1	Ties PWR_EN to VIO or GND	PWR_EN tied to VIO
JP2	Ties DC34_SEL pin to ground. Remove and jump with resistor for alternate voltage selections.	DC34_SEL tied to GND

Table 5-3. Jumper Descriptions (continued)

Jumper	Description	Default Position
JP3	Selects LS1 input between DCDC3 output and external supply from J1	IN_LS1 tied to DC3
JP4	Ties VIO to either DCDC4 output or 3.3-V supply from USB2ANY adaptor (J9). VIO supplies the pull-up voltage for the device I/Os.	VIO tied to V3p3
JP5	Ties AC_DET pin to either VSYS or GND. Tying to GND causes the device to start upon VSYS application.	AC_DET tied to VSYS

6 Setup

Figure 6-1 displays an example setup for using the TPS65218 EVM.

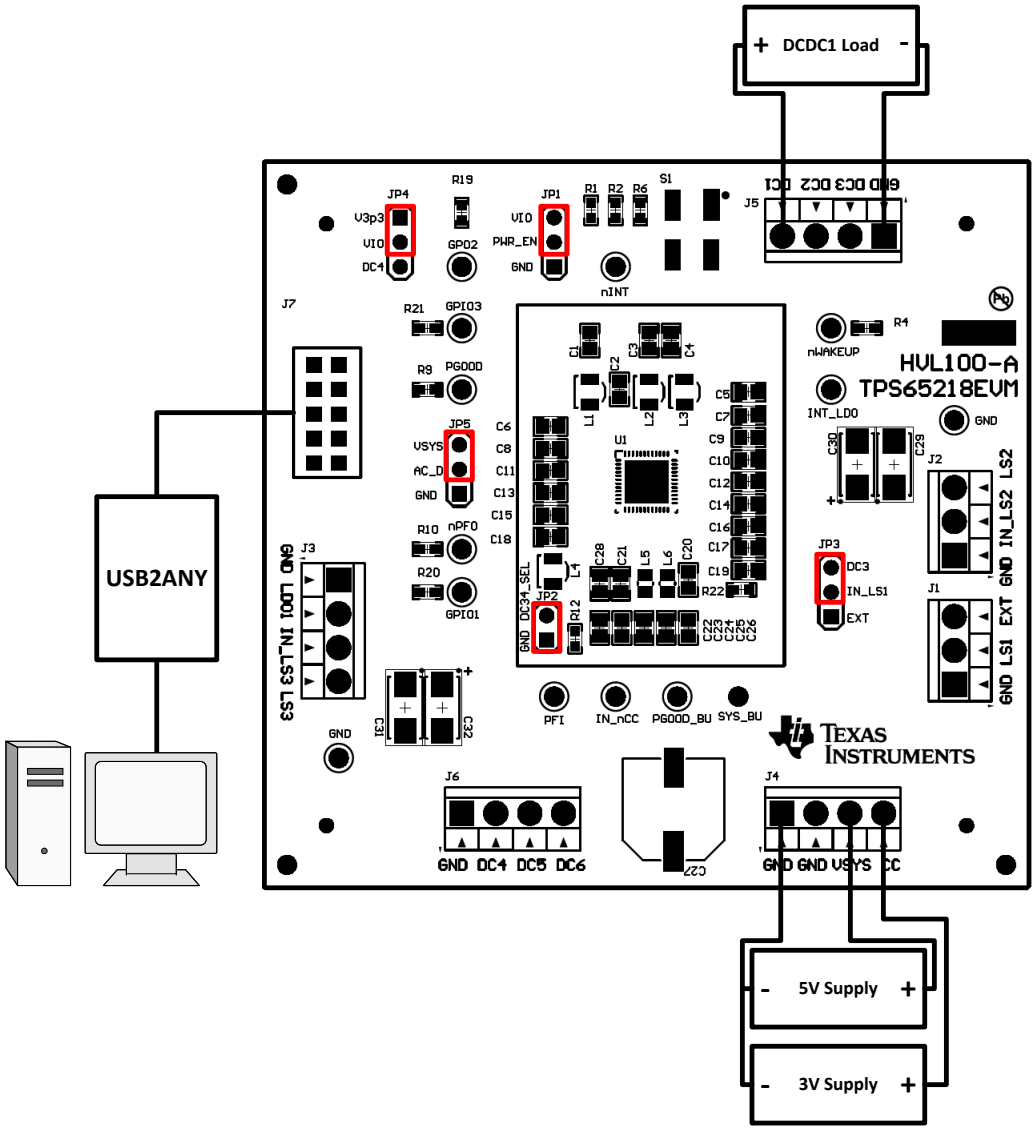


Figure 6-1. TPS65218 EVM Setup

7 Software

7.1 Software Installation Instruction

A GUI is supplied to provide a simple way to communicate to the device via I^2C. The GUI can be downloaded from: IPG-UI EVM GUI

Information on the installation of the IPG-UI can be found in the *IPG-UI User's Guide*.

You will also need to download the BOOSTXL-TPS65218 IPG-UI Device Support File. After you finish setting up the IPG-UI software, run the installer associated with your operating system to add the TPS65218 device file to your IPG-UI device library.

7.2 Using the TPS65218 GUI

Detailed information regarding the usage of the IPG-UI can also be found in the *IPG-UI User's Guide*. A brief overview is provided here for reference.

The proper device must first be selected from the "Select Devices" drop-down menu.

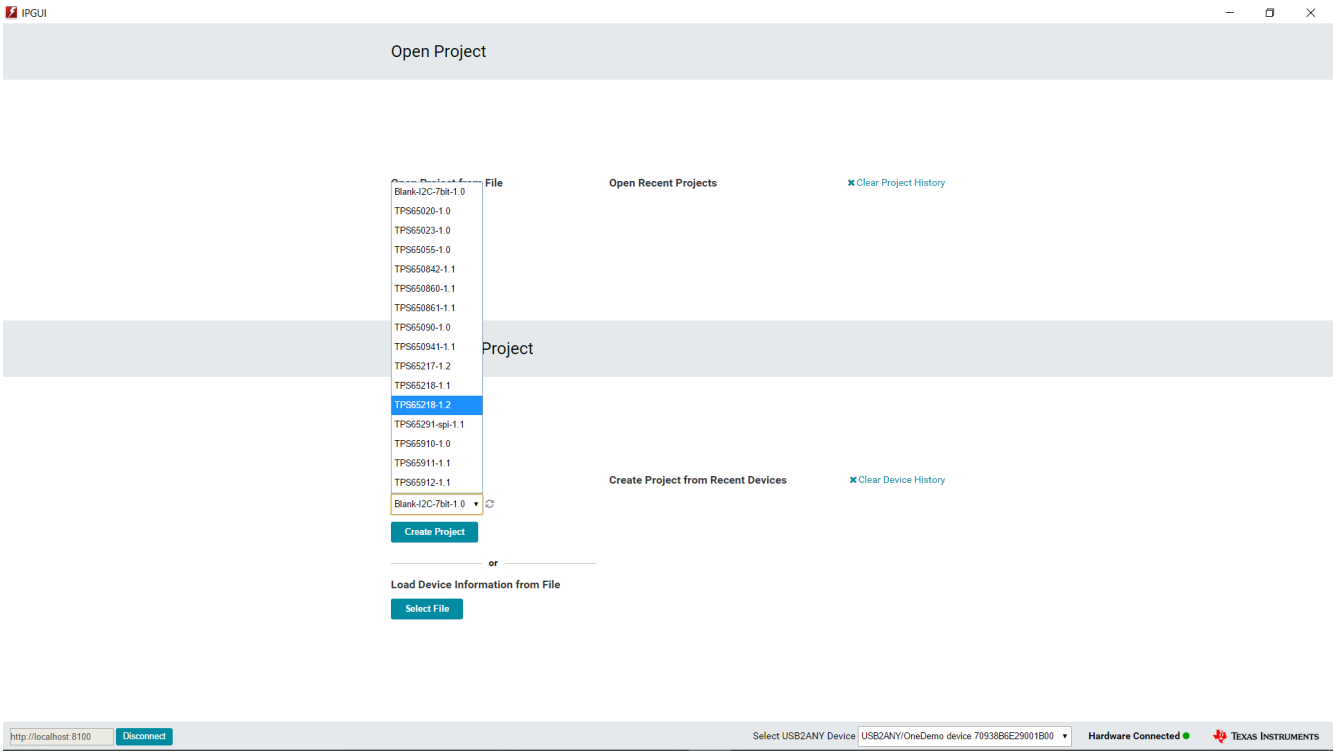


Figure 7-1. GUI front Page

From there, the next screen is the device introduction page, which includes a brief overview as well as the functional block diagram for the device.

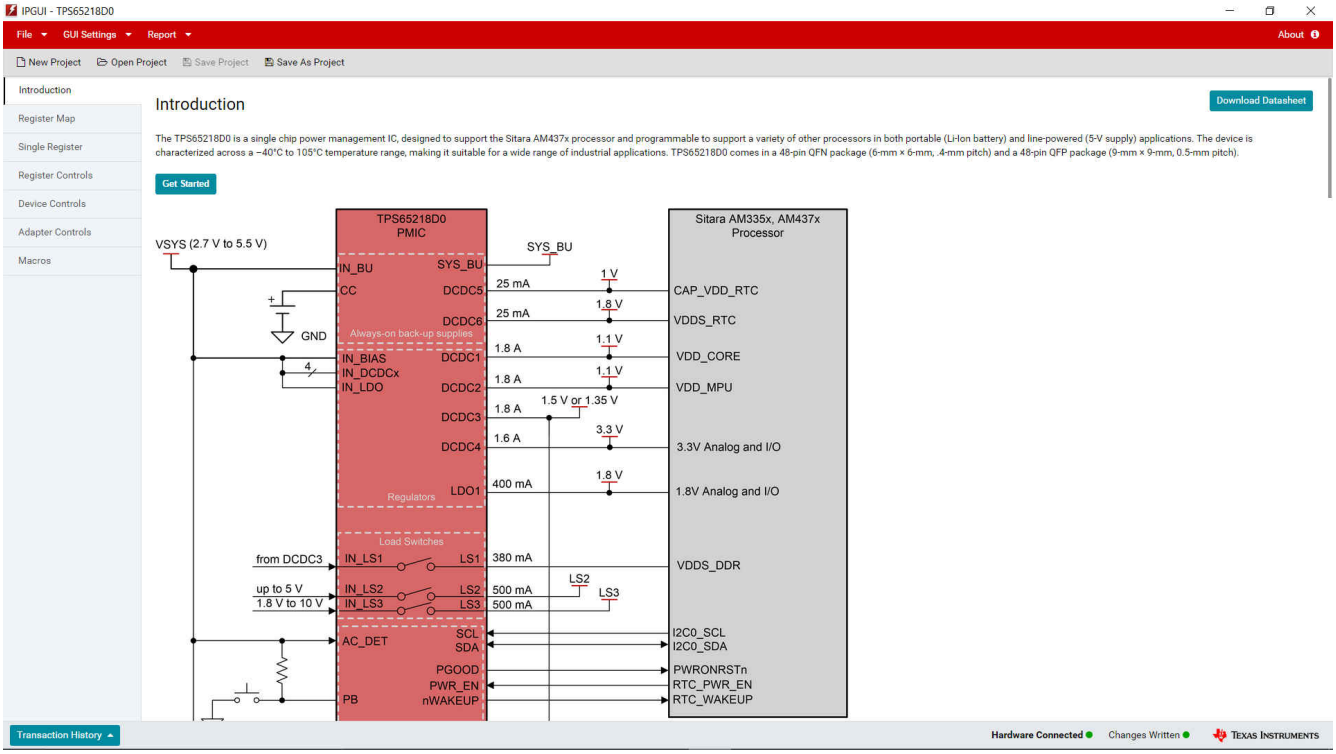


Figure 7-2. GUI Device Introduction

Finally, clicking on "Get Started" or on "Register Map" takes you to the I^2C controls for the device sorted by register address.

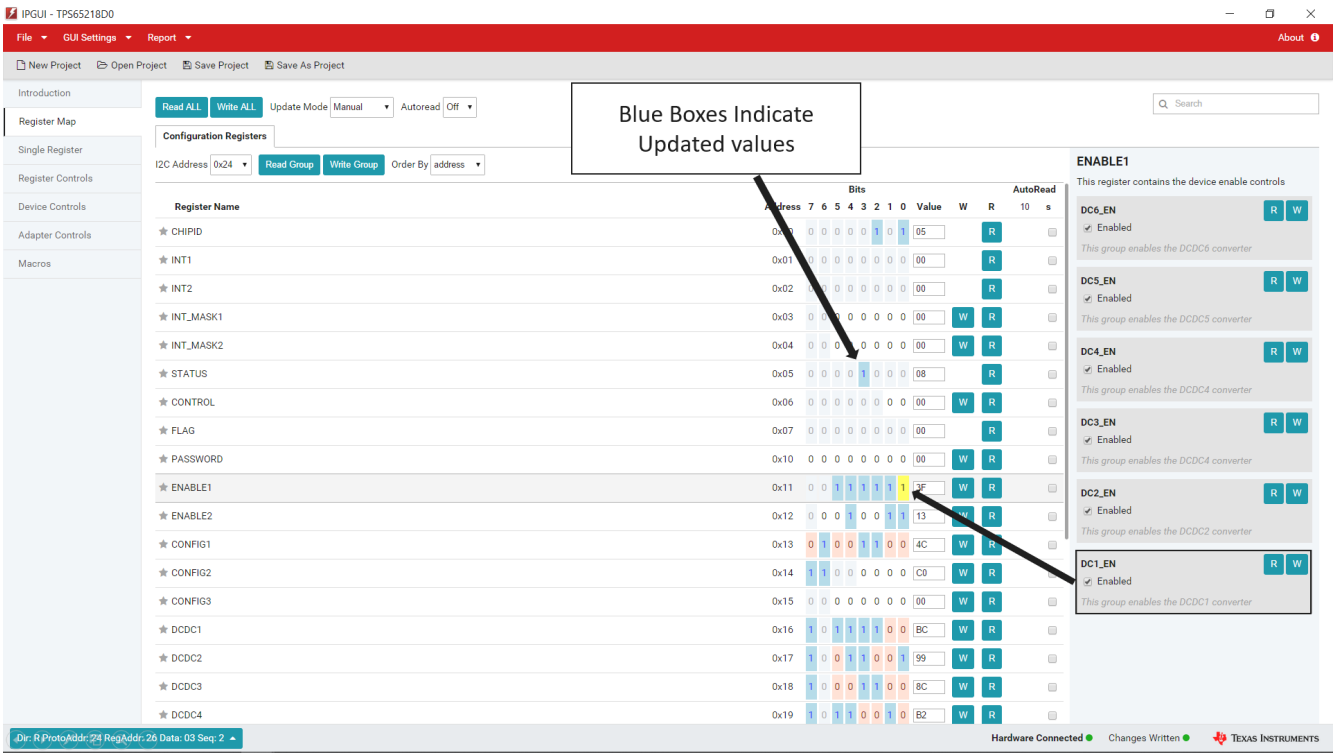


Figure 7-3. GUI Register Map

Alternatively, the part can be controlled using the "Register Controls" tab to sort by functionality rather than by I²C address location.

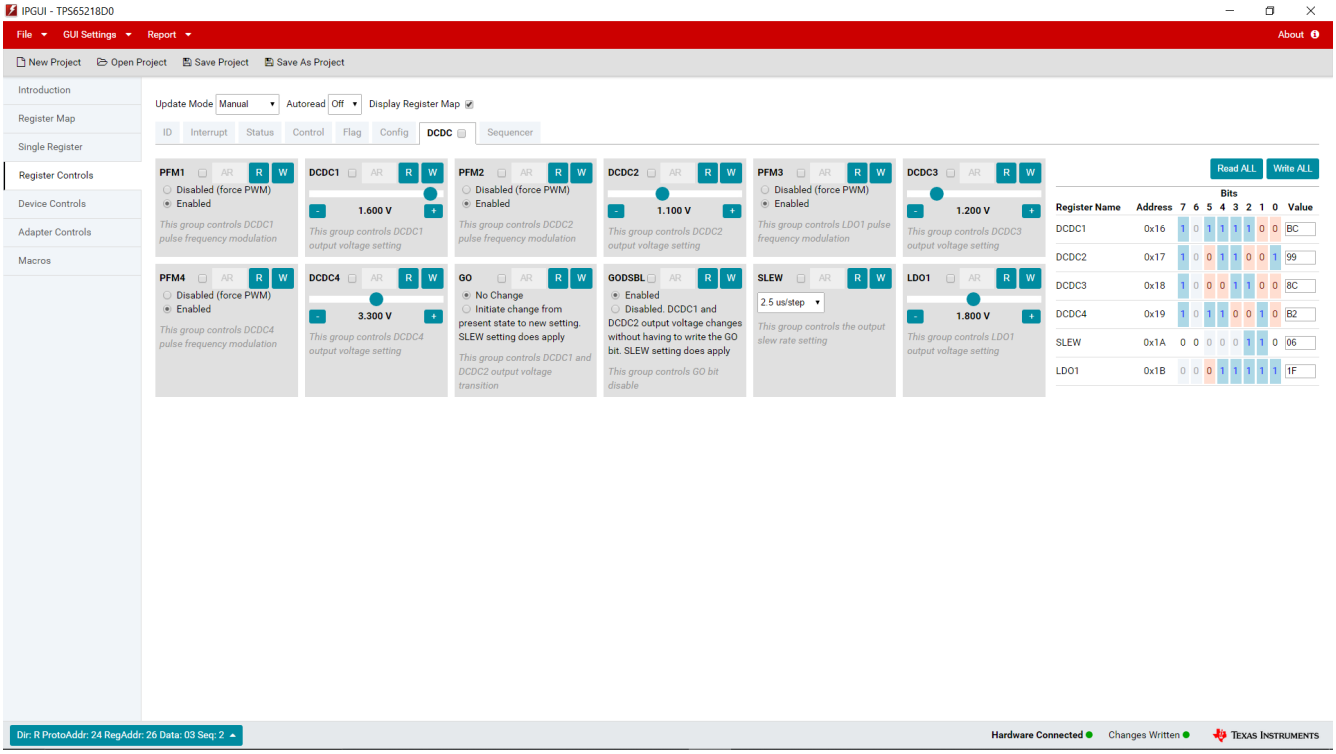


Figure 7-4. GUI Register Controls

With this information, it is possible to begin evaluating the TPS65218 device.

8 Bill of Materials

Table 8-1 lists the BOM for this EVM.

Table 8-1. Bill of Materials

Designator	Description	Value	Voltage Rating	Dielectric	Footprint	Qty.	Manufacturer	Manufacturer PN
C1, C3, C4	Capacitor	10µ	16V	X5R	805	3	MuRata	GRM21BR61C106KE15L
C8	Capacitor	10µ	6.3 V	X7R	805	1	TDK	C2012X7R0J106K125AB
C2, C5–C7, C11, C12, C14, C17–C19	Capacitor	4.7µ	10V	X7R	805	10	TDK	C2012X7R1A475K125AC
C10, C16, C23–C26	Capacitor	10µ	10V	X7R	805	6	TDK	C2012X7R1A106K125AC
C9, C21, C22	Capacitor	100n	100V	X5R	805	3	TDK	C2012X5R2A104K125AA
C13	Capacitor	4.7µ	25V	X5R	805	1	TDK	C2012X5R1E475K125AB
C15	Capacitor	10µ	16V	X7R	805	1	Samsung	CL21B106KOQNNNE
C28	Capacitor	47µ	10V	X5R	805	1	TDK	C2012X5R1A476M125AC
C20	Capacitor	1µ	10V	X7R	805	1	TDK	C2012X7R1A105K
C27	Capacitor	470µ	25V		CAP_EEE Size G	0	Panasonic	EEE1EA471UAP
C29, C30, C31, C32	Capacitor	68µ	16V		6032	0	Kemet	B45197A3686+30
L1, L2, L3, L4	Inductor	1.5µ			IND_SPM3012	4	TDK	SPM3012T-1R5M
L5, L6	Inductor	10µ			805	2	TDK	MLZ2012N100LT
R1, R2, R4, R6, R9, R10, R12, R19, R20, R21	Resistor	100K			603	10	Vishay-Dale	CRCW0603100KFKEA
R3, R5, R7, R8, R11, R23, R24	Resistor	0			805	7	Vishay-Dale	CRCW080500000Z0EAHP
R13–R18	Resistor	1K			603	0	Vishay-Dale	CRCW06031K00FKEA
R22	Resistor	10			603	1	Vishay-Dale	CRCW060310R0JNEAHP
R25, R26	Resistor	4.75K			603	2	Vishay-Dale	CRCW06034K75FKEA
S1	Switch		32V		6.3x5.36x6.6 mm	1	C&K Components	KT11P2JM34LFS
U1	PMIC				RSL (S-PQFP-N48) 0.4 pitch	1	Texas Instruments	TPS65218D0

9 Layout

Figure 9-1 through Figure 9-6 illustrate the PCB layouts for the evaluation module.

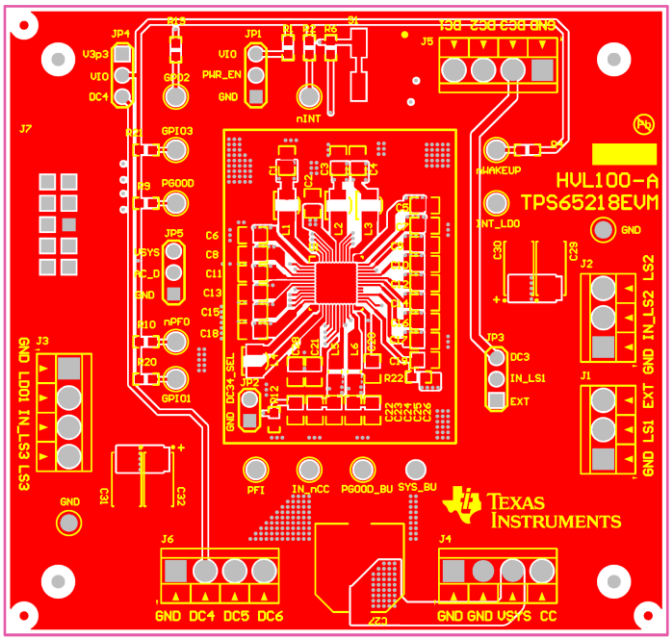


Figure 9-1. Top Layer Silkscreen

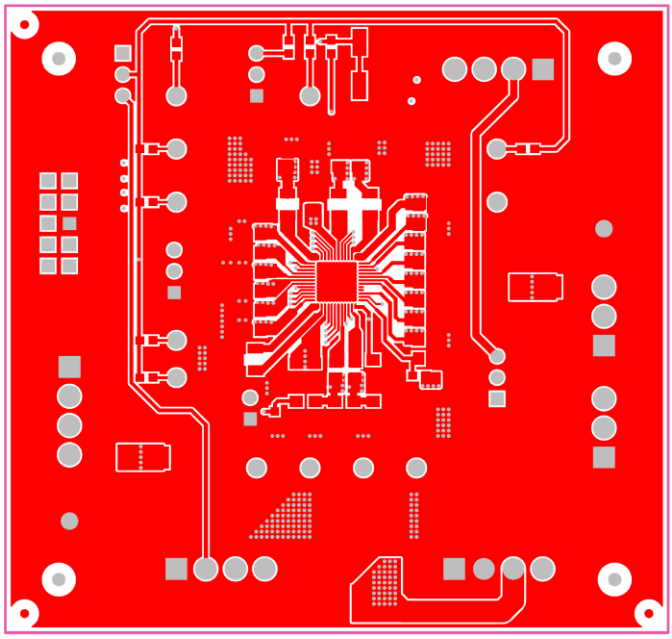


Figure 9-2. Top Layer

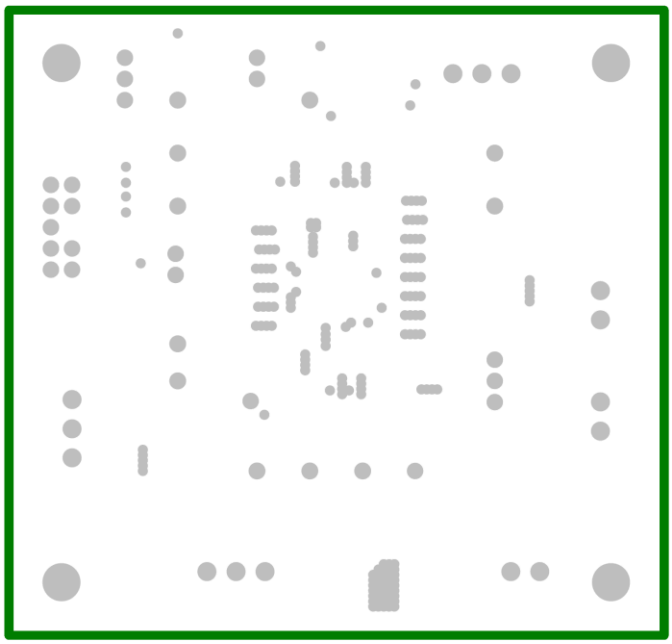


Figure 9-3. Ground Plane

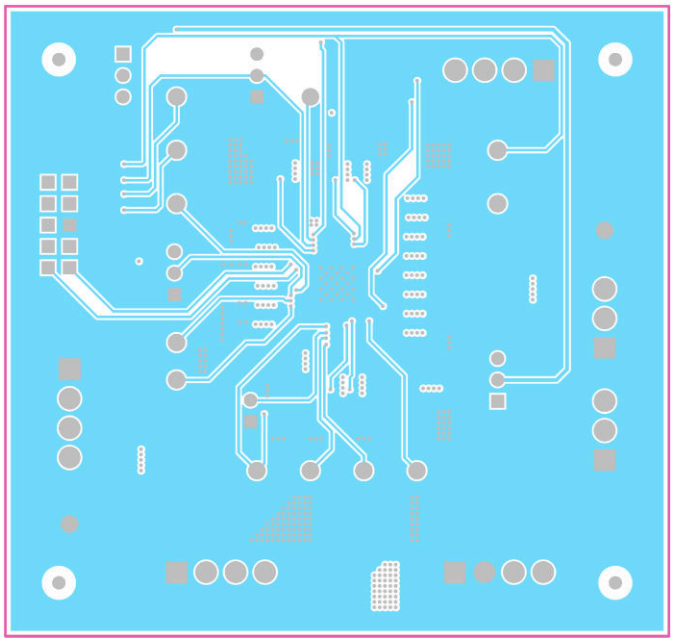


Figure 9-4. Mid Layer

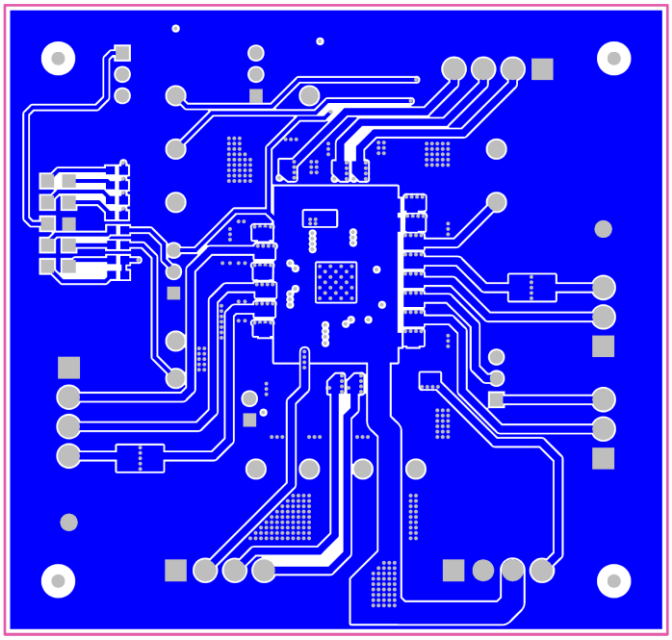


Figure 9-5. Bottom Layer

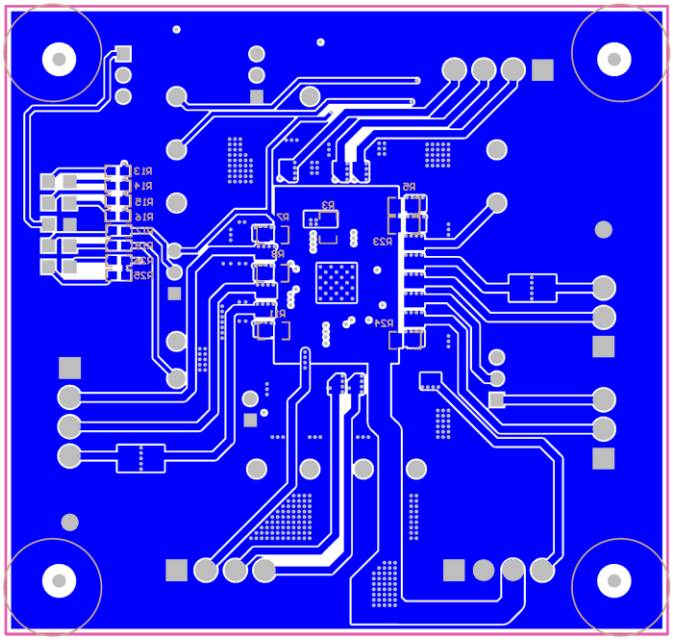


Figure 9-6. Bottom Layer Silkscreen

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2022) to Revision B (October 2022)	Page
• Updated EVM Schematic	4
• Updated Bill of Materials	11

Changes from Revision * (November 2014) to Revision A (August 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed GUI description	2
• Updated link to software	2
• Changed links to GUI and supporting hardware	8
• Updated descriptions	8
• Changed topic title	8
• Changed steps to use GUI	8
• Added new images	8
• Updated software links	8

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