# Evaluation Module for the TPS54561 Step-Down Converter

This user's guide contains information for the TPS54561EVM-555 evaluation module (PWR555) including the performance specifications, schematic, and the bill of materials.

**Contents**



**List of Figures**



**List of Tables**



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# 1 Introduction

This user's guide contains background information for the TPS54561 as well as support documentation for the TPS54561EVM-555 evaluation module (PWR555). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54561EVM-555.

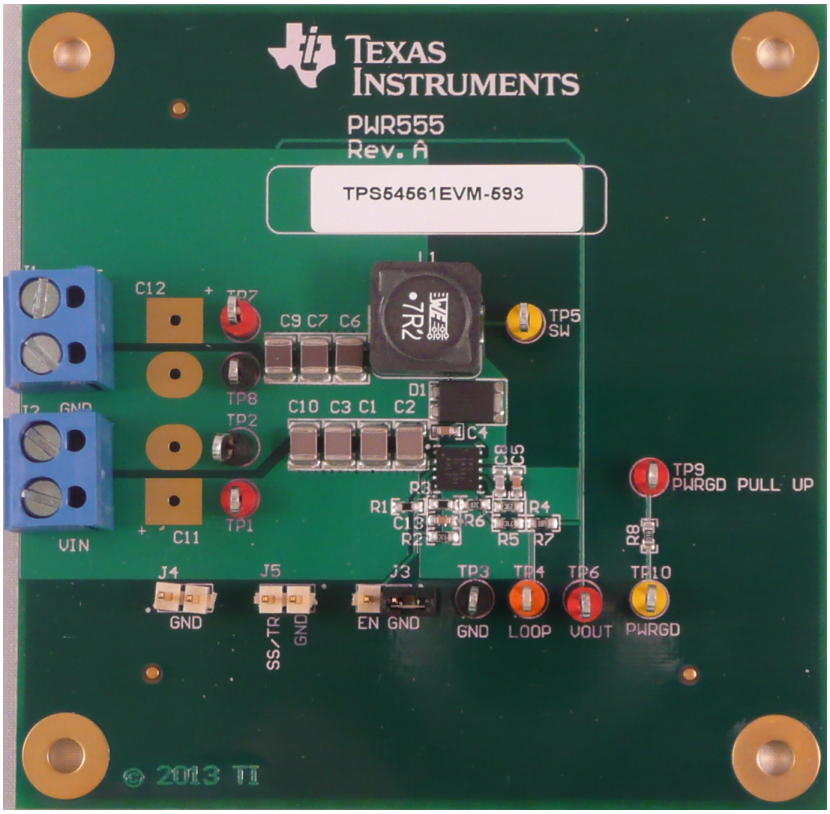



**Figure 1. TPS54561EVM-555 Board**

## 1.1 Background

The TPS54561 DC-DC converter is designed to provide up to a 5-A output from an input voltage source of 4.5 V to 60 V. Rated input voltage and output current range for the evaluation module are given in Table 1. This evaluation module is designed to demonstrate the small, printed-circuit-board (PCB) areas that may be achieved when designing with the TPS54561 regulator. The switching frequency is externally set at a nominal 400 kHz. The high-side MOSFET is incorporated inside the TPS54561 package along with the gate-drive circuitry. The compensation components are external to the integrated circuit (IC), and an external resistor divider allows for an adjustable output voltage. Additionally, the TPS54561 provides an adjustable undervoltage lockout with hysteresis through an external resistor divider at the EN pin and adjustable soft-start with an external capacitor at the SS/TR pin. The SS/TR pin can also be used to have the output voltage track an external reference. Lastly, the PWRGD pin is an integrated open drain output power good signal. The absolute maximum input voltage is 60 V for the TPS54561EVM-555.

**Table 1. Input Voltage and Output Current Summary**

| EVM | Input Voltage Range | Output Current Range |
|---|---|---|
| TPS54561EVM-555 | $V_{IN}$ = 7 V to 60 V | $I_{OUT}$ = 0 A to 5 A |

## 1.2 Performance Specification Summary

A summary of the TPS54561EVM-555 (EVM) performance specifications is provided in Table 2. Specifications are given for an input voltage of $V_{IN}$ = 12 V, an output voltage of 5 V, and an ambient temperature of 25°C, unless otherwise specified. This EVM is designed and tested for $V_{IN}$ = 7 V to 60 V.

**Table 2. TPS54561EVM-555 Performance Specification Summary**

| Specification | Test Conditions | | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ voltage range | | | 7 | 12 | 60 | V |
| Output voltage set point | | | | 5 | | V |
| Output current range | $V_{IN}$ = 7 V to 60 V | | 0 | | 5 | A |
| Line regulation | $I_{OUT}$ = 5 A, $V_{IN}$ = 7 V to 60 V | | | ±0.03% | | |
| Load regulation | $V_{IN}$ = 12 V, $I_{OUT}$ = 0.001 A to 5 A | | | ±0.03% | | |
| Load transient response | $I_{OUT}$ = 1.25 A to 3.75 A | Voltage change | | –160 | | mV |
| | | Recovery time | | 250 | | µs |
| | $I_{OUT}$ = 3.75 A to 1.25 A | Voltage change | | 160 | | mV |
| | | Recovery time | | 250 | | µs |
| Loop bandwidth | $V_{IN}$ = 12 V, $I_{OUT}$ = 5 A | | | 20 | | kHz |
| Phase margin | $V_{IN}$ = 12 V, $I_{OUT}$ = 5 A | | | 67 | | ° |
| Input voltage ripple | $I_{OUT}$ = 5 A | | | 480 | | mVpp |
| Output voltage ripple | $I_{OUT}$ = 5 A | | | 5 | | mVpp |
| Output rise time | 10% to 90% | | | 3.8 | | ms |
| Operating frequency | | | | 400 | | kHz |
| Maximum efficiency | TPS54561EVM-555, $V_{IN}$ = 12 V, $I_{OUT}$ = 1.1 A | | | 92.4% | | |
| DCM threshold | $V_{IN}$ = 12 V | | | 410 | | mA |
| Pulse skipping threshold | $V_{IN}$ = 12 V | | | 25 | | mA |
| No load input current | $V_{IN}$ = 12 V | | | 280 | | µA |
| UVLO start threshold | | | | 6.5 | | V |
| UVLO stop threshold | | | | 5.0 | | V |

## 1.3 Schematic

Figure 2 is the schematic for the EVM.

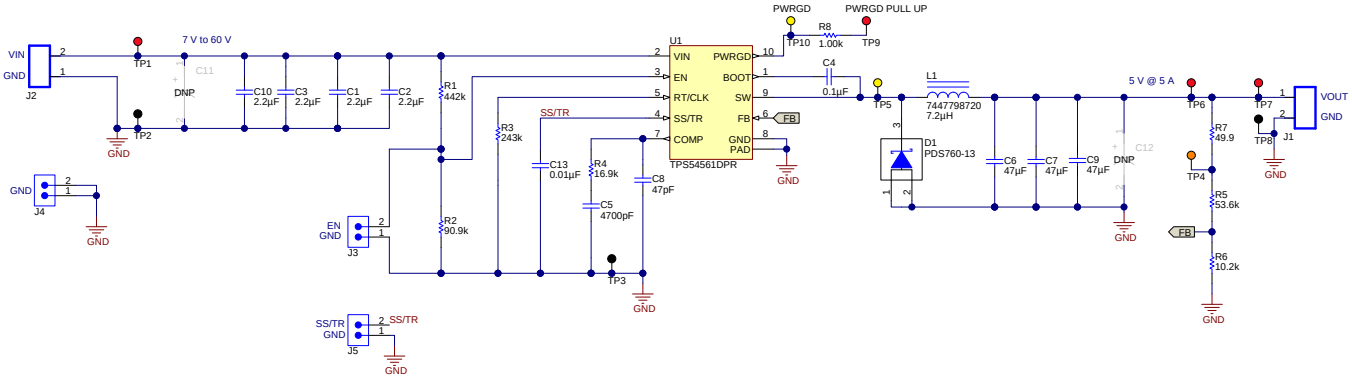



**Figure 2. TPS54561EVM-555 Schematic**

## 1.4 Modifications

These evaluation modules are designed to provide access to the features of the TPS54561. Some modifications can be made to this module. Component selection for modifications can be done with the aid of WEBENCH or the excel spreadsheet (SLVC452), located on the product page.

### 1.4.1 Output Voltage Set Point

To change the output voltage of the EVM, the value of resistor R5 ($R_{HS}$) should be changed while keeping R6 ($R_{LS}$) fixed. The output voltage can be adjusted to a minimum of the 0.8 V internal reference. The value of R5 for a specific output voltage can be calculated using Equation 1:

$$R_{HS} = R_{LS} \times \left( \frac{Vout - 0.8V}{0.8\ V} \right) \quad (1)$$

Table 3 lists the R5 values for some common output voltages, assuming R6 = 10.2 kΩ. Note $V_{IN}$ must be in a range to keep the on time greater than the minimum on-time. The values given in Table 3 are standard 1% values, not the exact value calculated using Equation 1.

**Table 3. R5 Values for Common Output Voltages**

| Output Voltage (V) | R5 Value (kΩ) |
|---|---|
| 1.8 | 12.7 |
| 2.5 | 21.5 |
| 3.3 | 31.6 |
| 5.0 | 53.6 |

Be aware, changing the output voltage can affect the loop response. It may be necessary to modify the compensation components. Please see the TPS54561 data sheet (SLVSBO1) for details.

### 1.4.2 Operating Frequency, Soft-Start and UVLO

The operating frequency, soft-start time and UVLO voltage may also be adjusted. R3 sets the operating frequency, C13 sets the slow-start time and the resistor divider of R1 and R2 sets the UVLO start and stop voltages. Please see the TPS54561 data sheet (SLVSBO1) for details.

# 2 Test Setup and Results

This section describes how to properly connect, set up, and use the EVM. The section also includes test results typical for the EVM covering efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, start up, and shutdown. Measurements were taken at an ambient temperature of 25°C.

## 2.1 I/O Connections

This EVM includes I/O connectors and test points as shown in Table 4. A power supply capable of supplying at least 5 A must be connected to J2 through a pair of 20-AWG wires. The load must be connected to J1 through a pair of 20-AWG wires. The maximum load-current capability must be 5 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the $V_{IN}$ input voltages with TP2 providing a convenient ground reference. TP3 is used to monitor the output voltage with TP4 as the ground reference.

**Table 4. EVM Connectors and Test points**

| Reference Designator | Function |
|---|---|
| J1 | $V_{OUT}$, 5 V at 5-A maximum |
| J2 | $V_{IN}$ (see Table 1 for $V_{IN}$ range) |
| J3 | EN jumper. Connect EN to ground to disable, open to enable. |
| J4 | GND header for additional ground connections |
| J5 | SS/TR header with GND reference for monitoring the soft-start or implementing sequencing/tracking |
| TP1 | $V_{IN}$ test point at $V_{IN}$ connector |
| TP2 | GND test point at $V_{IN}$ |
| TP3 | Output voltage test point at $V_{OUT}$ connector |
| TP4 | GND test point at $V_{OUT}$ connector |
| TP5 | SW test point |
| TP6 | $V_{OUT}$ test point used for loop response measurements |
| TP7 | Test point between voltage divider network and output. Used for loop response measurements. |
| TP8 | GND test point |
| TP9 | Test point for pull up voltage of the open drain output power good signal |
| TP10 | PWRGD test point |

## 2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 1.1 A with $V_{IN}$ = 12 V, and then decreases as the load current increases towards full load. Figure 3 shows the efficiency for the EVM. Figure 4 shows the light-load efficiency for the EVM using a semi-log scale. The efficiency may be lower at higher ambient temperatures due to temperature variation in the drain-to-source resistance of the internal MOSFET.

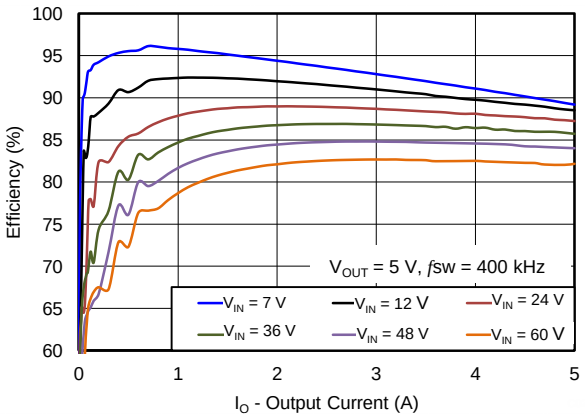



**Figure 3. Efficiency Versus Load Current**

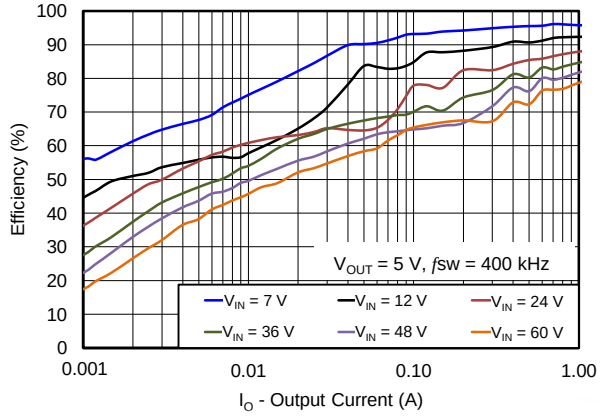



**Figure 4. Light-Load Efficiency**

## 2.3 Output Voltage Regulation

The load regulation for the EVM is shown in Figure 5. The line regulation for the EVM is shown in Figure 6.

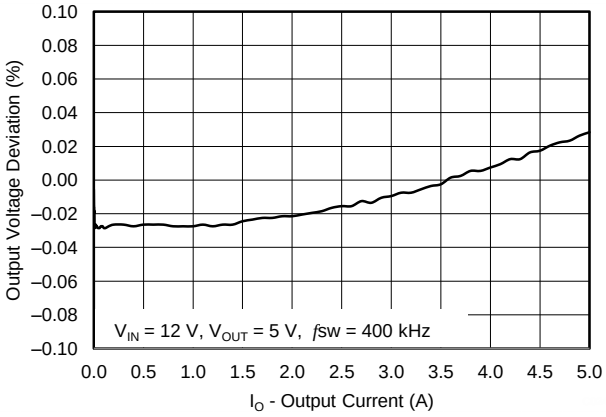



**Figure 5. Regulation Versus Output Current**

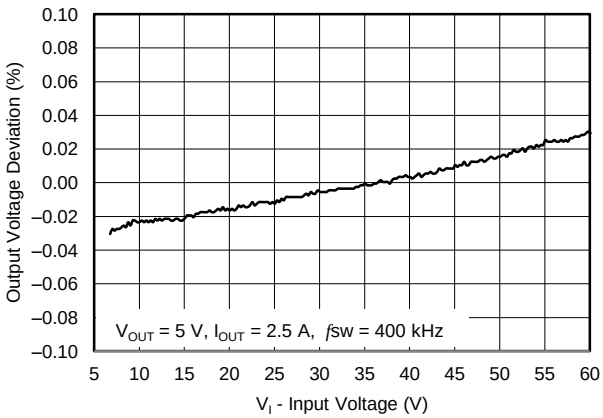



**Figure 6. Regulation Versus Input Voltage**

## 2.4 Load Transients and Loop Response

The EVM response to load transients is shown in Figure 7. The current step is from 25% to 75% of the maximum rated load at 12-V input. The current step slew rate is 100 mA/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

The EVM loop-response characteristics are shown in Figure 8. Gain and phase plots are shown for $V_{IN}$ voltage of 12 V. Load current for the measurement is 5 A.

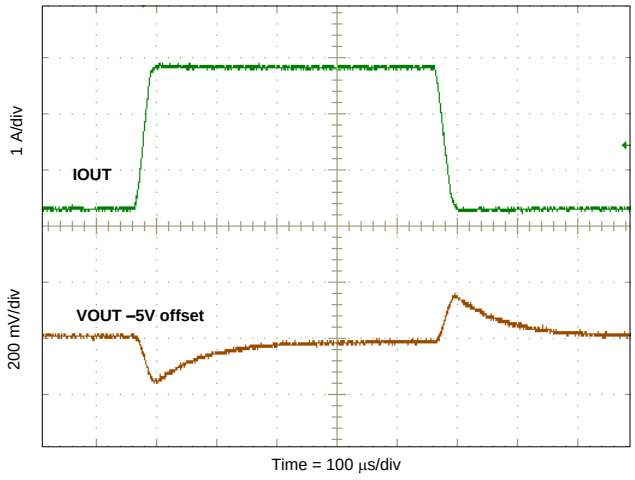



**Figure 7. Load Transient Response**

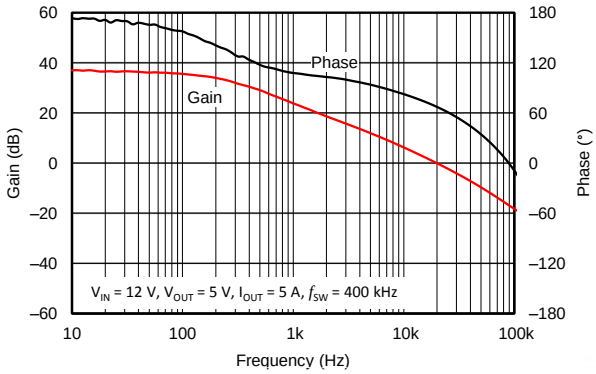



**Figure 8. Loop Response**

## 2.5 Line Transients

The EVM response to line transients is shown in Figure 9. The input voltage step is from 8 V to 40 V. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

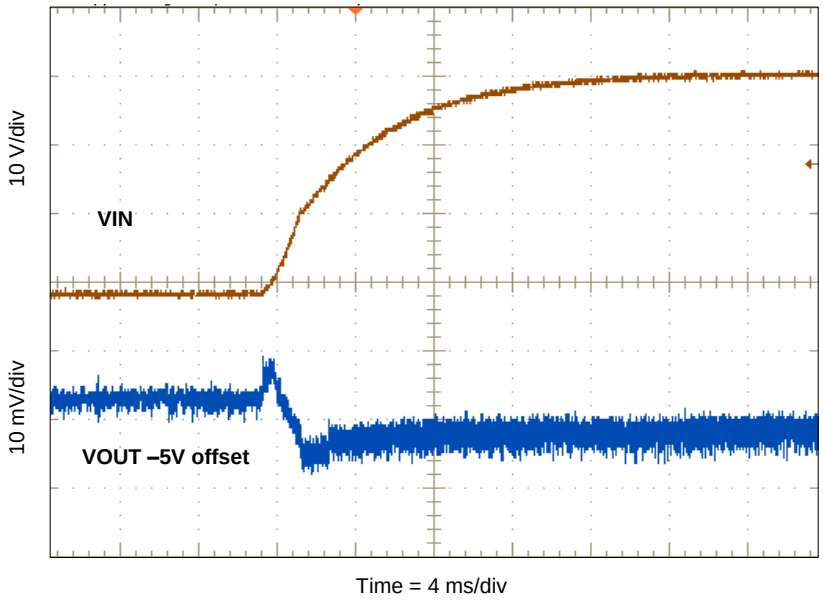



**Figure 9. Line Transient Response**

## 2.6 Input Voltage Ripple

The EVM CCM input voltage ripple is shown in Figure 10. The output current is the rated full load of 5 A and $V_{IN}$ = 12 V. The voltage ripple is measured directly across the input capacitors.

The DCM input voltage ripple is shown in Figure 11. The output current is 0.1 A and $V_{IN}$ = 12 V.

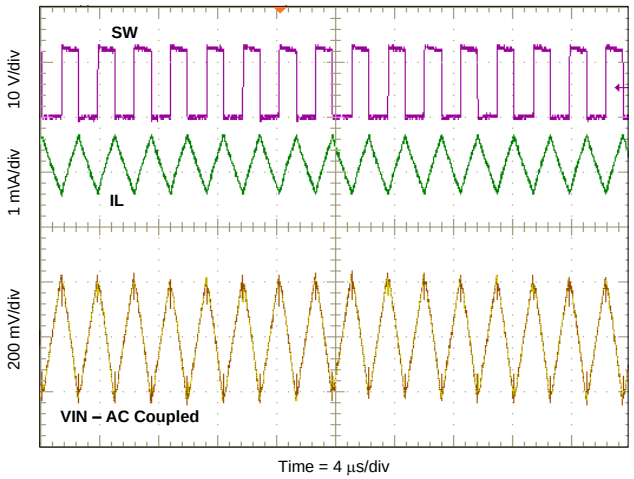



**Figure 10. Input Voltage Ripple CCM**

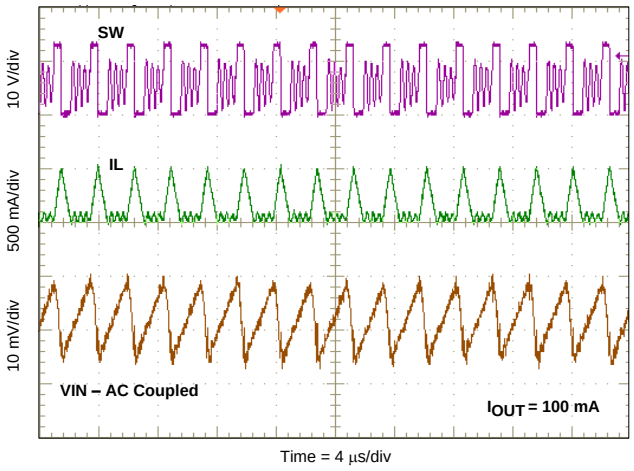



**Figure 11. Input Voltage Ripple DCM**

## 2.7 Output Voltage Ripple

The EVM CCM output voltage ripple is shown in Figure 12. The output current is the rated full load of 5 A and $V_{IN}$ = 12 V. The voltage ripple is measured directly across the output capacitors.

The DCM output voltage ripple is shown in Figure 13. The output current is 0.1 A and $V_{IN}$ = 12 V.

The Pulse Skip Eco-mode™ output voltage ripple is shown in Figure 14. There is no external load on the output and $V_{IN}$ = 12 V.

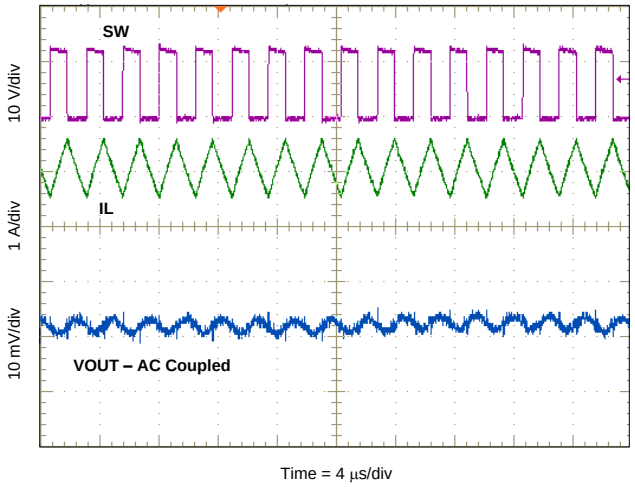



Figure 12. Output Voltage Ripple CCM

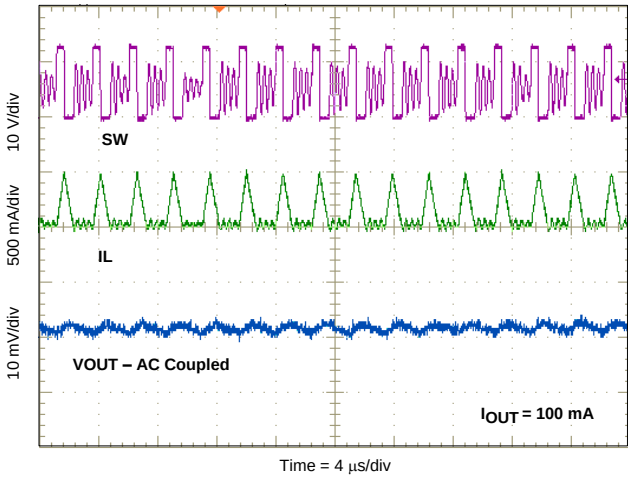



Figure 13. Output Voltage Ripple DCM

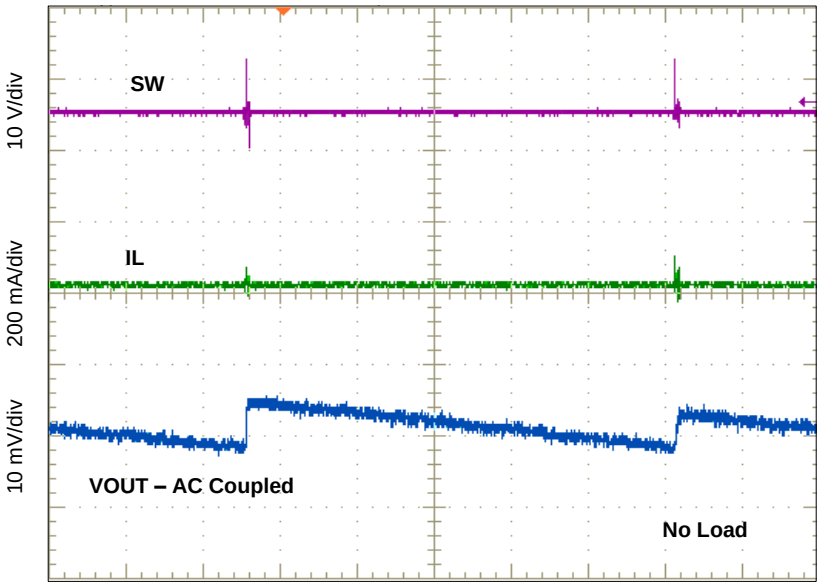



Figure 14. Output Voltage Ripple Eco-mode

## 2.8 Start Up

The start up waveforms are shown in Figure 15, Figure 16, and Figure 17. The input voltage for these plots is 12 V with a 5-A resistive load. In Figure 15 the top trace shows $V_{IN}$, the middle trace shows EN, and the bottom trace shows $V_{OUT}$. The input voltage is initially applied, and when the input reaches the undervoltage lockout threshold, the start up sequence begins and the output ramps up toward the set value of 5 V.

In Figure 16 the input voltage is initially applied with EN held low. When EN is released, the start up sequence begins and the output ramps up toward the set value of 5 V.

In Figure 17 the input voltage is initially applied with EN held low. An external voltage of 3.3 V is supplied to $V_{OUT}$. When EN is released, the start up sequence begins and the internal reference ramps up from 0 V with the internal soft-start. When the internal reference reaches the FB voltage the output begins ramping toward the set value of 5 V.

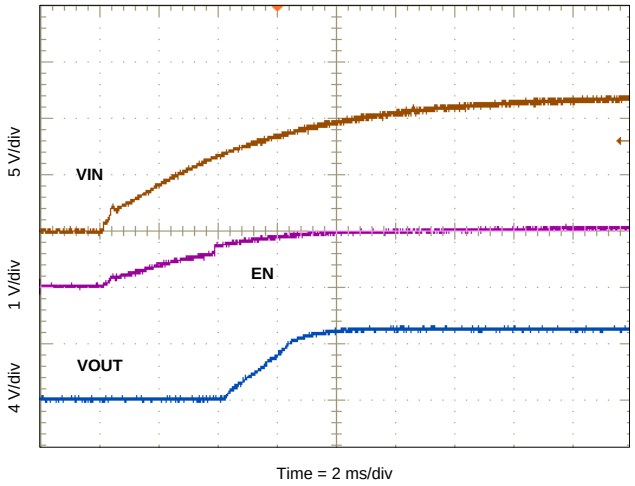



**Figure 15. Start Up Relative to $V_{IN}$**

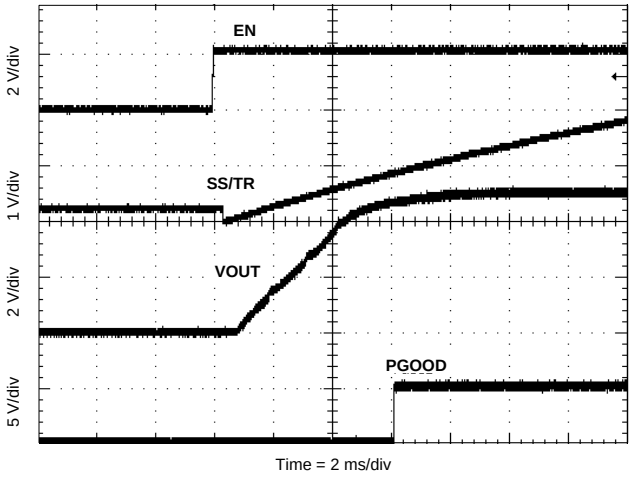
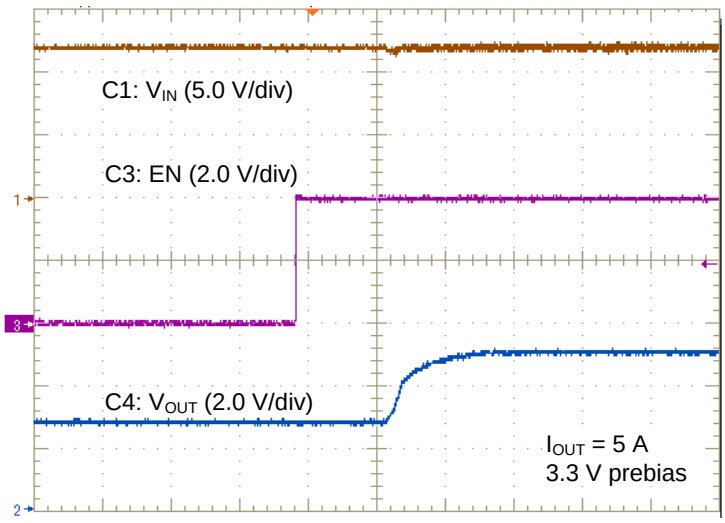



**Figure 16. Start Up Relative to EN**



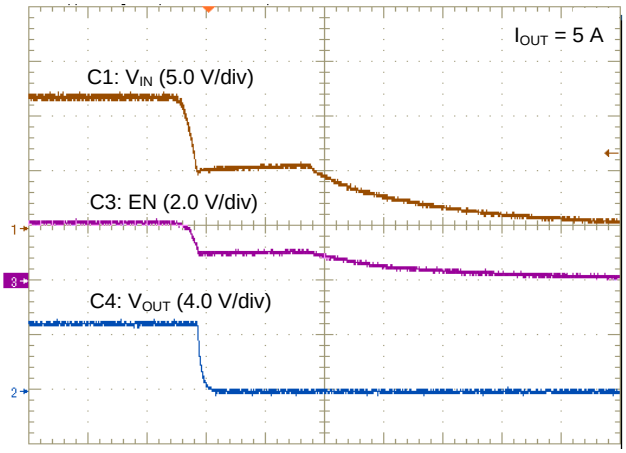

**Time: 2.0 ms/div**

**Figure 17. Prebias Start Up Relative to EN**

## 2.9 Shutdown

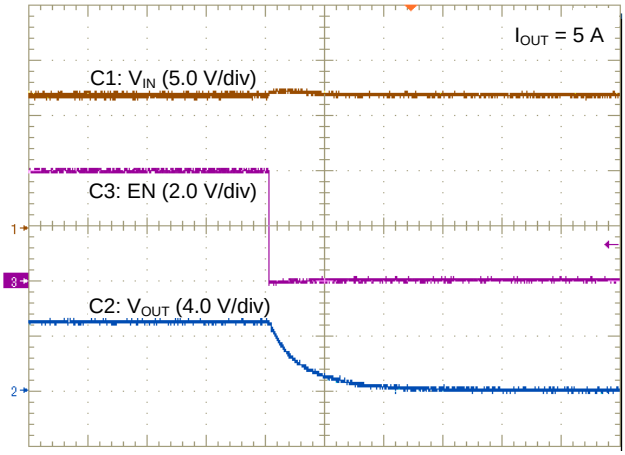
The shutdown waveforms are shown in Figure 18 and Figure 19. The input voltage for these plots is 12 V with a 5-A resistive load. The top trace shows $V_{IN}$, the middle trace shows EN, and the bottom trace shows $V_{OUT}$. In Figure 18 the input voltage is removed, and when the input falls below the undervoltage lockout threshold, the TPS54561 shuts down and the output falls to ground.

In Figure 19, the input voltage is held at 12 V, and EN is shorted to ground. When EN is grounded, the TPS54561 is disabled, and the output voltage discharges to ground.




**Time: 2.0 ms/div**

**Figure 18. Shutdown Relative to $V_{IN}$**

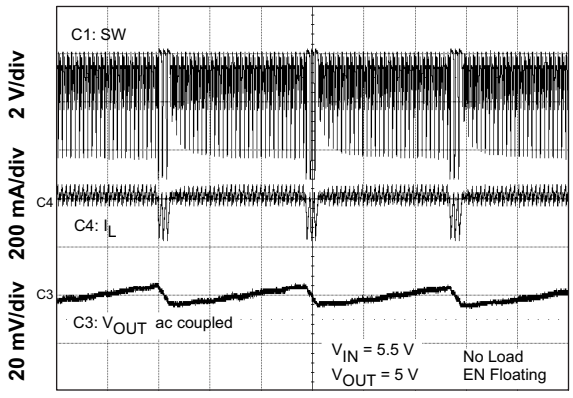



**Time: 200 µs/div**

**Figure 19. Shutdown Relative to EN**

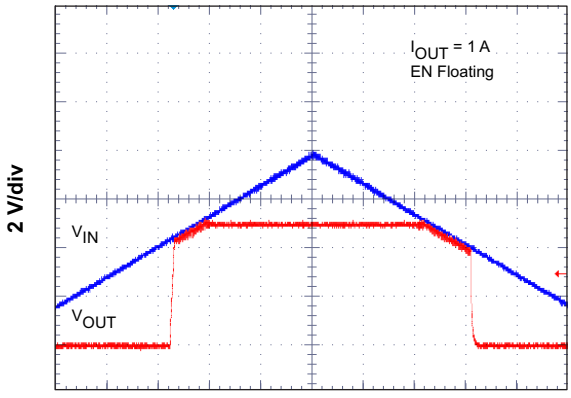
## 2.10 Low Dropout Operation

For improved low dropout operation, the TPS54561 includes a small integrated low-side MOSFET to pull SW to GND when the BOOT to SW voltage drops below 2.1 V. This recharges the BOOT capacitor for driving the high-side MOSFET. Figure 20 shows the steady state operation and Figure 21 shows the start up and shutdown in a low dropout condition. Both measurements are taken with a 5-V output.




**Time = 20 µs/div**

**Figure 20. Low Dropout Operation**




**Time = 40 µs/div**

**Figure 21. Low Dropout Start Up and Shutdown**

# 3 Board Layout

This section provides a description of the EVM, board layout, and layer illustrations.

## 3.1 Layout

The board layout for the EVM is shown in Figure 22 through Figure 25. The top-side layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz copper.

The top layer contains the main power traces for $V_{IN}$, $V_{OUT}$, and SW. Also on the top layer are connections for the remaining pins of the TPS54561 and a large area filled with ground. The bottom layer contains ground and a signal route for the bootstrap capacitor. The top and bottom and internal ground traces are connected with multiple vias placed around the board including six vias directly under the TPS54561 device to provide a thermal path from the top-side ground plane to the bottom-side ground plane.

The input decoupling capacitors (C1-C3, C10), bootstrap capacitor (C4), and frequency set resistor (R3) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. To reduce noise on the PWRGD signal, the PWRGD traces and pull up resistor (R8) is kept away from the switching node at the SW pin. The voltage divider network ties to the output voltage at the point of regulation, the copper $V_{OUT}$ trace past the output connector (J1). For the TPS54561, an additional input bulk capacitor may be required (C11), depending on the EVM connection to the input supply.

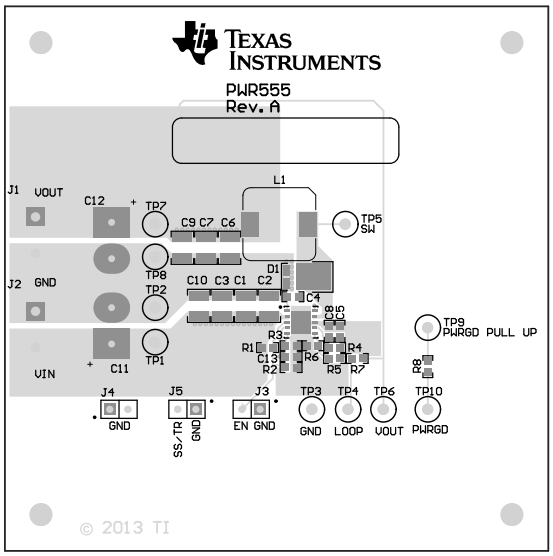



**Figure 22. TPS54561EVM-555 Top Assembly and Silkscreen**

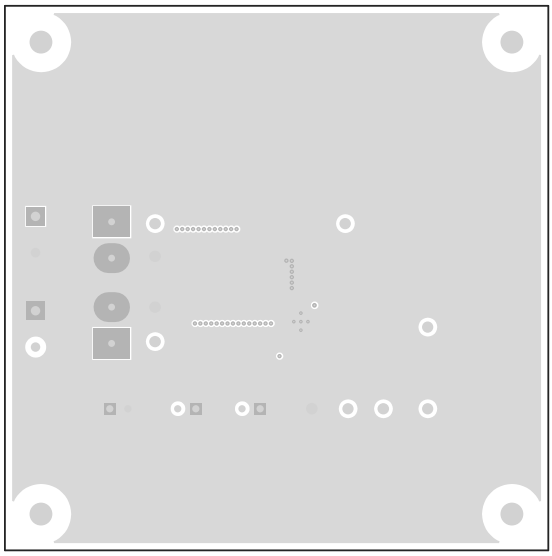


**Figure 23. TPS54561EVM-555 Layer 2 Layout**

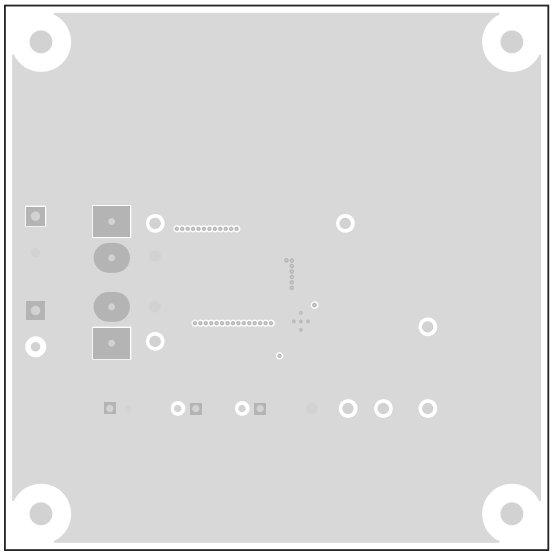


**Figure 24. TPS54561EVM-555 Layer 3 Layout**

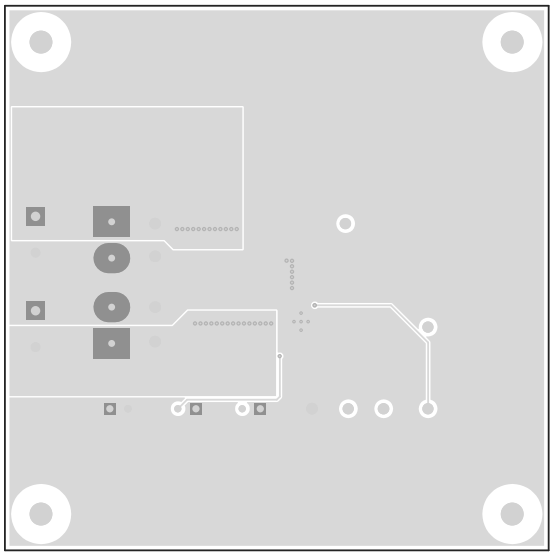


**Figure 25. TPS54561EVM-555 Bottom-Side Layout**

## 3.2 Estimated Circuit Area

The estimated PCB area for the components used in this design is 1.025 $in^2$ (661 $mm^2$). This area does not include test points or connectors. This design uses 0603 components for easy modifications. The area can be reduced by using smaller-sized components.

# 4 Bill of Materials

Table 5 presents the bill of materials for the EVM.

**Table 5. TPS54561EVM-555 Bill of Materials**

| Designator | Quantity | Value | Description | PackageReference | PartNumber | Manufacturer |
|---|---|---|---|---|---|---|
| PCB | 1 | | Printed Circuit Board | | PWR555 | Any |
| C1, C2, C3, C10 | 4 | 2.2uF | CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210 | 1210 | GRM32ER72A225KA35L | MuRata |
| C4 | 1 | 0.1uF | CAP, CERM, 0.1uF, 10V, +/-10%, X7R, 0603 | 0603 | STD | STD |
| C5 | 1 | 4700pF | CAP, CERM, 4700pF, 50V, +/-5%, X7R, 0603 | 0603 | STD | STD |
| C6, C7, C9 | 3 | 47uF | CAP, CERM, 47uF, 16V, +/-20%, X5R, 1210 | 1210 | GRM32ER61C476ME15L | MuRata |
| C8 | 1 | 47pF | CAP, CERM, 47pF, 50V, +/-5%, C0G/NP0, 0603 | 0603 | STD | STD |
| C13 | 1 | 0.01uF | CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0603 | 0603 | STD | STD |
| D1 | 1 | 60V | Diode, Schottky, 60V, 7A, PowerDI5 | PowerDI5 | PDS760-13 | Diodes Inc. |
| J1, J2 | 2 | ED120/2DS | Terminal Block, 2-pin, 15-A, 5.1mm | 0.40 x 0.35 inch | ED120/2DS | OST |
| J3, J4, J5 | 3 | | Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator | TSW-102-07-G-S | TSW-102-07-G-S | Samtec, Inc. |
| L1 | 1 | 7.2uH | Inductor, Shielded, Metal Composite, 7.2uH, 6A, 0.0113 ohm, SMD | 10.2 x 6.4 x 10.2mm | 7447798720 | Wurth Elektronik eiSos |
| LBL1 | 1 | | Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll | PCB Label 1.25"H x 0.250"W | THT-13-457-10 | Brady |
| R1 | 1 | 442k | RES, 442k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R2 | 1 | 90.9k | RES, 90.9k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R3 | 1 | 243k | RES, 243k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R4 | 1 | 16.9k | RES, 16.9k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R5 | 1 | 53.6k | RES, 53.6k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R6 | 1 | 10.2k | RES, 10.2k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R7 | 1 | 49.9 | RES, 49.9 ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| R8 | 1 | 1.00k | RES, 1.00k ohm, 1%, 0.1W, 0603 | 0603 | STD | STD |
| SH-J3 | 1 | 1x2 | Shunt, 100mil, Gold plated, Black | Shunt | SNT-100-BK-G | Samtec |
| TP1, TP6, TP7, TP9 | 4 | Red | Test Point, TH, Multipurpose, Red | Keystone5010 | 5010 | Keystone |
| TP2, TP3, TP8 | 3 | Black | Test Point, TH, Multipurpose, Black | Keystone5011 | 5011 | Keystone |
| TP4 | 1 | Orange | Test Point, TH, Multipurpose, Orange | Keystone5013 | 5013 | Keystone |
| TP5, TP10 | 2 | Yellow | Test Point, TH Multipurpose, Yellow | Keystone5014 | 5014 | Keystone |
| U1 | 1 | TPS54561DPR | 60 V Input, 5 A, Step Down DC-DC Converter with Soft-Start and Eco-mode | DPR | TPS54561DPR | Texas Instruments |
| C11, C12 | 0 | Open | Capacitor, Aluminum, 20% | Multi sizes | Engineering Only | Any |

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