User's Guide

TPS54020 SWIFT™ Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains background information for the TPS54020 as well as support documentation for the TPS54020EVM-082 evaluation module (EVM). Also included are the performance specifications, the schematic, and the bill of materials.

Table of Contents

List of Figures

List of Tables

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1 Introduction

1.1 Background

The TPS54020 dc/dc converter is designed to provide up to 10-A output current. The TPS54020 implements split-input power rails with separate input voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 17 V whereas the control input (V_{IN}) is rated for 4.5 V to 17 V. This EVM provides connections for both inputs but is designed and tested using the PVIN connected to V_{IN}. The rated input voltage and output current range for the EVM are given in Table 1-1. This EVM is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54020 regulator. The switching frequency is externally set by a resistor at a nominal 500 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54020 package along with the gate-drive circuitry. The low drain-to-source ON resistance of the MOSFET allows the TPS54020 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54020 provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 20 V for the EVM, but the recommended maximum input voltage of 17 V should not be exceeded.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54020EVM-082	VIN = 8 V to 17 V (V_{IN} start voltage = 7.5 V)	0 A to 10 A

1.2 Performance Specification Summary

A summary of the EVM performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 1.8 V, unless otherwise specified. This EVM is designed and tested for V_{IN} = 8 V to 17 V with the V_{IN} and PVIN pins connect together with the jumper J2. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. Performance Specifications

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range (PV_{IN} = V_{IN})			8	12	17	V
V_{IN} start voltage				7.5		V
V_{IN} stop voltage				7.1		V
Output voltage set point				1.8		V
Output current range	V_{IN} = 8 V to 17 V		0		10	A
Line regulation	I_O = 5 A, V_{IN} = 8 V to 17 V			±0.3%		
Load regulation	V_{IN} = 12 V, I_O = 0 A to 10 A			±0.5%		
Load transient response	I_O = 2.5 A to 47.5 A	Voltage change		–150		mV
		Recovery time		200		µS
	I_O = 47.5 A to 2.5 A	Voltage change		150		mV
		Recovery time		200		µS
Loop bandwidth	V_{IN} = 12 V, I_O = 1.9 A			30		kHz
Phase margin	V_{IN} = 12 V , I_O = 1.9 A			60		Degrees
Input ripple voltage	I_O = 10 A			300		mVpp
Output ripple voltage	I_O = 6 A			18		mVpp

Table 1-2. Performance Specifications (continued)

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output rise time			26		mS
Operating frequency			500		kHz
Peak efficiency	TPS54020EVM-082, V_{IN} = 12 V, I_O = 5 A		89%		

1.3 Modifications

These EVMs are designed to provide access to the features of the TPS54020. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

The output voltage is set by the resistor divider network of R7 and R10. The lower divider resistor R10 should not be modified and should remain at 2.55 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R7. Changing the value of R7 changes the output voltage between 0.6 V and 5 V. The value of R7 for a specific output voltage is calculated using Equation 1.

$$R7 = \frac{(V_{out} - V_{ref}) \times R10}{V_{ref}} \quad (1)$$

Table 1-3 lists the R7 values for some common output voltages. Note that V_{IN} must then be within a range so that the minimum on time is greater than 150 ns. The values given in Table 1-3 show both the ideal required values and the closest E96 standard values.

Table 1-3. Output Voltage Examples with R10 of 2.55 kΩ

DESIRED V_{OUT}	IDEAL R7	CLOSEST E96 MATCH	RESULTING V_{OUT}
1.8	5.100 kΩ	5.11 kΩ	1.802
2.5	8.075 kΩ	8.06 kΩ	2.496
3.3	11.475 kΩ	11.5 kΩ	3.306
5.0	18.700 kΩ	18.7 kΩ	5.000

1.3.2 Slow-Start Time

The slow-start time is adjusted by changing the value of C14. Use Equation 2 to calculate the required value of C14 for a desired slow-start time.

$$C14 = \frac{T_{SS} \times I_{SS}}{V_{ref}} \quad (2)$$

Where:

T_{SS} = desired slow start time
I_{SS} = slow start charging current = 2.3-µA nominal
V_{REF} = 0.6-V reference voltage

The EVM is set for a slow-start time of approximately 26 ms using C14 = 0.1 µF.

1.3.3 Adjustable UVLO

The undervoltage lockout (UVLO) is adjusted externally using R6 and R11. The EVM is set for a start voltage of 7.5 V and a stop voltage of 7.1 V using R6 = 69.8 kΩ and R11 = 13.3 kΩ. Use Equation 3 and Equation 4 to calculate required resistor values for different start and stop voltages.

UVLO Top Resistor

$$R6 = \frac{V_{Start} \times \left(\frac{V_{EN\ falling}}{V_{EN\ rising}} \right) - V_{Stop}}{I_p \times \left(1 - \frac{V_{EN\ falling}}{V_{EN\ rising}} \right) + I_h} \quad (3)$$

UVLO Bottom Resistor

$$R11 = \frac{R6 \times V_{EN\ falling}}{V_{Stop} - V_{EN\ falling} + R6 \times \left(I_p + I_h \right)} \quad (4)$$

Where:

Variable	Description	Nominal Value
V_{Start}	Desired start voltage	As desired, but must be greater than 4.4 V
V_{Stop}	Desired stop voltage	As desired, but must be greater than 4.2 V
V_{EN} falling	Enable pin stop threshold voltage	1.17-V nominal
V_{EN} rising	Enable pin start threshold voltage	1.21-V nominal
I_p	Enable pin source current while OFF	1.15-µA nominal
I_h	Enable pin hysteresis current	2.15-µA nominal

1.3.4 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. For most applications, the PVIN and V_{IN} inputs are connected together using a jumper across J2. When V_{IN} is connected to PVIN, only 1 input voltage is required and is supplied at J1. If desired, these two input voltage rails may be separated by removing the jumper across J2. Two input voltages must then be provided at both J1 and J4.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the EVM. The section also includes test results typical for the EVM and includes efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input / Output Connections

The EVM is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 5 A must be connected to J1, and a pair of 20-AWG wires is recommended. The jumper across J2 must be in place across pins 1 and 2. See Section 1.3.4 for split-input voltage rail operation. The load must be connected to J3 and a pair of 20-AWG wires is recommended. The load must be capable of drawing 10 A at 1.8 V. Wire lengths should be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the PVIN input voltages with TP6 providing a convenient ground reference. TP5 is used to monitor the output voltage with TP8 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	PVIN input voltage connector. (See Table 1-1 for V_{IN} range.)
J2	PVIN to VIN jumper. Shunt SH1 is normally connected from pin 1 to pin 2 to tie VIN to PVIN for common rail voltage operation.
J3	VOUT, 1.8 V at 10-A maximum.
J4	V_{IN} input voltage connector. Not normally used.
J5	2-pin header for enable. Connect EN to ground to disable, open to enable.
J6	2-pin header used to for sequencing via the slow start voltage.

Table 2-1. EVM Connectors and Test Points (continued)

Reference Designator	Function
TP1	Test point for PVIN.
TP2	Test point for Power Good. Biased from V_{OUT}.
TP3	Test point for SYNC OUT. In RT mode, this is a clock output. In SYNC mode, this is a digital input.
TP4	Test point for V_{IN}.
TP5	Test point for V_{OUT}.
TP6	Test point for PGND, near input.
TP7	Test point for PH, or Switch Node.
TP8	Test point for PGND, near output.
TP9	Test point between voltage divider network and output. Used for loop response measurements.
TP10	Test point for ENABLE.
TP11	Test point for the timing resistor RT and Clock.
TP12	Test point for slow start.
TP13	Test point for AGND.
TP14	Test point for AGND.

2.2 Efficiency

The efficiency of this EVM peaks at a load current between 3 A and 6 A and then decreases as the load current increases toward full load. Figure 2-1 shows the efficiency for the EVM at an ambient temperature of 25°C.

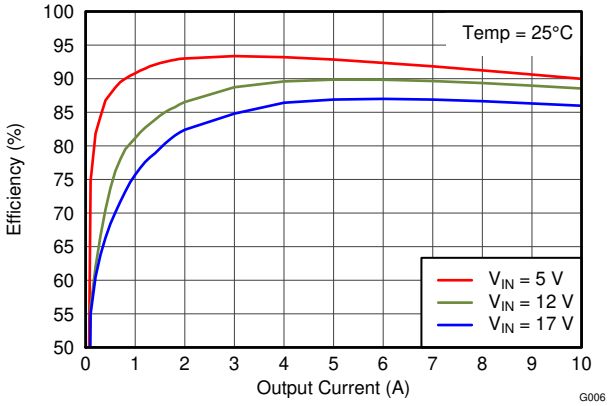

Figure 2-1. EVM Efficiency at 25°C

The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance R_{DS_ON} of the internal MOSFETs.

2.3 Output Voltage Load Regulation

Figure 2-2 shows the load regulation for the EVM.

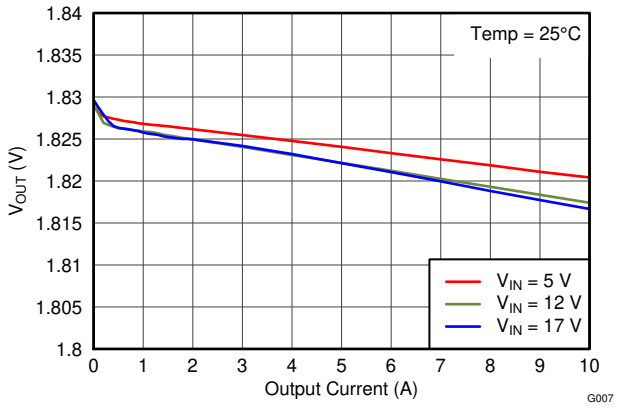

Figure 2-2. TPS54020EVM-082 Load Regulation

2.4 Output Voltage Line Regulation

Figure 2-3 shows the line regulation for the TPS54020EVM-082.

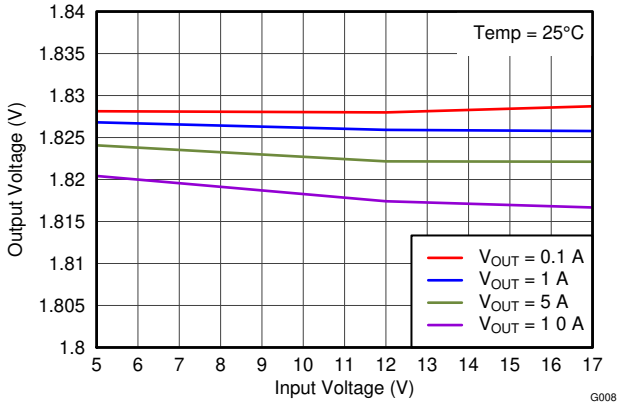

Figure 2-3. TPS54020EVM-082 Line Regulation

2.5 Load Transient

Figure 2-4 shows the EVM response to load transients. The current step is from 0 A to 4.7 A with an input voltage of 5 V. The transient was applied by switching in a real resistor load. The current step slew rate is approximately 50 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Parameter	Description
Bottom Trace	Output current switching between 2.5 A and 7.5 A, 2.5 A/div
Top trace	Output voltage, AC coupled, at 100 mV/div
Time Scale	200 µs/div
Conditions	Input voltage = 12 V, temperature = 25°C

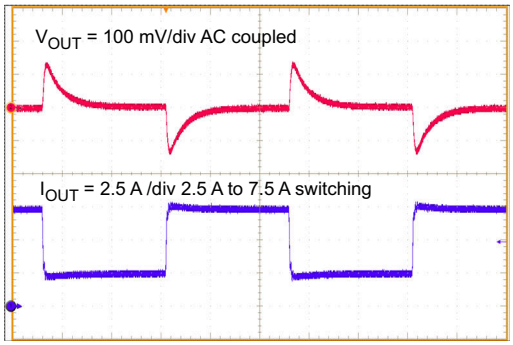

Figure 2-4. TPS54020EVM-082 Transient Response

2.6 Control Loop Response

Figure 2-5 shows the EVM control loop response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V and a constant resistance load current of 5 A.

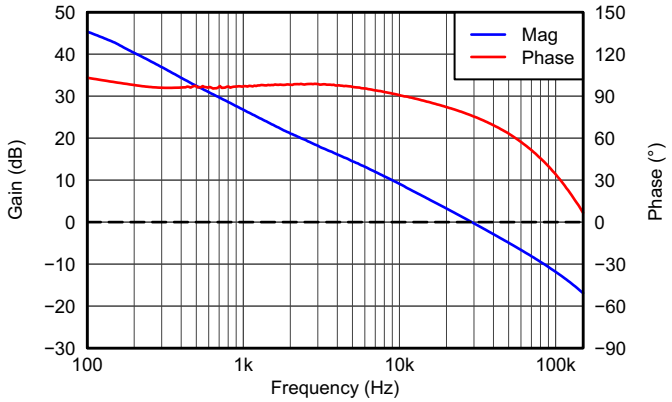

Figure 2-5. TPS54020EVM-082 Loop Bode Response

2.7 Output Voltage Ripple

Figure 2-6 shows the TPS54020EVM-082 output voltage ripple. The output current is the rated full load of 10 A and V_{IN} = 12 V. The ripple voltage is measured directly across the output capacitors.

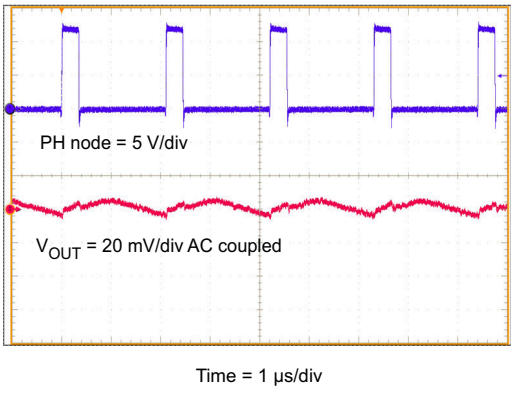

Figure 2-6. TPS54020EVM-082 Output Ripple

2.8 Input Voltage Ripple

Figure 2-7 shows the EVM input voltage ripple. The output current is the rated full load of 10 A and V_{IN} = 12 V. The ripple voltage is measured directly across the input capacitors.

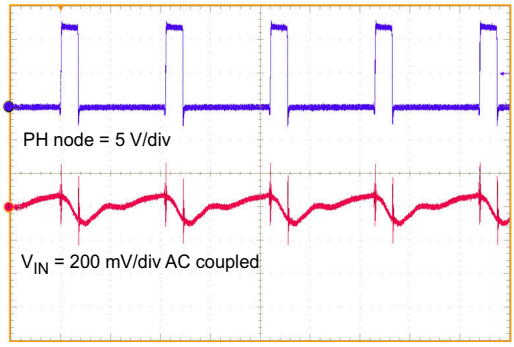

Figure 2-7. TPS54020EVM-082 Input Ripple

2.9 Start Up

Figure 2-8 and Figure 2-9 show the start-up waveforms for the EVM. In Figure 2-8, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R6 and R11 resistor divider network. In Figure 2-9, the input voltage is initially applied and the output is inhibited by using a jumper at J5 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.8 V. The input voltage for these plots is 12 V and the load is 10-A resistive load.

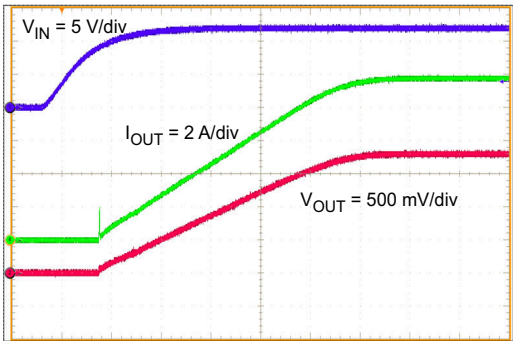

Figure 2-8. TPS54020EVM-082 Start Up with V_{IN}

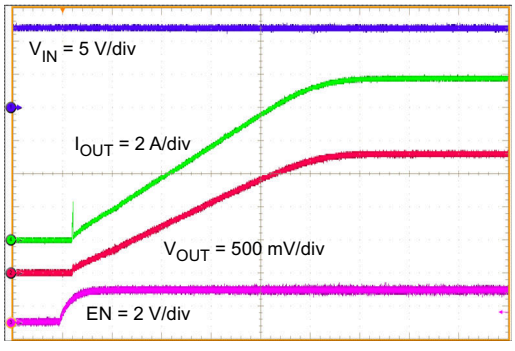

Figure 2-9. TPS54020EVM-082 Start Up with EN

2.10 Pre-Bias Start Up

The TPS54020 is designed to start up into a pre-biased output. The output voltage is not discharged to ground at the beginning of the slow-start sequence, but only starts to increase towards regulation once the slow start voltage reaches the pre-bias bus voltage. Figure 2-10 shows the start-up waveform with the output voltage pre-biased to 1 V.

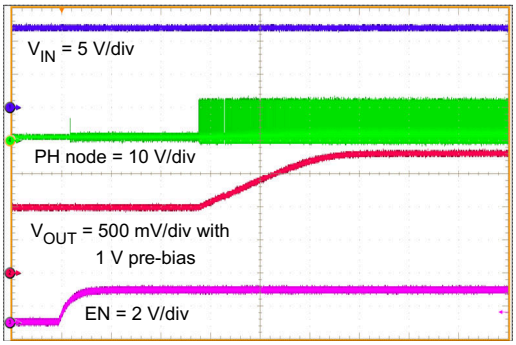

Figure 2-10. TPS54020EVM-082 Pre-Bias Startup

2.11 Hiccup Mode Current Limit

The EVM features hiccup mode current limit. When an overcurrent event occurs, the device shuts down and restarts. Figure 2-11 shows the hiccup restart sequence in an over current condition.

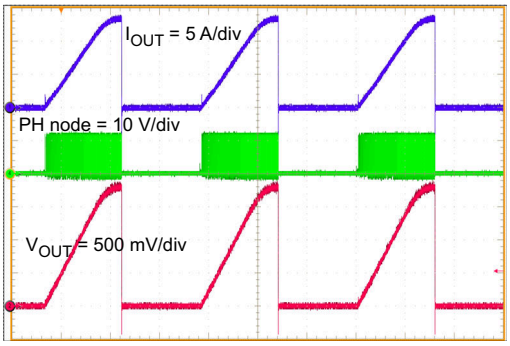

Figure 2-11. TPS54020EVM-082 Hiccup Mode Current Limit

3 Board Layout

This section provides a description of the EVM board layout and layer illustrations.

3.1 Layout

The board layout for the EVM is shown in Figure 3-1 through Figure 3-6. The top-side layer of the EVM is laid out in a manner typical of a user application. All 4 layers (top, bottom, and 2 internal) are 2-oz copper.

The top layer contains the main power traces for PVIN, V_{IN}, V_{OUT} and VPHASE. Also on the top layer are connections for several analog pins of the TPS54020 and a large area filled with PGND. The two internal layers are the same and contain mostly power planes, including PGND, V_{OUT}, PVIN and VPHASE. The bottom layer contains the remainder of the analog circuit connections, plus power planes similar to the internal layers. The top-side power and ground planes are connected to the bottom and internal power and ground planes with multiple vias placed around the board including several vias directly under the TPS54020 device to provide a thermal path from the top-side power planes to the other layer power planes.

The input decoupling capacitor C4 and bootstrap capacitor C5 are both located as close to the IC as possible. Additionally, the voltage set-point resistor divider components are kept close to the IC. The location of the connection to the voltage divider network at R5 defines the point of regulation, which is the copper VOUT trace at the output connector J3. For the TPS54020, an additional input bulk capacitor is included to effectively reduce the source impedance from the input supply to the switcher. Critical analog circuits such as the voltage setpoint divider, frequency set resistor, slow-start capacitor, and compensation components are terminated to analog ground (AGND) using a ground trace that is separate from the power ground plane.

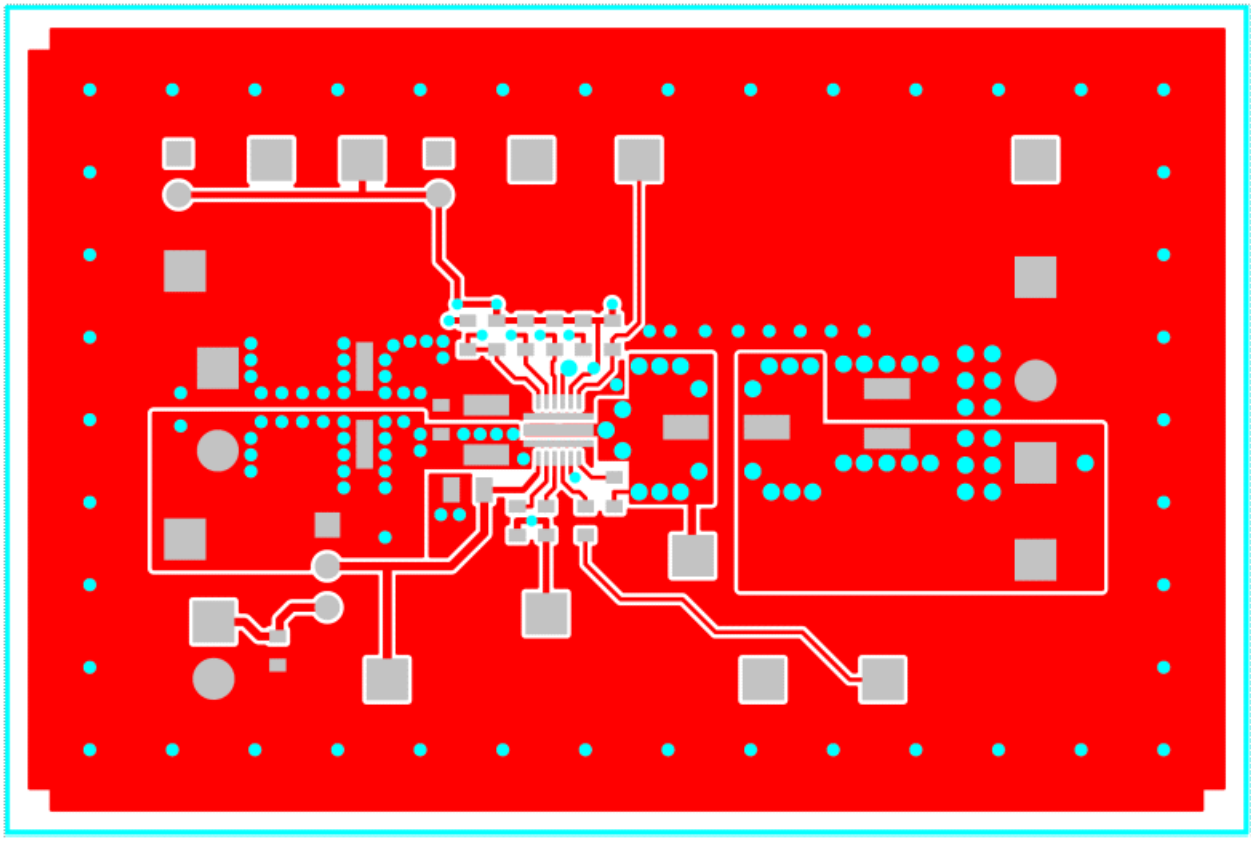

Figure 3-1. TPS54020EVM-082 Top Side Copper

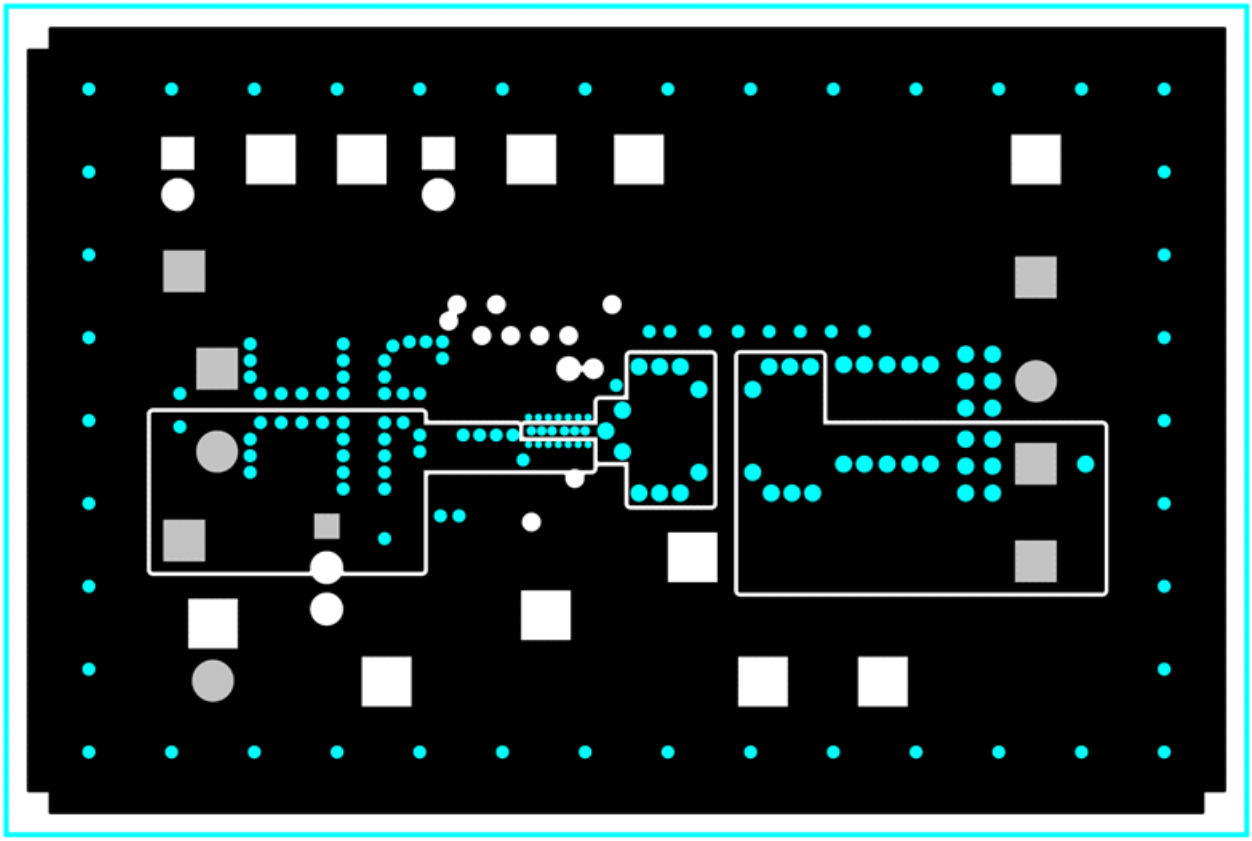

Figure 3-2. TPS54020EVM-082 Internal 1 Copper

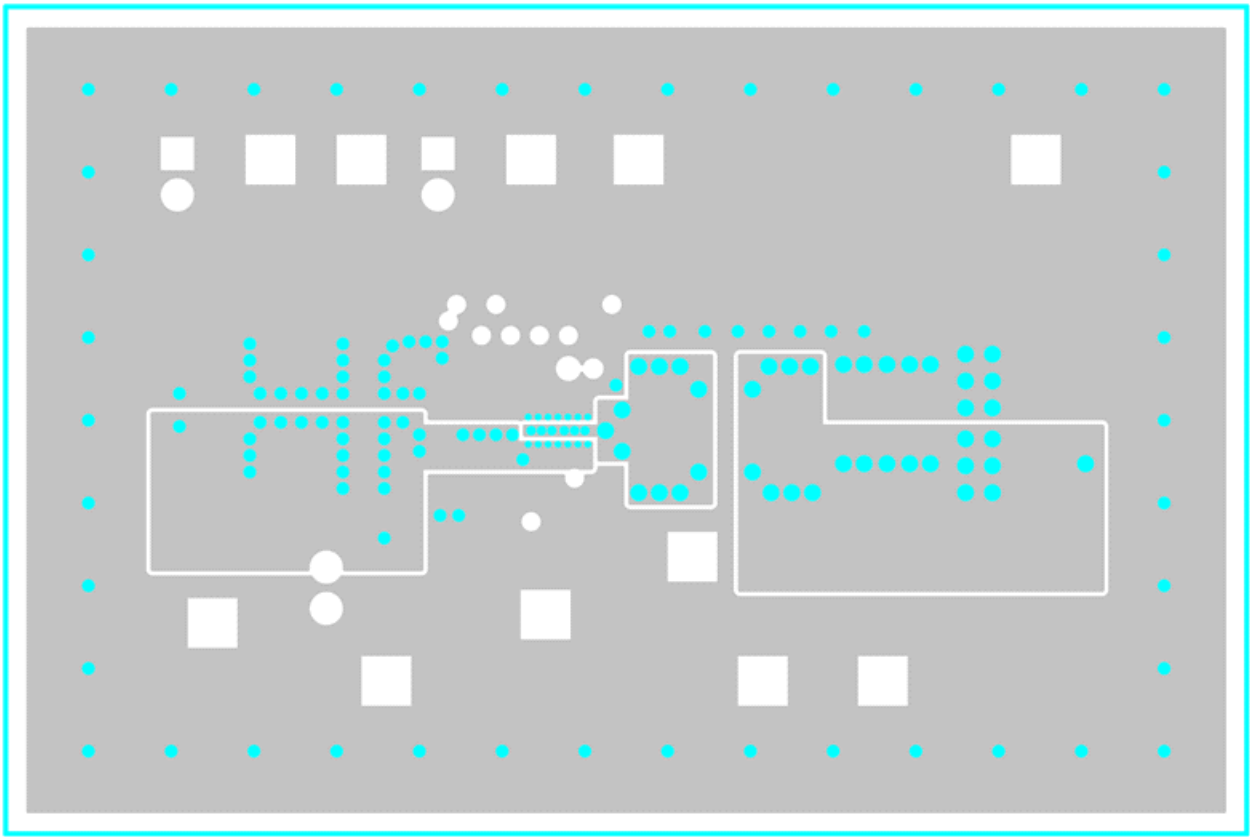

Figure 3-3. TPS54020EVM-082 Internal 2 Copper

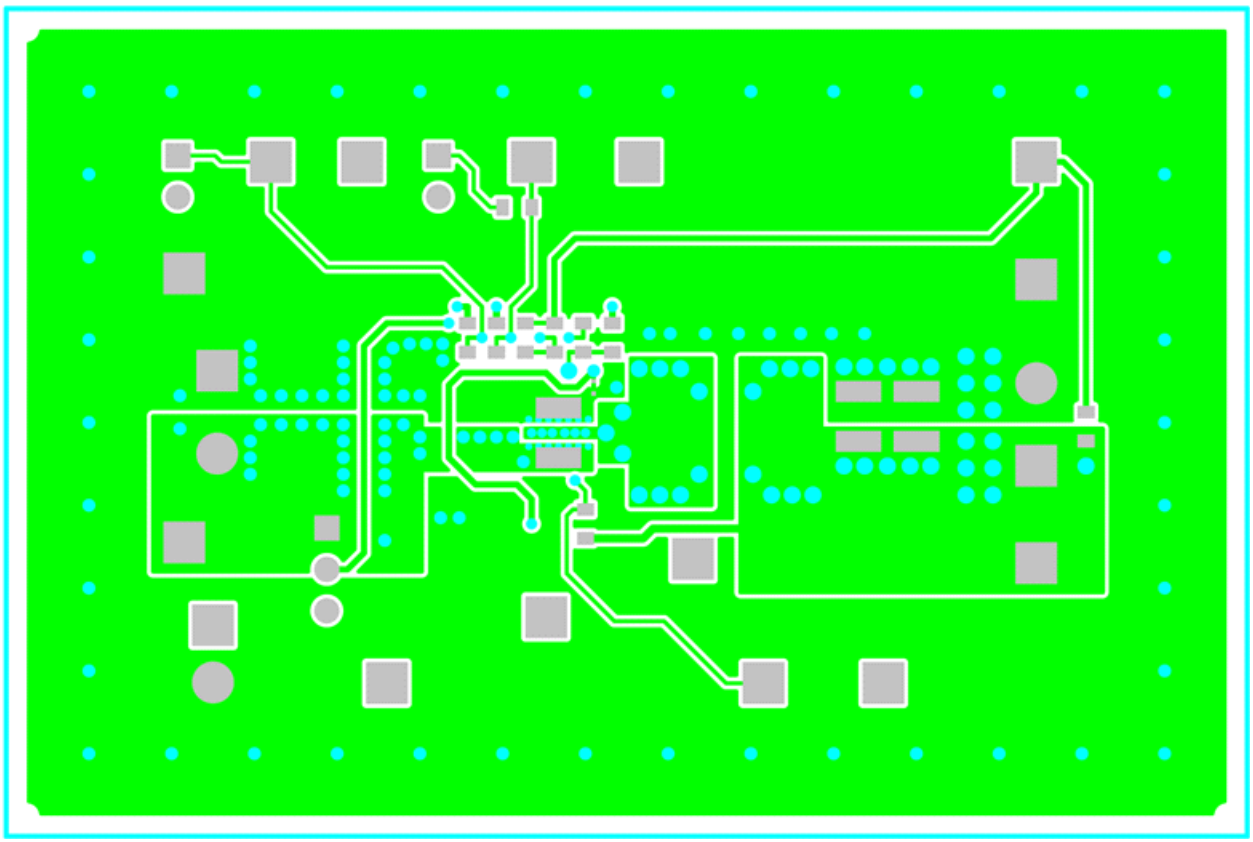

Figure 3-4. TPS54020EVM-082 Bottom Side Copper

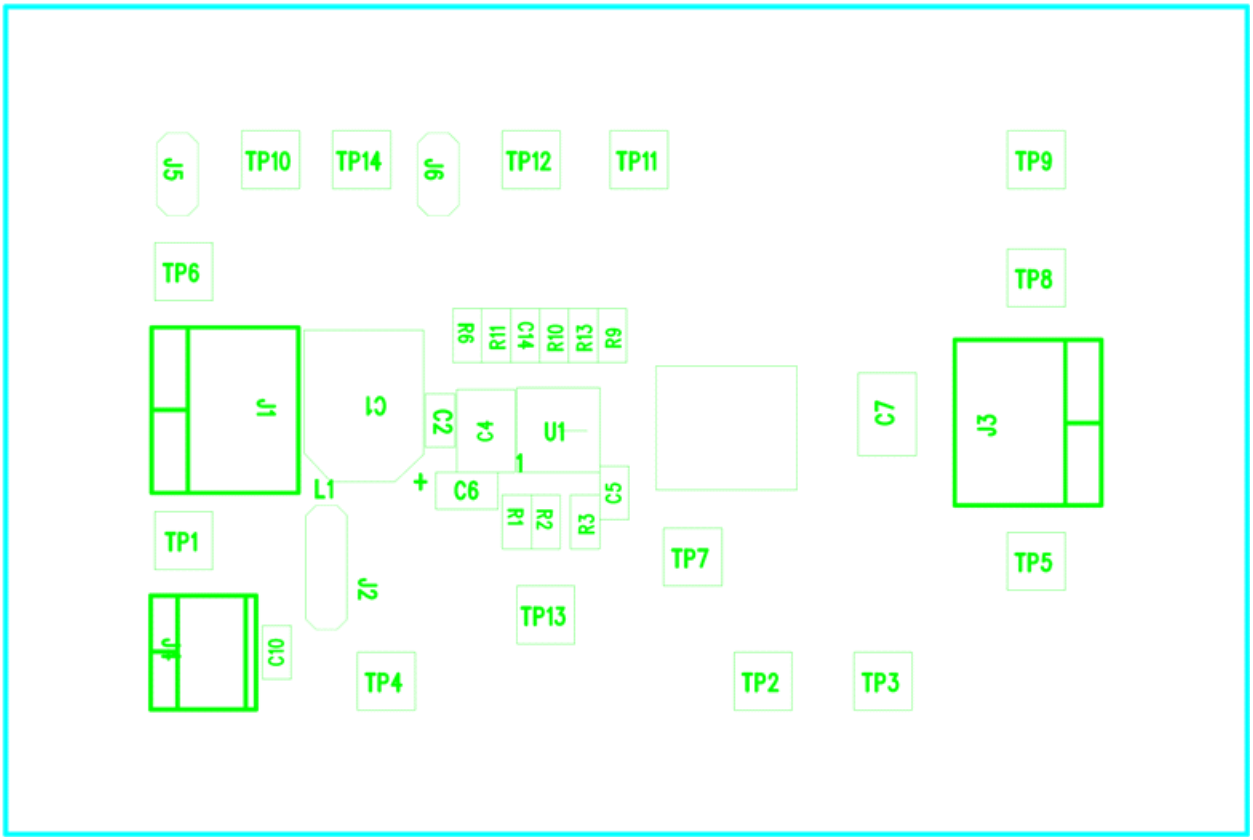

Figure 3-5. TPS54020EVM-082 Top Side Component Placement

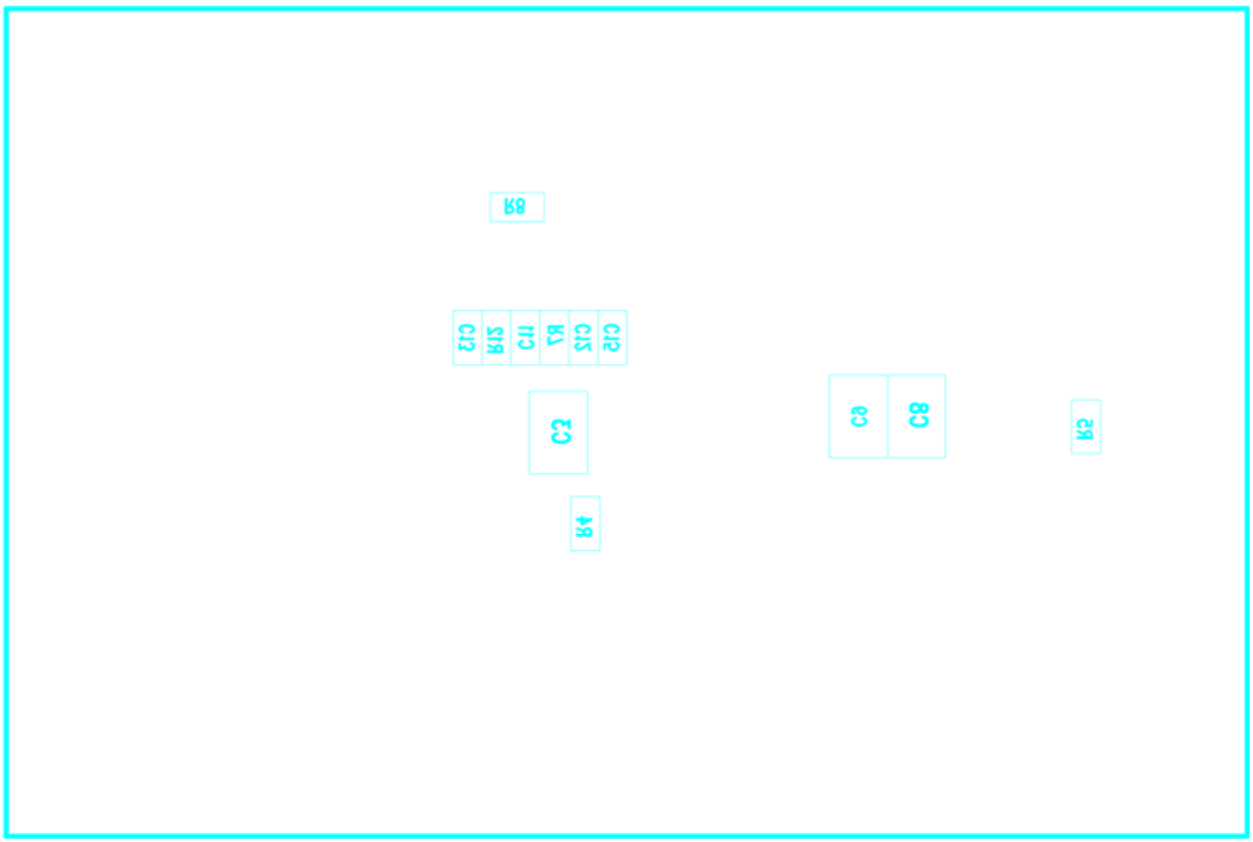

Figure 3-6. TPS54020EVM-082 Bottom Side Component Placement

4 Schematic and Bill of Materials

This section presents the EVM schematic and bill of materials.

4.1 Schematic

Figure 4-1 shows the schematic for the EVM.

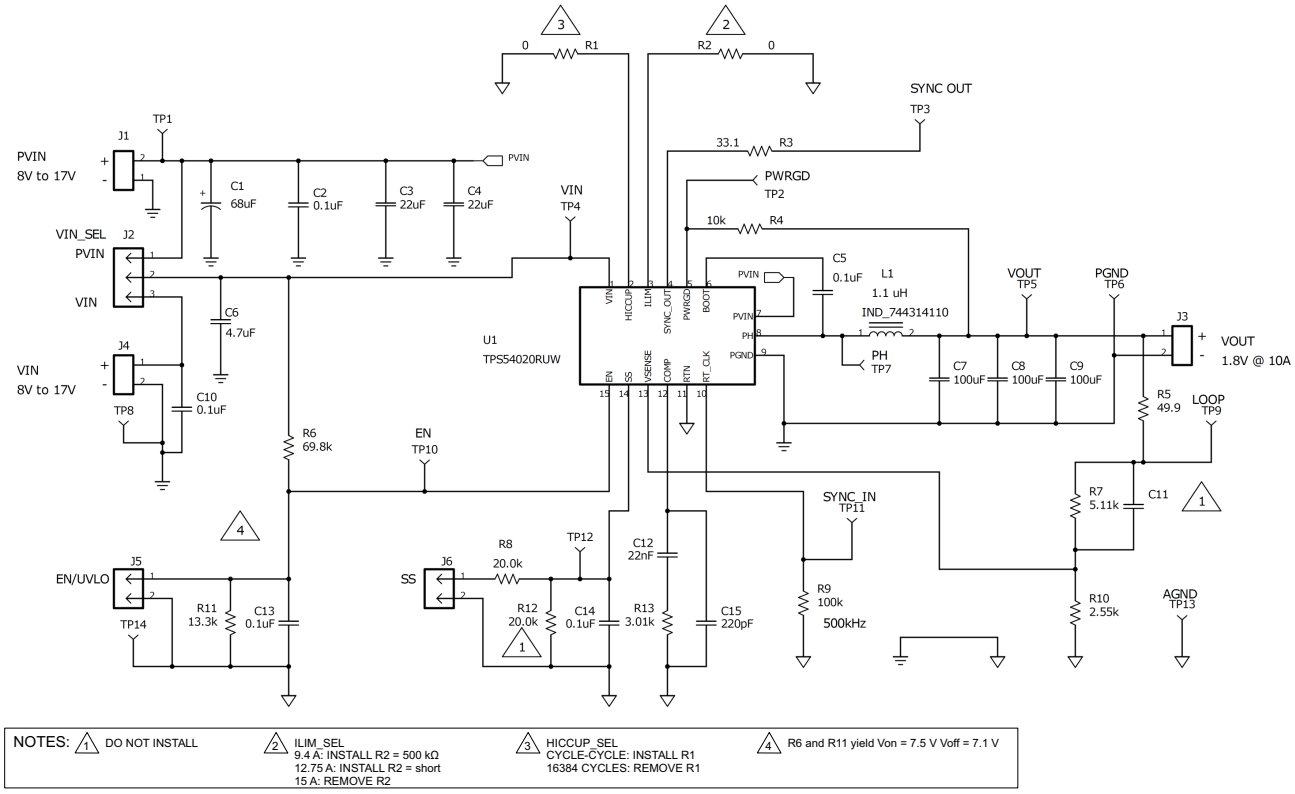

Figure 4-1. TPS54020EVM-082 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the EVM.

Table 4-1. TPS54020EVM-082 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	Mfr
1	C1	68 µF	Capacitor, aluminum, 25 V, ±20%	0.260 × 0.276 in	EEE-FK1E680P	Panasonic
5	C2, C5, C10, C13, C14	0.1 µF	Capacitor, ceramic, 25 V, X7R, 10%	603	Std	Std
2	C3, C4	22 µF	Capacitor, ceramic, 25 V, X5R, 10%	1210	Std	Std
1	C6	4.7 µF	Capacitor, ceramic, 25 V, X5R, 10%	805	Std	Std
3	C7, C8, C9	100 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	1210	Std	Std
0	C11	820 pF	Capacitor, ceramic, 50 V, X7R, 10%	603	Std	Std
1	C12	22 nF	Capacitor, ceramic, 16 V, X7R, 10%	603	Std	Std
1	C15	220 pF	Capacitor, ceramic, 50 V, X7R, 10%	603	Std	Std
2	J1, J3	ED120/2DS	Terminal block, 2 pin, 15 A, 5.1 mm	0.40 × 0.35 in	ED120/2DS	OST
1	J2	PEC03SAAN	Header, male 3 pin, 100-mil spacing	0.100 in × 3	PEC03SAAN	Sullins
1	J4	ED555/2DS	Terminal block, 2 pin, 6 A, 3.5 mm	0.27 × 0.25 in	ED555/2DS	OST
2	J5, J6	PEC02SAAN	Header, male 2 pin, 100-mil spacing,	0.100 in × 2	PEC02SAAN	Sullins
1	L1	1.1 µH	Inductor, power choke, 20 ±%	6.9 × 7 mm	744314110	IND_744314110
0	R1	0	Resistor, chip, 1/16W, 1%	603	Std	Std
0	R2	0	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R3	33.1	Resistor, chip, 1/16W, 1%	603	Std	Std
3	R4	10k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R7	5.11k	Resistor, chip, 1/16W, 1%	604	Std	Std
1	R5	49.9	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R6	69.8k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R8	20.0k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R9	100k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R10	2.55k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R11	13.3k	Resistor, chip, 1/16W, 1%	603	Std	Std
0	R12	20.0k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	R13	3.01k	Resistor, chip, 1/16W, 1%	603	Std	Std
1	Shunt1	NA	Shunt, 100-mil, black	0.100 in	929950-00	3M
2	TP1, TP5	5010	Test point, red, thru hole	0.125 × 0.125 in	5010	Keystone
6	TP2, TP3, TP4, TP10, TP11, TP12	5012	Test point, white, thru hole	0.125 × 0.125 in	5012	Keystone
4	TP6, TP8, TP13, TP14	5011	Test point, black, thru hole	0.125 × 0.125 in	5011	Keystone
2	TP7, TP9	5013	Test point, orange, thru hole	0.125 x 0.125 in	5013	Keystone
1	U1	TPS54020RUW	IC, 4.5 V–17 V input, 10-A sync. step down SWIFT converter	QFN	TPS54020RUW	TPS54020RUW
1	—		PCB, 3.0 in × 2.0 in × 0.062 in		PWR082	Any
Note 1. This assembly is ESD sensitive. Observe ESD precautions.						

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2012) to Revision A (November 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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