User's Guide

TPS54120 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide describes the operational use of the TPS54120 Evaluation Module (PWR103) as a reference design for engineering demonstration and evaluation of the TPS54120, low-noise 1-A power supply. Included in this user's guide are the following:

- Setup and operation instructions
- Schematic diagram
- Layout description
- Bill of materials
- Test results

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1 Background

The Texas Instruments TPS54120 EVM (PWR103) helps design engineers evaluate the operation and performance of the TPS54120 (Switcher + LDO) for possible use in their own circuit application. This particular EVM configuration contains all of the external components required for a low-noise 1-A solution with internal thermal and current limit shutdowns, and enable circuitry in a 3.5-mm × 5.5-mm, QFN, thermally enhanced PowerPad™ package.

The power input of the IC (PVIN) is rated for 1.6 V to 17 V while the control input (VIN) is rated for 4.5 V to 17 V. The TPS54120 provides both inputs, but this EVM is designed and tested using the PVIN connected to VIN with a minimum input voltage of 7 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the TPS54120 device. The switching frequency is externally set at a nominal 480 KHz.

The integrated switcher (SW) and LDO are optimized to allow the TPS54120 to achieve high efficiencies and a low output noise. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable LDO output voltage from 0.8 V to 6 V. Additionally, the TPS54120 provides adjustable slow start, tracking, and enable inputs. The TPS54120, including other external components that is capable of delivering up to 1-A low noise supply to the load.

Table 1-1. EVM Specifications

EVM	INPUT VOLTAGE	SW OUTPUT VOLTAGE	LDO OUTPUT VOLTAGE	OUTPUT CURRENT
TPS54120	7 V – 17 V	4.1 V	3.3 V	0 A – 1 A

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS54120EVM.

2.1 Input and Output Connections and Jumper Descriptions

- **J1-LDO OUT and J2-GND:** The output of the LDO and the ground connector. The default setting is 3.3 V. This is the low noise output from the TPS54120.
- **J3-VIN and J4-GND:** Input power supply voltage and the ground connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added across J3 and J4 if the supply leads are greater than six inches. For example, an additional 47-µF electrolytic capacitor across J3 and J4 can improve the transient response of the TPS54120 while eliminating unwanted ringing on the input due to long wire connections.
- **J5:** The SMA connector for the output voltage of the LDO. The connector for J5 is not populated on the TPS54120EVM (PWR103). This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements.
- **J7-SW OUT and J6-GND:** The output of the SW and the ground connector. This is the output voltage from the switcher converter and the input voltage to the LDO. The default setting is 4.1 V.
- **J8:** The SMA connector for the output voltage of the SW. The connector for J8 is not populated on the TPS54120EVM (PWR103). This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements.

- **JP1-LDOEN:** LDO enable. To enable the output of the LDO, connect this jumper from the center pin to the “on” pin. This will connect the enable pin to the LDO input supply. To disable, connect this jumper from the center pin to the “off” pin. This will short the LDO enable pin to ground.
- **JP2:** The jumper connection between the output of the switcher converter to the LDO input. A shorting jumper is required for normal operation. If you want to disconnect the LDO from the SW, remove the shorting jumper wire.
- **JP3-SW EN:** Switcher converter enable jumper. To enable the SWITCHER output, leave this jumper unconnected (there is an internal pullup on this pin). To disable, install a shorting jumper. This will short the enable pin to ground.
- **TP1-PWRGD:** The power-good connector test point. It is power-good open-collector flag for the switcher converter. Tie this pin through a 10-k resistor to a regulated supply < 5.5 V to monitor the status of the switcher converter output.
- **TP2-SENSE:** The SW sense (feedback) pin test point
- **TP3-SW OUT:** This is the positive switcher output test point. In addition to J7, this test point can also be used to measure the output voltage of the switcher.
- **TP4-LDO IN:** The LDO input voltage test point
- **TP5-LDO OUT:** The LDO output test point. In addition to J1, this test point can also be used to measure the output voltage of the LDO.

2.2 Modifications

These evaluation modules are designed to provide access to the features of the TPS54120. However, some modifications can be made to this module.

2.2.1 SW Output Voltage Setpoint

The output voltage of the switcher is set by the resistor divider network of R5 and R6. R6 is fixed at 10 kΩ. To change the switcher output voltage of the EVM, it is necessary to change the value of resistor R5. The value of R5 for a specific output voltage can be calculated using Equation 1. Note that the SW output must be 0.8 V above the LDO output for best PSR and noise performance.

$$R5 = 10\ k\Omega\ (SW\ V_{OUT} - 0.8\ V) / (0.8\ V) \quad (1)$$

Table 2-1 lists the R5 values for some common output voltages. The values given in Table 2-1 are standard values, not the exact value calculated using Equation 1.

Table 2-1. Sample 1% Resistor Values for Common SW Output Voltages

SW OUTPUT VOLTAGE (V)	R5 VALUE (kΩ)
1.8	12.4
2.5	21.5
3.3	31.6
4.1	41.2
5	52.3
6	64.9

2.2.2 LDO Output Voltage Setpoint

The output voltage of the LDO also can be set by an external resistor divider network (R1 and R2). R2 is fixed at 10kΩ. To change the LDO output voltage of the EVM, it is necessary to change the value of resistor R1. Changing the value of R1 can change the output voltage from 0.8 V to 6 V. The value of R1 for a specific output voltage can be calculated using Equation 2. Note that the LDO output should be 0.8 V below the SW output for best PSR and noise performance.

$$R1 = 10\ k\Omega\ (LDO\ V_{OUT} - 0.8\ V) / (0.8\ V) \quad (2)$$

Table 2-2 lists the R1 values for some common output voltages. Note that the minimum V_{IN} equals V_{OUT} + VDO or 2.2 V, whichever is greater. The values given in Table 2-2 are standard values, not the exact value calculated using Equation 2.

Table 2-2. Sample 1% Resistor Values for Common LDO Output Voltages

LDO OUTPUT VOLTAGE (V)	R1 VALUE (kΩ)
0.8	0 (Short)
1	2.49
1.2	4.99
1.5	8.87
1.8	12.5
2.5	21
3.3	30.9
5	52.3

2.2.3 Switcher Slow-Start Time

The slow-start time can be adjusted by changing the value of C7. Use Equation 3 to calculate the required value of C7 for a desired slow-start time (T_{SS}).

$$C7(nF) = T_{SS}(ms)\ I_{SS}(\mu A) / V_{REF}(V) \quad (3)$$

Basically, the device has an internal pullup current source of I_{SS} = 2.3 µA that charges the external slow-start capacitor, C7. The voltage reference V_{REF} (V) for this part is 0.8 V.

2.2.4 LDO Start-Up

The start-up time of the LDO can be adjusted by changing the value of C13. In addition to start-up time, the capacitor on the NR pin is used for noise reduction as well. However, the noise reduction effect is nearly saturated at 0.01 µF.

2.3 Equipment Interconnect

- Turn off the input power supply after verifying that its output voltage is set to the desired supply voltage (less than 17 V) and the current limit is set to approximately 500 mA. Connect the positive voltage lead from the input power supply to J3 (VIN) and the ground lead to J4 (GND).
- Connect a 0-A to 1-A load (I_{Load}) between LDO OUT and GND using J1 and J2.
- Disable the output of the LDO by connecting a shorting jumper at JP1 from the “off” pin to the center pin (LDO EN).

3 Operation

- Turn on the input power supply. Verify that the switcher output voltage is near 4.1 V and the LDO output is near 0 V.
- Enable the LDO output by connecting the jumper on JP1 from the “on” pin to the center pin (LDO EN).
- Verify that the LDO output voltage is 3.3 V.
- Vary the load current and V_{IN} voltage as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TPS54120EVM (PWR103) characteristics of this EVM design.

4.1 Output Voltage Ripple

Figure 4-1 shows the output voltage ripple of the LDO and SWITCHER converter for the TPS54120EVM with V_{IN} = 12 V, SW OUT = 4.1 V, LDO OUT = 3.3 V, I_{OUT} = 400 mA, $F_{switching}$ = 480 kHz.

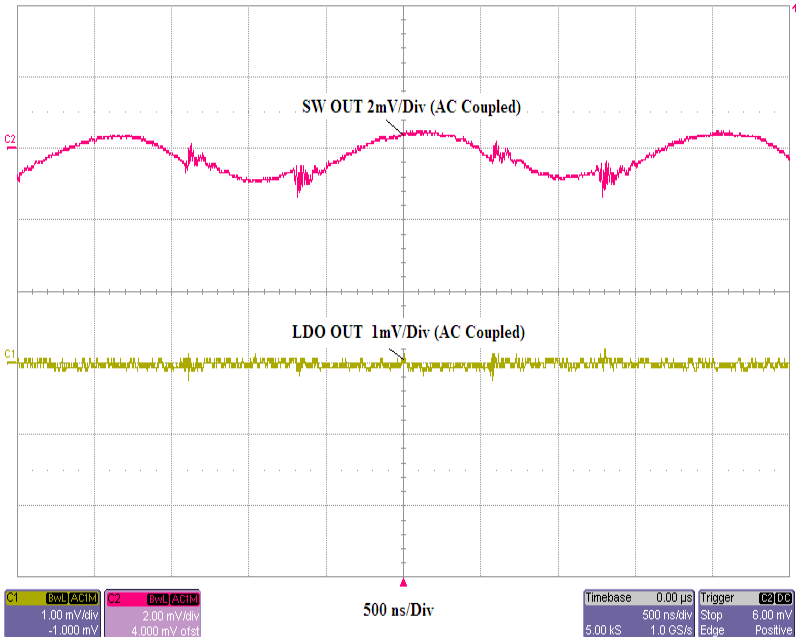

Figure 4-1. Output Voltages of Both the SW and LDO with a 400-mA Load

4.2 Output Noise

Figure 4-2 shows the output voltage noise spectrum for the TPS54120EVM with V_{IN} = 12 V, LDO OUT = 3.3 V, SW OUT = 4.1 V, I_{OUT} = 400 mA, $F_{switching}$ = 480 kHz.

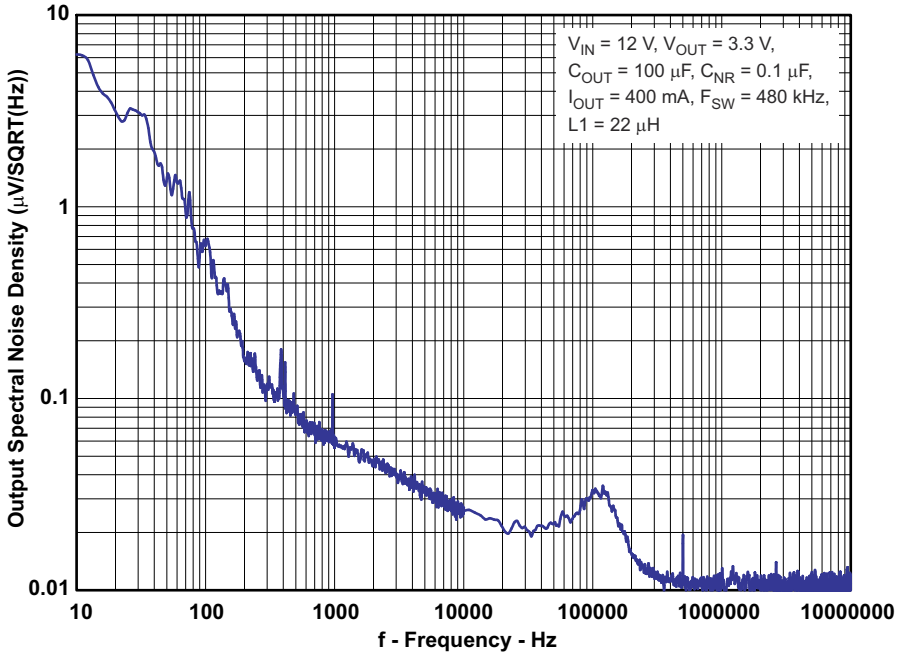

Figure 4-2. Output Spectrum Noise Density vs Frequency

4.3 Output Turn-On

Figure 4-3 shows the SW output voltage turn-on from the SW enable for the TPS54120EVM with V_{IN} = 12 V, SW OUT = 4.1 V, LDO OUT = 3.3 V, and I_{OUT} = 400 mA, $F_{switching}$ = 480 kHz.

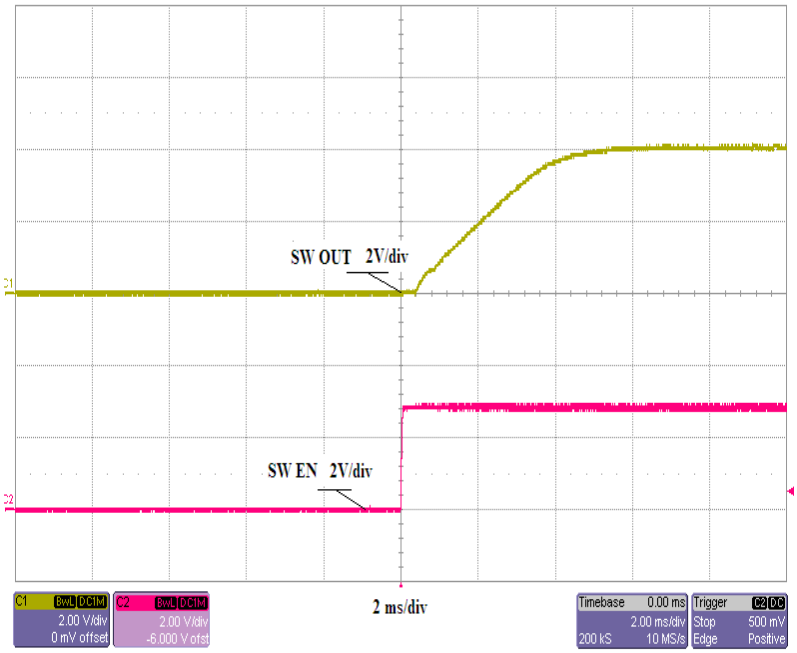

Figure 4-3. Switcher Converter Output Voltage Turn-On, SW Enable

Figure 4-4 shows the LDO output voltage turn-on from the LDO enable for the TPS54120EVM with V_{IN} = 12 V, SW OUT = 4.1 V, LDO OUT = 3.3 V, and I_{OUT} = 400 mA, $F_{switching}$ = 480 kHz.

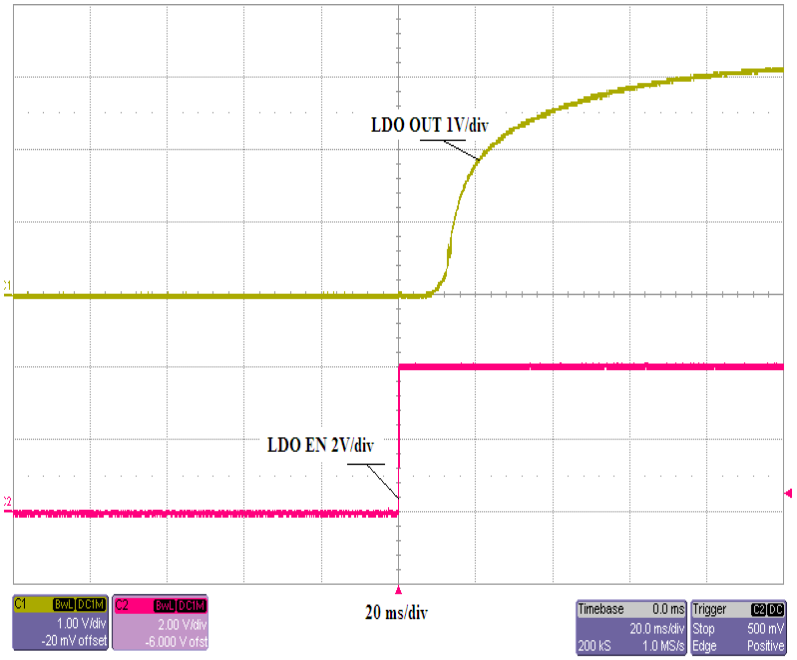

Figure 4-4. LDO Output Voltage Turn-On, LDO Enable

Figure 4-5 shows the LDO output voltage turn-on of TPS54120 from the SW enable for the TPS54120EVM with V_{IN} = 12 V, SW OUT = 4.1 V, LDO OUT = 3.3 V, and I_{OUT} = 400 mA, $F_{switching}$ = 480 kHz.

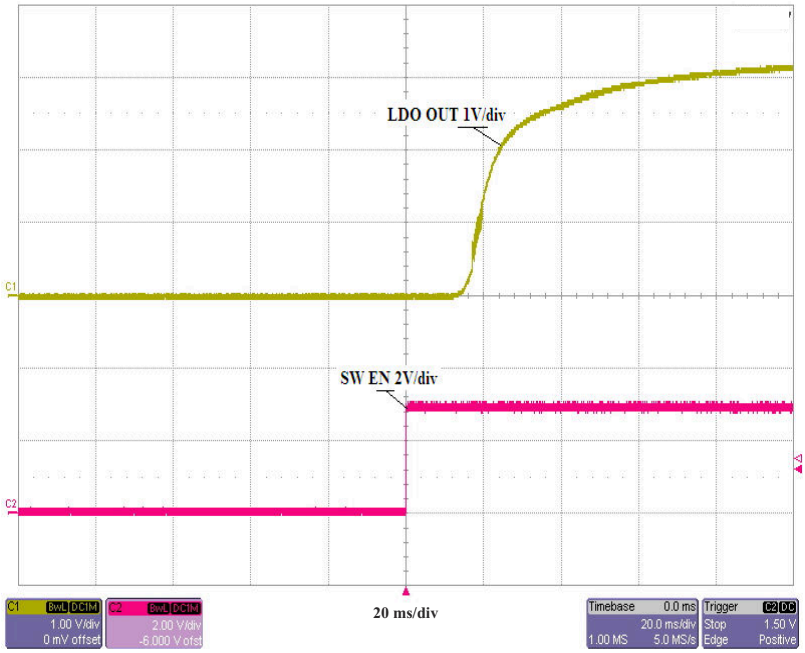

Figure 4-5. LDO Output Voltage Turn-On, SW Enable

4.4 Load Transient

Figure 4-6 shows the TPS54120 response to load transients. The current step is from 30% to 75% of the maximum rated load at 12-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output of both the switcher and the LDO.

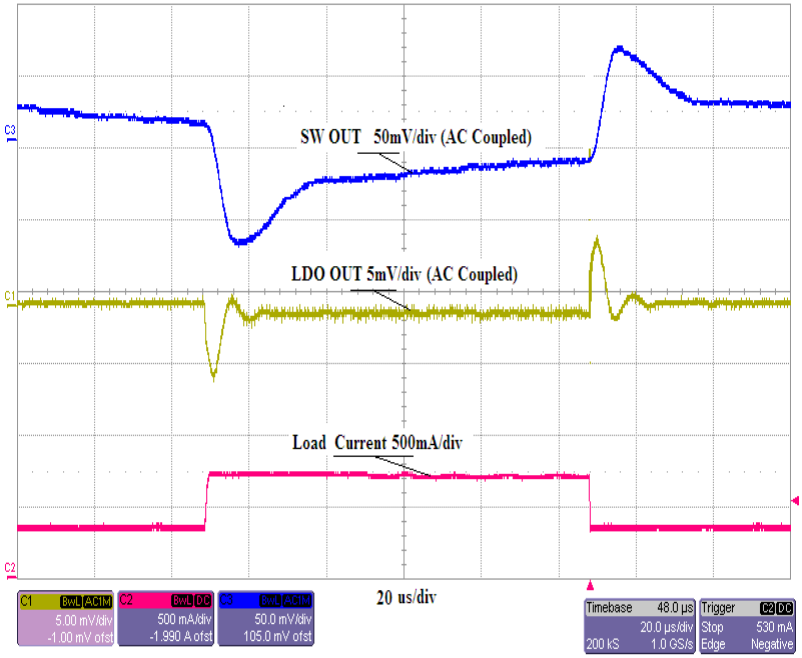

Figure 4-6. TPS54120 Transient Response

4.5 Efficiency

Figure 4-7 shows the efficiency for the TPS54120 at an ambient temperature of 25°C for V_{IN} = 8 V, 10 V, 12 V, and 15 V. The switcher output voltage is set to 4.1 V and the LDO is set to 3.3 V.

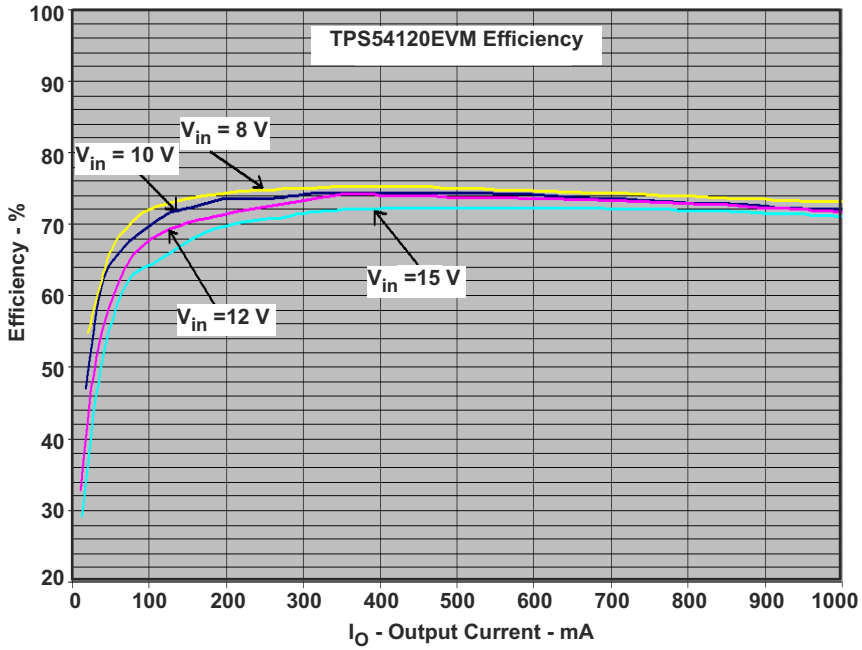

Figure 4-7. TPS54120 Efficiency

4.6 Thermal Characteristic

This section shows a thermal image of the TPS54120 running at a 12-V input and 1-A load, 3.3-V LDO OUT, and 4.1-V switcher out. There is no air flow and the ambient temperature is 25°C. The peak temperature of the IC (56.4°C) is well below the maximum recommended operating condition listed in the data sheet of 150°C.

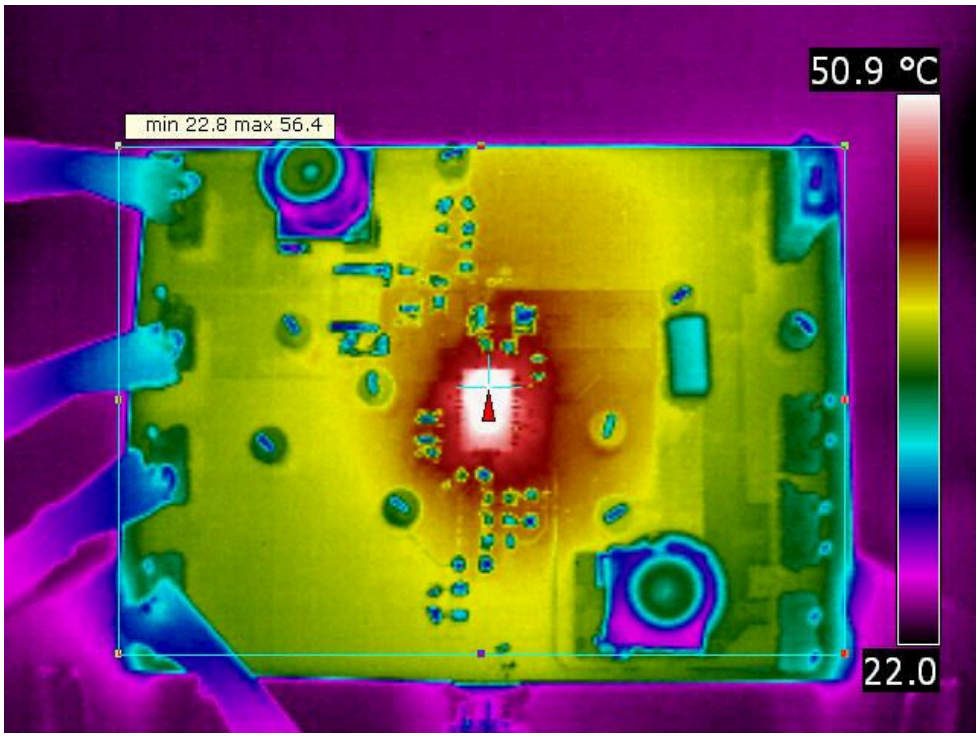

Figure 4-8. TPS54120 Thermal Image

5 Board Layout

This section provides a description of the TPS54120, board layout, and layer illustrations.

5.1 Layout Description

The board layout for the TPS54120 evaluation board is shown in Figure 5-1 through Figure 5-4. The board consists of four layers. It is laid out in such a way the analog ground of the LDO is shielded as much as possible from the noise of the switcher. Also, critical analog circuits such as the voltage set point divider, frequency set resistor, slow-start capacitor, and compensation components are terminated to ground using a via separate from the power ground pour. The top-side layer of the EVM is laid out in a manner typical of a user application.

The top layer contains the analog ground of the LDO and a portion of the output power ground of the SW side. The first internal layer is connected to the powerpad and the analog ground of the IC; mostly this layer is used for power dissipation. Only a few traces are implemented on this layer such as the LDO enable and the PWRGD test point trace.

The second internal layer is mostly used for analog ground as well. For shielding the LDO ground from the switch node noise, a small isolated power ground plane is made in the center of this layer to reduce capacitive coupling with analog ground. This layer also contains the input voltage trace of the switcher connecting the input capacitor and the connector J3.

About one quarter of the bottom layer contains the main input power ground trace. The inductor (L1) and the output capacitors (C9, C10) of the switcher are located in the center of the layer. The remaining surface area is connected to the analog ground of the top and the internal layers through vias. Some of these vias are directly under the TPS54120 device to provide a thermal path from the top-side ground plane to the internal and bottom-side ground plane.

The input decoupling capacitor of the SW (C5) is located as close as possible to the IC. PVIN and VIN are connected together in this EVM, and then through vias, they are connected to the input voltage trace in the second internal layer. Whereas, the decoupling capacitor ground is connected through vias to the bottom layer. The compensation and the soft-start capacitors (C6, C7, and C8), the CLK/RT resistor (R3), and the SW feedback resistor (R6) are grounded to a power-ground trace in the center of the top layer. This helps shield them from noises of the high current ground plane.

The inductor (L1), the boot capacitor (C12), and the output capacitors of the SW (C9, C10) are placed on the bottom layer of the board to shield the switching noise into the LDO side. However, the boot capacitor (C12) and the inductor (L1) are connected through vias directly into the PH pin of the IC. This connects them as close as possible to the PH pin and reduces parasitic inductance of long traces. Also, the noise reduction capacitor (C13) is placed as close as possible to the IC.

The input of the LDO is connected to the output of the switcher using a shorting jumper and a long trace parallel with the trace that connects the ground on the LDO with the ground of the switcher. Critical analog ground of the LDO circuits such as the voltage set point divider, the LDO input, and output capacitors are terminated to ground using a wide ground trace separate from the power ground pour. In addition, the input and the output LDO capacitors are kept close to the IC. The voltage divider network of the LDO ties to the LDO output voltage at the copper of the LDO output trace.

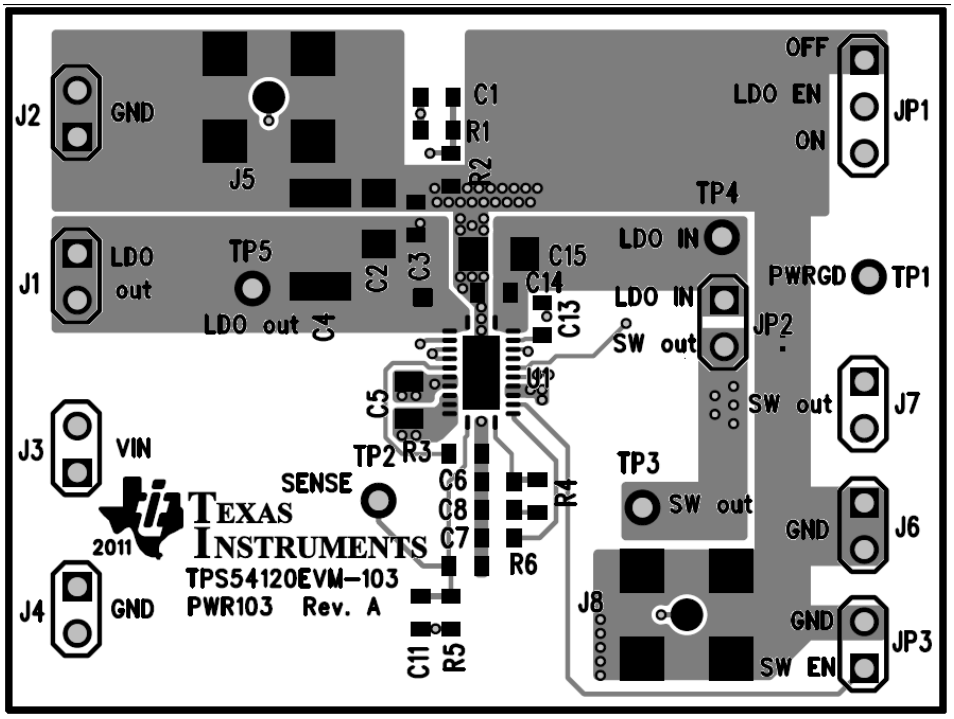

Figure 5-1. Top Side Silkscreen and Routing

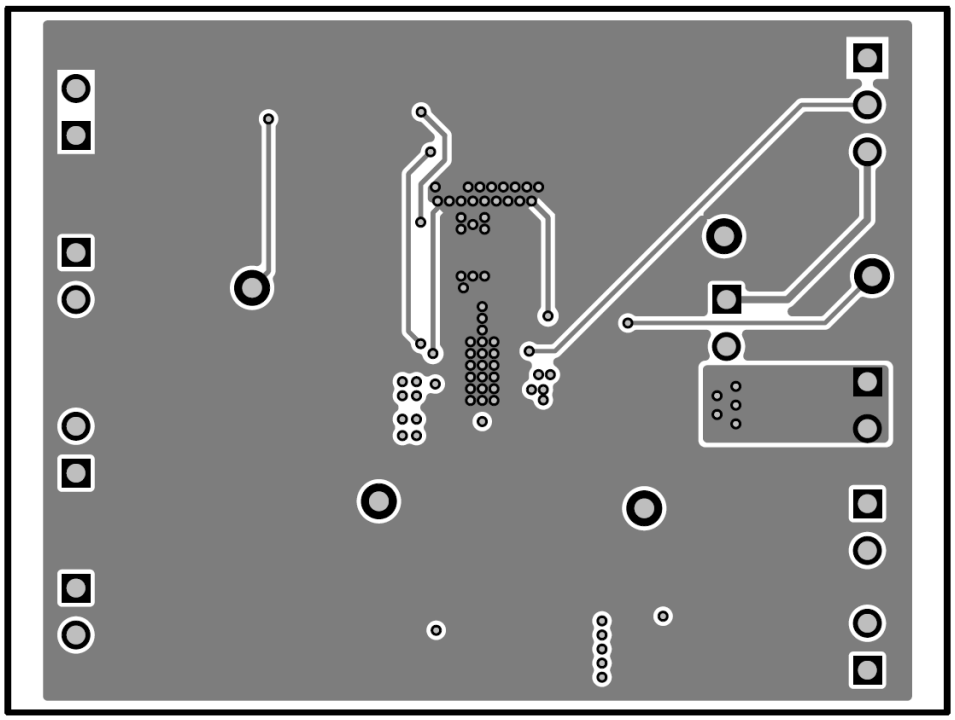

Figure 5-2. Second Layer (Internal) Routing

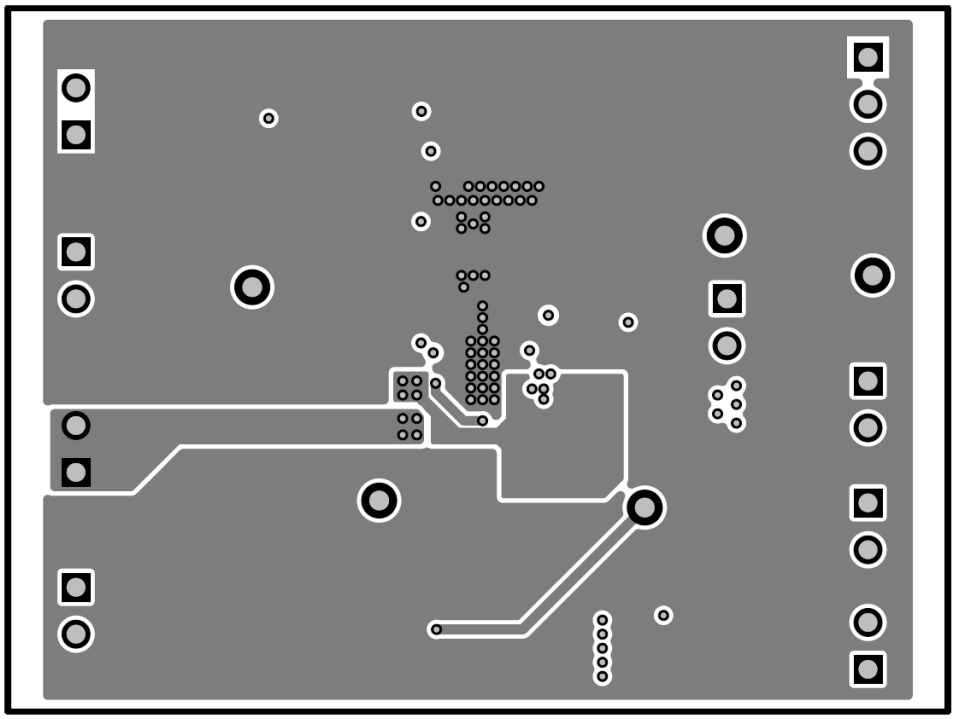

Figure 5-3. Third Layer (Internal) Routing

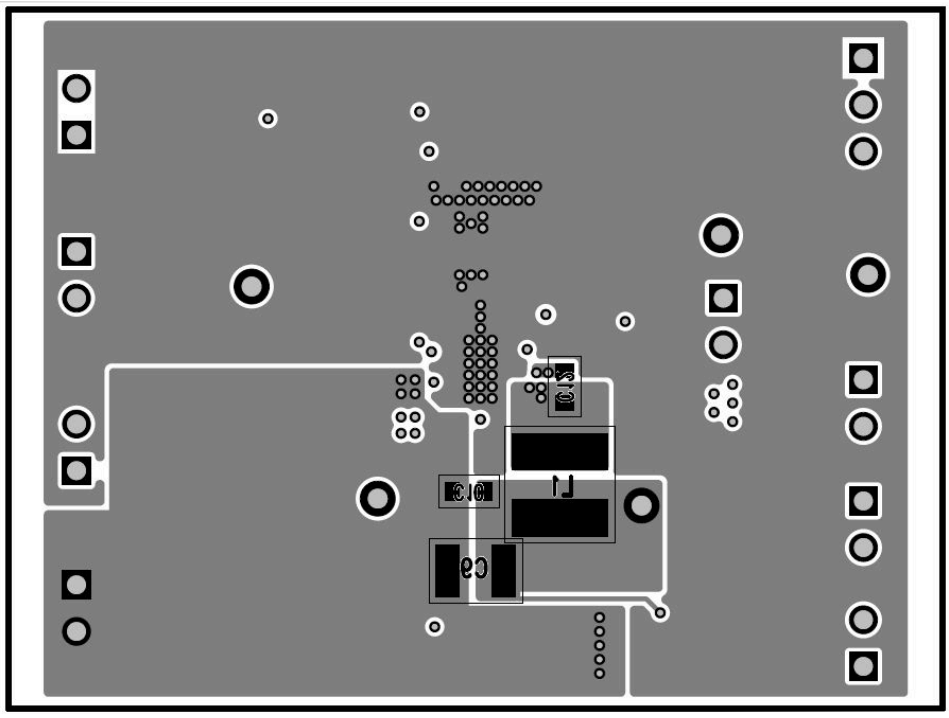

Figure 5-4. Bottom Layer Silkscreen and Routing

6 Schematic

Figure 6-1 is the schematic for the TPS54120 evaluation board.

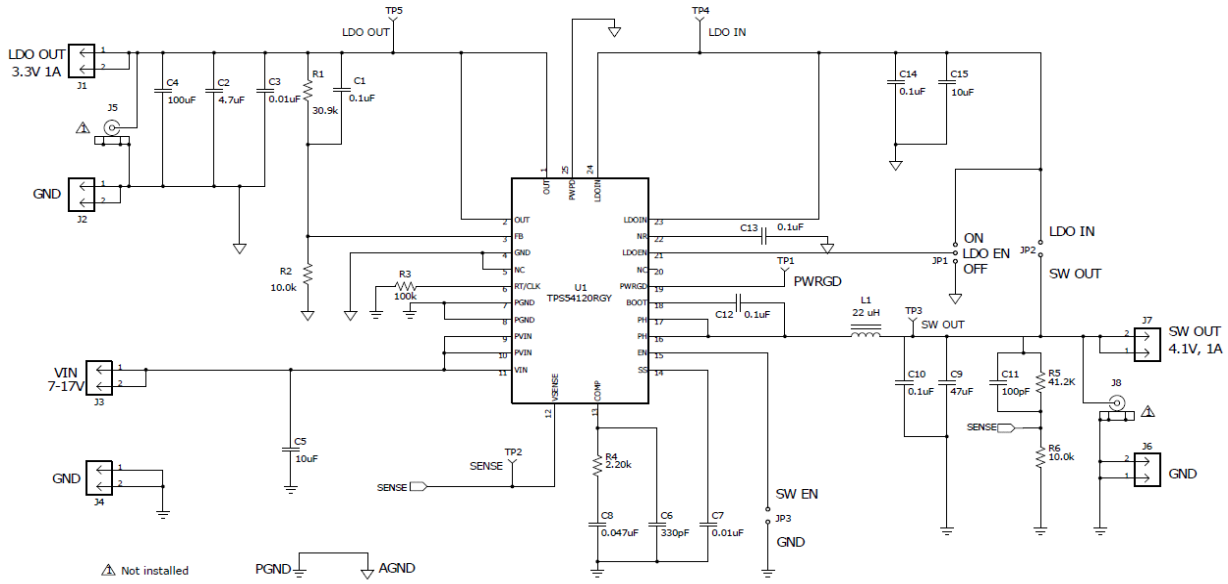

Figure 6-1. Schematic

7 Bill of Materials

Table 7-1 presents the bill of materials for the TPS54120 evaluation board.

Table 7-1. Bill of Materials

COUNT	REFDES	VALUE	DESCRIPTION	SIZE	PART NUMBER	MFR
5	C1, C10, C12–C14	0.1 µF	Capacitor, Ceramic, 16 V, X7R, 10%	0603	STD	STD
1	C11	100 pF	Capacitor, Ceramic, 50 V, C0G, 5%	0603	STD	STD
1	C15	10 µF	Capacitor, Ceramic, 6.3 V, X7R, 10%	1206	STD	STD
1	C2	4.7 µF	Capacitor, Ceramic, 10 V, X7R, 10%	1206	STD	STD
2	C3, C7	0.01 µF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	STD	STD
1	C4	100 µF	Capacitor, Ceramic, 6.3 V, 20%, X5R	1812	STD	STD
1	C5	10 µF	Capacitor, Ceramic, 25 V, X5R, 10%	0805	STD	STD
1	C6	330 pF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	STD	STD
1	C8	0.047 µF	Capacitor, Ceramic, 25 V, X7R, 10%	0603	STD	STD
1	C9	47 µF	Capacitor, Ceramic, 6.3 V, X5R, 20%	1210	STD	STD
6	J1-4, J6-7	PEC02SAAN	Header, Male 2-pin, 100-mil spacing	0.100 inch × 2	PEC02SAAN	Sullins
0	J5, J8	Open	Connector, SMT Straight, Jack Receptacle	0.250 SQ	142-0711-201	Johnson
1	JP1	PEC03SAAN	Header, Male 3-pin, 100-mil spacing	0.100 inch × 3	PEC03SAAN	Sullins
2	JP2–3	PEC02SAAN	Header, Male 2-pin, 100-mil spacing	0.100 inch × 2	PEC02SAAN	Sullins
1	L1	22 µH	Inductor, SMT, Power Choke 1.1 A, ±20%	4838	74408943220	WE
1	R1	30.9 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
2	R2, R6	10.0 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	100 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	2.20 k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	41.2 K	Resistor, Chip, 1/16W, 1%	0603	Std	Std
5	TP1-5	5002	Test Point, White, Thru Hole Color Keyed	0.100 × 0.100 inch		Keystone
1	U1	TPS54120RGY	IC, Integrated SWITCHER and LDO Low Noise 1-A Power Supply	QFN-24	TPS54120RGY	TI
3	—		Shunt, 100-mil, Black	0.100	929950-00	3M
1			PCB, 2.0" × 1.5" × 0.031"		PWR103	Any

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2012) to Revision A (November 2021) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 2
- Updated the user's guide title 2
- Edited user's guide for clarity..... 2

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