TPS718xxEVM-213 and TPS719xxEVM-213

This user's guide describes the characteristics, operation, and use of the Texas Instruments TPS718xxEVM-213 and TPS719xxEVM-213 evaluation module (EVM). Each TPS718xx and TPS719xx low quiescent current, wide bandwidth, dual low-dropout linear regulator is capable of supplying up to 200 mA of current per output. This user's guide includes setup instructions, a schematic diagram, a bill of materials (BOM), and PCB layout drawings for the evaluation module.

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1 Introduction

Texas Instruments' TPS718xxEVM-213 and TPS719xxEVM-213 evaluation module (EVM) helps designers evaluate the operation and performance of the TPS718xx and TPS719xx family of linear regulators. These are low quiescent current, wide bandwidth, low-dropout linear regulators in a SC70 package.

This EVM demonstrates the TPS71933-28, which provides up to 200 mA from each of its 3.3-V and 2.8-V regulated output pins. Other fixed-output voltage versions of the TPS718xx and TPS719xx families can be evaluated by replacing the TPS71933-28 on the EVM as these parts have the same pinout. See the TPS718xx and TPS719xx data sheet (SBVS088) for the various fixed-output voltage options available.

2 I/O Connectors, Setup, and Operation

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS718xxEVM-213 and TPS719xxEVM-213.

2.1 Input/Output Connector Descriptions

2.1.1 J1 –VIN

This header is the positive input connection to the linear regulator. The leads to the input supply should be twisted and kept as short as possible to minimize inductive droop during a load transient.

2.1.2 J2 – GND

This header is the input return connection for the input power supply.

2.1.3 J3 – VOUT

This header provides the output of each linear regulator on the ends, with the ground return on the two middle pins. Connect the appropriate load for each output to this header.

2.1.4 JP1– EN1

This jumper enables or disables output 1 of the dual linear regulator. Connect the shorting jumper from the center EN pin to either the ON or OFF position. This pin should never be left floating.

2.1.5 JP2– EN2

This jumper enables or disables output 2 of the dual linear regulator. Connect the shorting jumper from the center EN pin to either the ON or OFF position. This pin should never be left floating.

2.1.6 TP1

This test point connects to the input of the dual linear regulator.

2.1.7 TP2

This test point connects to output 1 of the dual linear regulator.

2.1.8 TP3

This test point connects to output 2 of the dual linear regulator.

2.2 Setup

The TPS718xx and TPS719xx ICs use the 2-mm X 2-mm SON package. The thermal performance of this package style and ambient temperature may limit the power dissipation, computed as Pd = $(V_{IN} - V_{O1}) \times I_{O1} + (V_{IN} - V_{O2}) \times I_{O2}$, and therefore maximum output current of each rail. Because the EVM's regulator output voltages and board layout are fixed, the regulator's input voltage, output current, and ambient temperature are the only variables that can be adjusted to manage power dissipation.

Table 1 shows the maximum input voltage at room temperature and full-rated load current of 200 mA. Above this voltage, the output current must be reduced to keep the power dissipation of the package below the maximums stated in the data sheet. Changes in output voltage or ambient temperature affect these values. Table 1 also shows the minimum input voltage required to produce an output for the linear regulator. The minimum input voltage is the output voltage plus the necessary dropout voltage at 200-mA output current.

Table 1. Minimum and Maximum Input Voltage

Output #	Output Voltage	Minimum Input Voltage	Maximum Input Voltage Before Current Derate (T = 25°C, Io = 200 mA)
1	3.3	3.7	6.5
2	2.8		6.5

2.3 Operation

JP1 is the enable for the OUT1 regulator and must be tied high to ON or low for OFF for proper operation. Use a shorting block to set JP1 to the desired configuration. JP2 is the enable for the OUT2 regulator and must be tied high to ON or low for OFF for proper operation. Use a shorting block to set JP2 to the desired configuration.

3 Board Layout

This section provides the HPA213 board layout and illustrations.

3.1 Layout

Figure 1, Figure 2, and Figure 3 show the board layout for the HPA213 printed-circuit board.

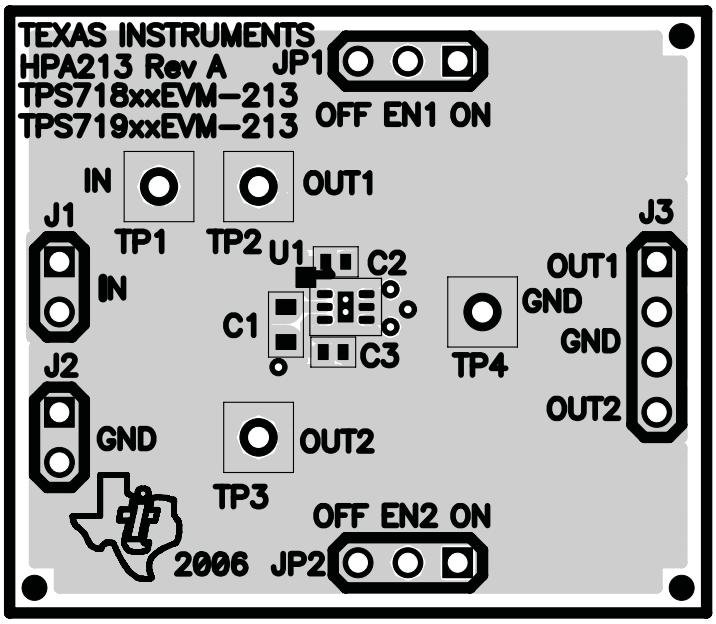

Figure 1. Assembly Layer

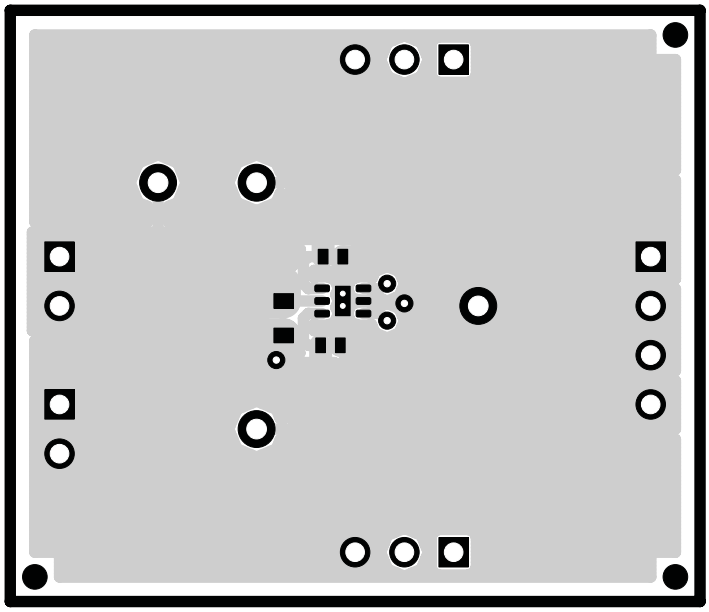

Figure 2. Top Layer Routing

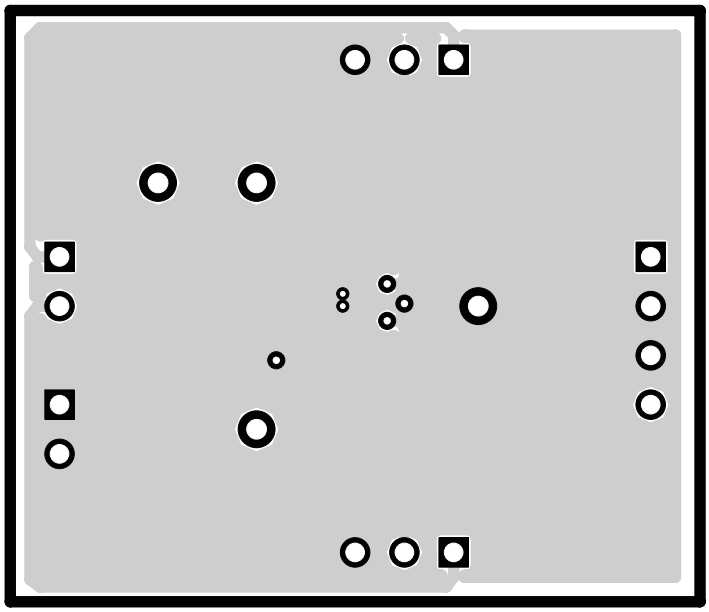

Figure 3. Bottom Layer Routing

4 Schematic and Bill of Materials

This section provides the HPA213 schematic and bill of materials.

4.1 Schematic

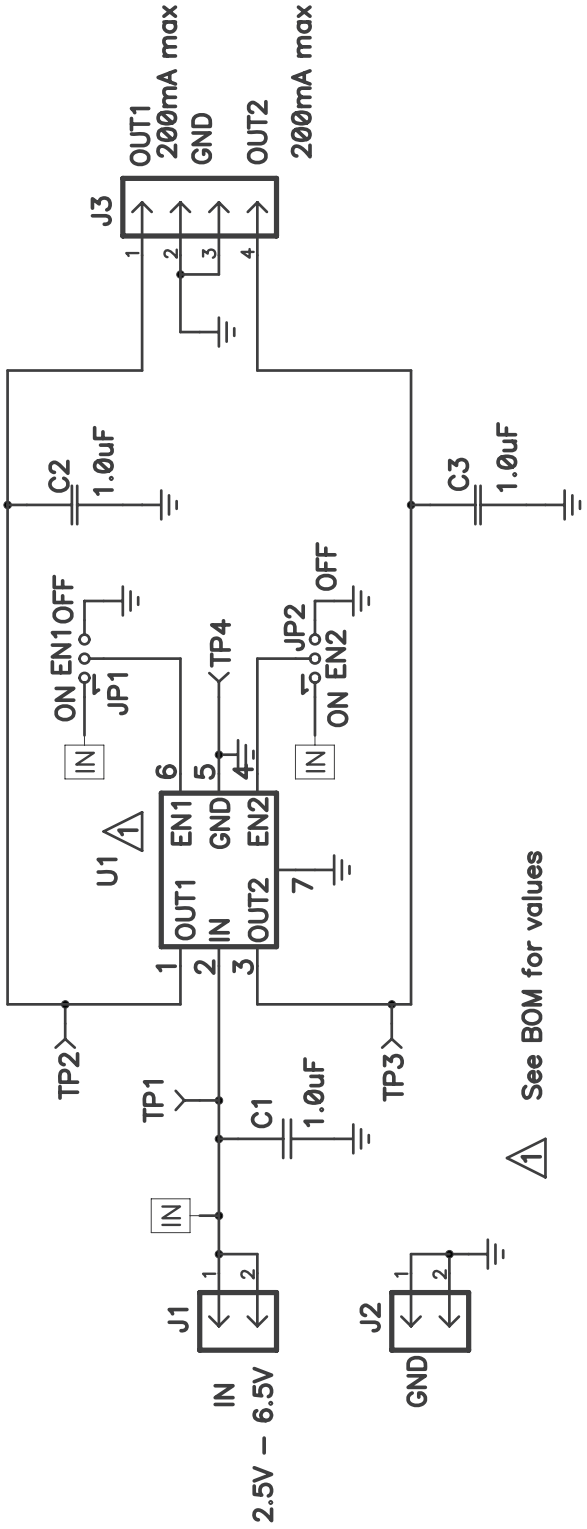

Figure 4. TPS718xxEVM-213 and TPS719xxEVM-213 Schematic

4.2 Bill of Materials

Table 2. HPA213 Bill of Materials

Count	Ref Des	Value	Description	Size	Part Number	MFR
1	C1	1.0 µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C105K	TDK
2	C2, C3	1.0 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0402	GRM155R60J105KE19D	Murata
2	J1, J2		Header, 2-pin, 100 mil spacing, (36-pin strip)	0.100 × 2	PTC36SAAN	Sullins
1	J3		Header, 4-pin, 100 mil spacing, (36-pin strip)	0.100 × 4	PTC36SAAN	Sullins
2	JP1, JP2		Header, 3-pin, 100 mil spacing, (36-pin strip)	0.100 × 3	PTC36SAAN	Sullins
3	TP1– TP3		Test Point, Red, Thru Hole Color Keyed	0.100 × 0.100	5000	Keystone
1	TP4		Test Point, Black, Thru Hole Color Keyed	0.100 × 0.100	5001	Keystone
1	U1		IC, Dual 200 mA, Low Noise, High PSRR, LDO Linear Regulators	SON-6	TPS71933-28DRV	TI
1	—		PCB, 1.4 In × 1.2 In × 0.062 In		HPA213	Any
2	—		Shunt, 100-mil, Black	0.1	929950-00	3M

5 Related Documentation From Texas Instruments

TPS718xx, TPS719xx, Dual, 200mA Output, Low Noise, High PSRR Low-Dropout Linear Regulators in 2mm x 2mm SON Package data sheet (SBVS088)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 6 V and the output voltage range of 1.2 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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