Texas Instruments

TPS65140EVM-031

User's Guide

February 2004

PMP Portable Power

SLVU104

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.7 V to 5.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the TPS65140EVM-031 evaluation module (EVM). This EVM contains Texas Instruments TPS65140 triple output LCD supply IC with linear regulator controller and VCOM buffer. This users guide includes EVM specifications, test results, schematic diagram, bill of materials (BOM), and recommended test setup.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1 – Introduction
- ❏ Chapter 2 – EVM Operation
- ❏ Chapter 3 – Board Layout
- ❏ Chapter 4 – Bill of Materials and Schematic

Related Documentation From Texas Instruments

SLVS497 − TPS65140 data sheet

If you need Assistance

Contact your local TI sales representative.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademark

Powermite is a registered trademark of Microsemi Corporation.

Contents

Figures

Tables

Chapter 1

Introduction

This chapter contains background information for the TPS65140EVM-031 evaluation module.

Topic **Page**

1.1 Background

The TPS65140EVM uses a TPS65140 multichannel output IC to provide three LCD power rails, as well as a linear regulator controller to provide 3.3 V and a VCOM buffer. The goal of the EVM is to facilitate evaluation of the TPS65140.

1.2 Performance Specification Summary

Table 1−1 provides a summary of the TPS65140EVM−031 performance specifications. All specifications are given for an ambient temperature of 25°C.

Table 1−1. Typical Performance Specification Summary for VIN = 3.3 V and VOUT1 = 10 V, T_A = 25°C

Specification	Voltage Range (V)			Current Range (mA)		
	Min	Typ	Max	Min	Typ	Max
VIN	2.7	3.3	4.0	3000		
VOUT1	9.85	10	10.15	0		300
VOUT2	−5.10	−5	−4.90	0	20	(1)
VOUT3	22.5	23	23.5	0	20	(1)
VOUT4		N/A(2)			N/A	
VCOM	4.92	5	5.07	0	650 peak	(1)

1) Maximum currents are determined by ambient conditions.
2) The linear regulator requires VIN ≥ 3.7 V for normal operation and should be disabled using JP3.

1.3 Modifications

The primary goal of this EVM is to facilitate user evaluation of the TPS65140. To facilitate user customization of the EVM, the board was designed with devices having 603 or larger footprints. So, a real implementation would likely occupy less total board space.

Changing components can improve or degrade EVM performance. For example, using an inductor with larger dc resistance for the main boost converter will lower efficiency of the solution. In addition, using a BJT with lower Beta or in a smaller package will limit the total output current that the linear regulator can provide.

The main boost converter requires external compensation components (R7, C11) for stability. This EVM has been optimized for an input voltage of 3.3 V. If a different input voltage and/or a different output voltage is to be applied, the main boost converter needs to be re-compensated in order to be stable over the entire load and temperature range (see Table 1−2 and Table 4−2).

Table 1−2. Typical Performance Specification Summary for VIN = 5 V and VOUT1 = 13.5V, T_A = 25°C

Specification	Voltage Range (V)			Current Range (mA)		
	Min	Typ	Max	Min	Typ	Max
VIN	4.0	5	5.8	2000		
VOUT1	13.30	13.5	13.70	0		400
VOUT2	−7.11	−7	−6.86	0	20	(1)
VOUT3	22.5	23	23.5	0	20	(1)
VOUT4	3.2	3.3	3.4	0	500	(1)
VCOM	6.65	6.75	6.85	0	650 peak	(1)

1) Maximum currents are determined by ambient conditions.

(This page has been left blank intentionally.)

Chapter 2

EVM Operation

This chapter describes how to properly test the TPS65140 using the TPS65140EVM−031.

Topic **Page**

2.1 Input/Output Connect

The EVM connection points are described in the following paragraphs.

2.1.1 J1−VIN

This is the positive connection to the input power supply. The leads to the input supply should be twisted and kept as short as possible.

2.1.2 J2−GND

This is the return connection to the input power supply.

2.1.3 J3−VOUT1

This is the positive output for the main boost convertr of the device.

2.1.4 J4−GND

This is the return connection for the load on the main boost converter of the device.

2.1.5 J5−VPGM

This is the power-good output pin.

2.1.6 J6−GND

This is the return connection for the load on the power-good pin.

2.1.7 J7−VOUT4

This is the output for the 3.3-V linear regulator.

2.1.8 J8−GND

This is the return connection for the load on the linear regulator.

2.1.9 J9−VOUT2

This is the negative output for the inverting charge pump.

2.1.10 J10−GND

This the return connection for the load on the inverting charge pump.

2.1.11 J11−VOUT3

This is the positive output for the positive charge pump.

2.1.12 J12−GND

This the return connection for the load on the positive charge pump.

2.1.13 JP1 − Mode

This is the charge pump mode pin connector. In order for the charge pump to operate as a voltage doubler, a jumper is installed to pull the mode pin to GND and C16 is left unpopulated. In order for the charge pump to operate as a voltage tripler, the jumper is removed and C16 is populated.

2.1.14 JP2−Enable (EN)

This is the enable pin for the main boost converter (VOUT1). The enable pin is pulled up to Vin by an onboard pullup resistor. Placing a jumper across pins 2−3 of JP2 shorts the enable pin to GND; thereby disabling the device. Placing a jumper across pins 1−2 of JP2 connects the enable pin to Vin and enables the device.

2.1.15 JP3−Enable Regulator (ENR)

This is the enable pin the linear regulator (VOUT4). The enable pin is pulled up to Vin by an onboard pullup resistor. Placing a jumper across pins 2−3 of JP3 shorts the enable pin to GND; thereby disabling the device. Placing a jumper across pins 1−2 of JP3 connects the enable pin to Vin and enables the device.

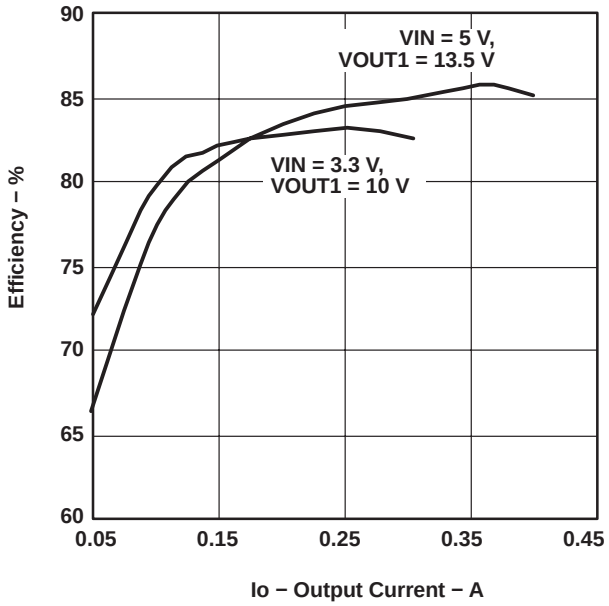
2.2 Test Setup

The absolute maximum input voltage is 6 V. The TPS65140 is designed to operate with a maximum input voltage of 5.8 V. Connect a power supply with 3.3 V output voltage and current limit set to at least 3 A. Short pins 1−2 on jumpers JP2 and JP3 to enable both the main boost converter and linear regulator. Connect a load not to exceed the maximum loads per Table 1−2 to each output of the EVM.

2.3 Test Results

Below are the efficiency results using this EVM:

Figure 2−1. TPS65140 VOUT1 Efficiency Using the CDRH5D28−4R2 Inductor



Note: Choosing a different inductor could change the effieciency by ± 5%.

Figure 2−2. TPS65140 Main Boost Converter Load Transient for VIN = 3.3V and VOUT = 10V

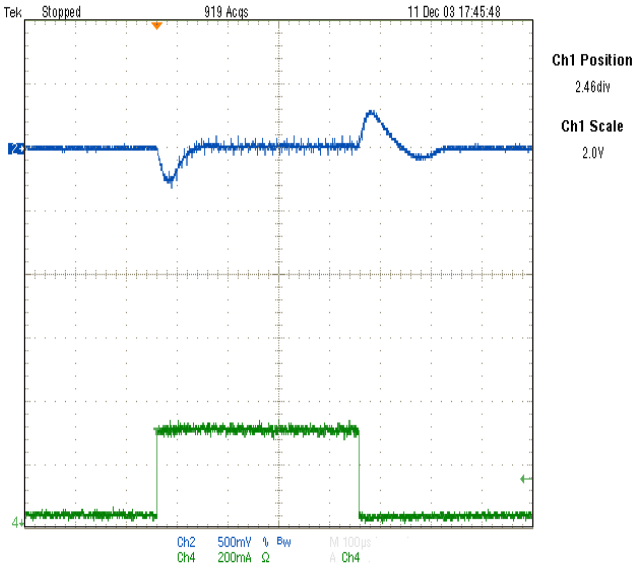
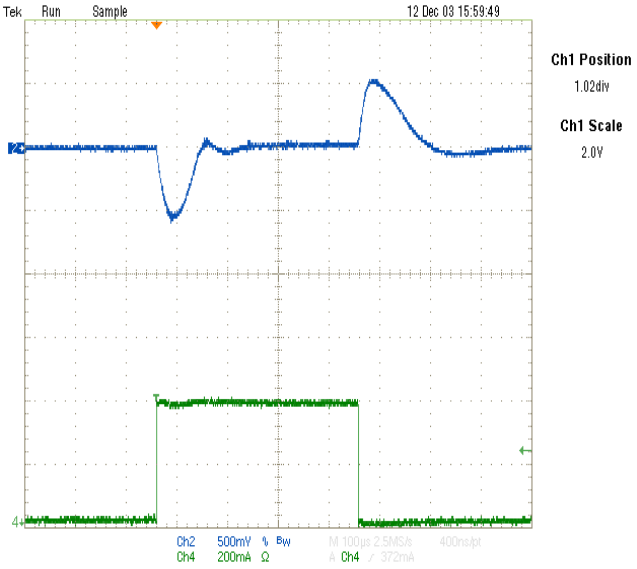


Figure 2−3. TPS65140 Main Boost Converter Load Transient for VIN = 5 V and VOUT = 13.5V



Chapter 3

Board Layout

This chapter provides the TPS65140EVM−031 board layout and illustrations.

Topic **Page**

3.1 Layout

Board layout is critical for all switch mode power supplies. Figures 3−1, 3−2, and 3−3 show the board layout for the HPA030 PWB. The switching nodes with high frequency noise are isolated from the noise sensitive feedback circuitry and careful attention has been given to the routing of high frequency current loops. Refer to the data sheet for more specific layout guidelines.

Figure 3−1. Top Assembly Layer

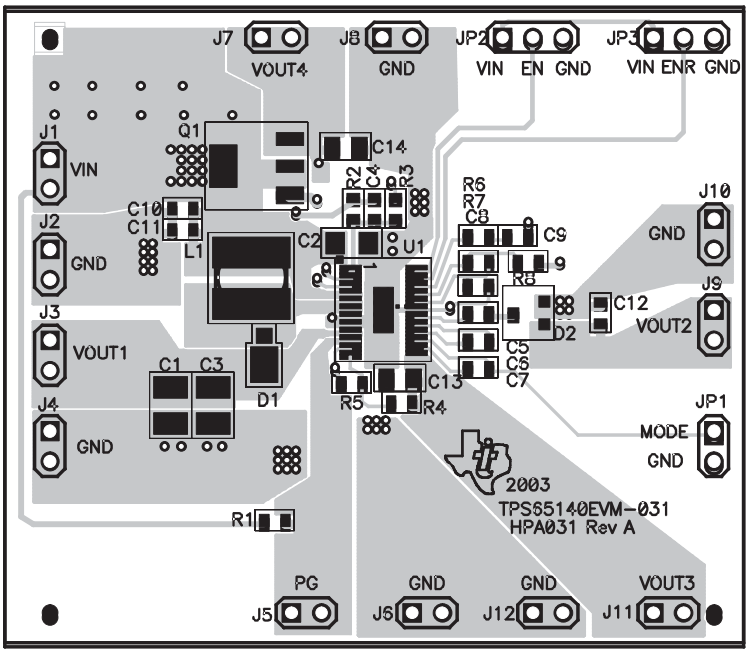


Figure 3−2. Top Layer Routing

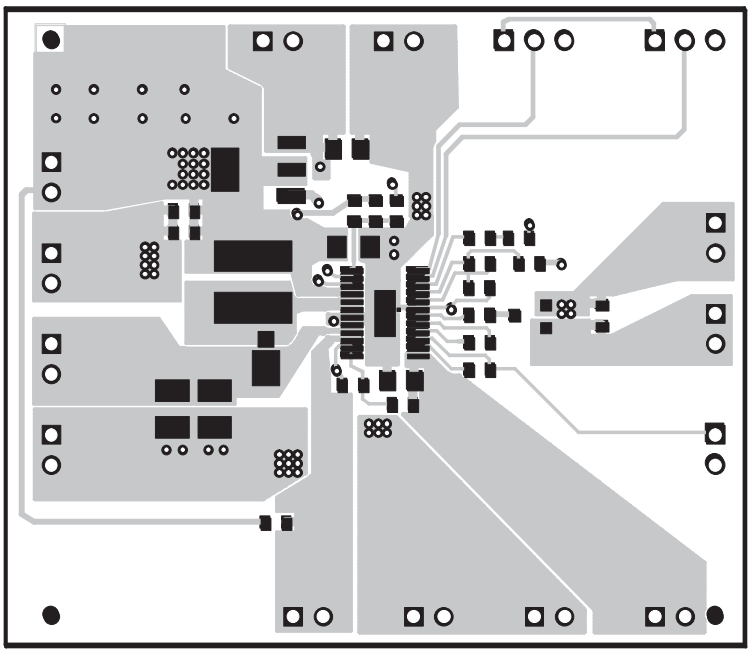
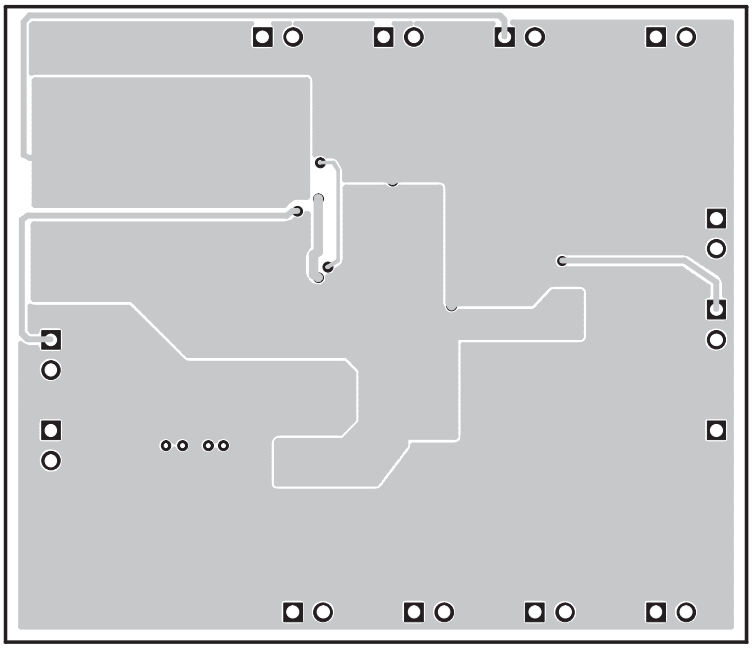


Figure 3−3. Bottom Layer Routing



(This page has been left blank intentionally.)

Chapter 4

Bill of Materials and Schematic

This chapter provides the TPS65140EVM-031 bill of materials and schematic.

Topic **Page**

Table 4−1. Bill of Materials for VIN = 3.3 V and VOUT1 = 10 V

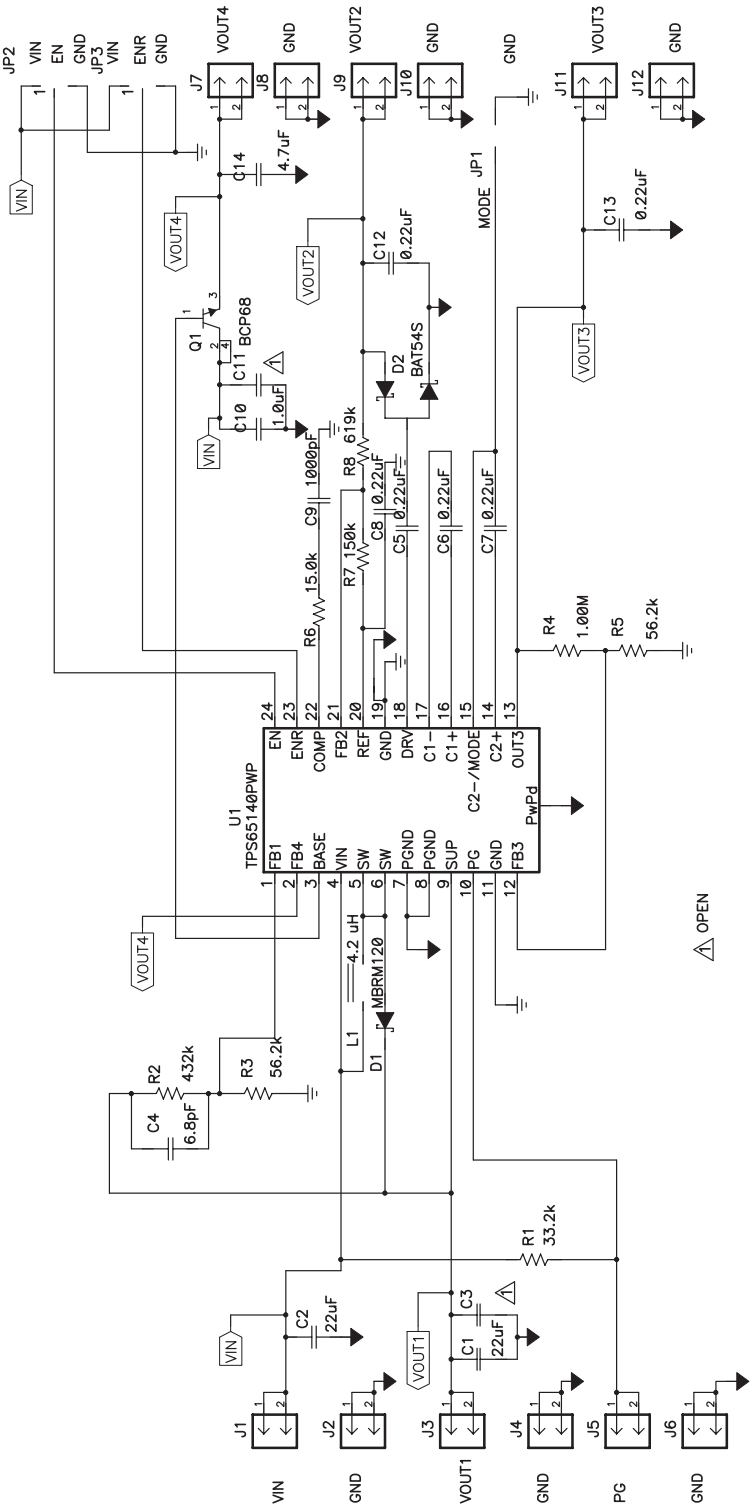
Count	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 22−μF, 16−V, X5R, 10%	1210	TDK	C3225X5R1C226KT
1	C10	Capacitor, ceramic, 1.0−μF, 10−V, X5R, 10%	603	TDK	C1608X5R1A105KT
0	C11	Capacitor, ceramic, xxx−μF, vv−V	603		
1	C13	Capacitor, ceramic, 0.22−μF, 50−V, X5R, 20%	805	TDK	C2012X5R1H224KT
1	C14	Capacitor, ceramic, 4.7−μF, 6.3−V, X5R, 10%	805	TDK	C2012X5R0J475KT
1	C2	Capacitor, ceramic, 22−μF, 6.3−V, X7R, 10%	1206	TDK	C3216X5R0J226KT
0	C3	Capacitor, ceramic, xx−μF, vv−V	1210		
1	C4	Capacitor, ceramic, 6.8−pF, 50−V, C0G, 5%	603	AVX	06035A6R8CAT2A
5	C5−C8, C12	Capacitor, ceramic, 0.22−μF, 25−V, X5R, 10%	603	TDK	C1608X5R1E224KT
1	C9	Capacitor, ceramic, 1000−pF, 50−V, X5R, 10%	603	TDK	C1608X7R1H102KT
1	D1	Diode, Schottky, 1A, 20V	457−04	On Semi	MBRM120
1	D2	Diode, Dual Schottky, 200−mA, 30−V	SOT23	Zetex	BAT54S
12	J1−J12	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2	Sullins	PTC36SAAN
1	JP1	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2	Sullins	PTC36SAAN
2	JP2, JP3	Header, 3−pin, 100 mil spacing, (36−pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	L1	Inductor, SM Toroid, 4.2−μH, 2.2−A, 31−mΩ	74480	Sumida	CDRH5D28−4R2
1	Q1	Transistor, NPN General Purpose Amplifier, VCE 20 V, VCB 30 V, VEB 5 V, IC 1A	SOT223	Fairchild	BCP68
1	R1	Resistor, Chip, 33.2 kΩ, 1/16−W, 1%	603	Std	Std
1	R2	Resistor, Chip, 432 kΩ, 1/16−W, 1%	603	Std	Std
2	R3, R5	Resistor, Chip, 56.2 kΩ, 1/16−W, 1%	603	Std	Std
1	R4	Resistor, Chip, 1.00 MΩ, 1/16−W, 1%	603	Std	Std
1	R6	Resistor, Chip, 15.0 kΩ, 1/16−W, 1%	603	Std	Std
1	R7	Resistor, Chip, 150 kΩ, 1/16−W, 1%	603	Std	Std
1	R8	Resistor, Chip, 619 kΩ, 1/16−W, 1%	603	Std	Std
1	U1	IC, (TFT) LCD supply	PWP24	TI	TPS65140PWP
1	−−	PCB, 2.45 In × 2.1 In × 0.062 In		Any	HPA031
3	−−	Shunt, 100−mil, black	0.100	3M	929950−00

Table 4−2. Bill of Materials for VIN = 5.0 V and VOUT1 = 13.5 V

Count	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 22−µF, 16−V, X5R, 10%	1210	TDK	C3225X5R1C226KT
1	C10	Capacitor, ceramic, 1.0−µF, 10−V, X5R, 10%	603	TDK	C1608X5R1A105KT
0	C11	Capacitor, ceramic, xxx−µF, vv−V	603		
1	C13	Capacitor, ceramic, 0.22−µF, 50−V, X5R, 20%	805	TDK	C2012X5R1H224KT
1	C14	Capacitor, ceramic, 4.7−µF, 6.3−V, X5R, 10%	805	TDK	C2012X5R0J475KT
1	C2	Capacitor, ceramic, 22−µF, 6.3−V, X7R, 10%	1206	TDK	C3216X5R0J226KT
0	C3	Capacitor, ceramic, xx−µF, vv−V	1210		
1	C4	Capacitor, ceramic, 3.3−pF, 50−V, C0G, 5%	603	AVX	06035A6R8CAT2A
5	C5−C8, C12	Capacitor, ceramic, 0.22−µF, 25−V, X5R, 10%	603	TDK	C1608X5R1E224KT
1	C9	Capacitor, ceramic, 2200−pF, 50−V, X5R, 10%	603	TDK	C1608X7R1H102KT
1	D1	Diode, Schottky, 1A, 20V	457−04	On Semi	MBRM120
1	D2	Diode, Dual Schottky, 200−mA, 30−V	SOT23	Zetex	BAT54S
12	J1−J12	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2	Sullins	PTC36SAAN
1	JP1	Header, 2−pin, 100 mil spacing, (36−pin strip)	0.100 x 2	Sullins	PTC36SAAN
2	JP2, JP3	Header, 3−pin, 100 mil spacing, (36−pin strip)	0.100 x 3	Sullins	PTC36SAAN
1	L1	Inductor, SM Toroid, 4.2−µH, 2.2−A, 31−mΩ	74480	Sumida	CDRH5D28−4R2
1	Q1	Transistor, NPN General Purpose Amplifier, VCE 20 V, VCB 30 V, VEB 5 V, IC 1A	SOT223	Fairchild	BCP68
1	R1	Resistor, Chip, 33.2 kΩ, 1/16−W, 1%	603	Std	Std
1	R2	Resistor, Chip, 825 kΩ, 1/16−W, 1%	603	Std	Std
2	R3, R5	Resistor, Chip, 80.6 kΩ, 1/16−W, 1%	603	Std	Std
1	R4	Resistor, Chip, 1.00 MΩ, 1/16−W, 1%	603	Std	Std
1	R6	Resistor, Chip, 4.32 kΩ, 1/16−W, 1%	603	Std	Std
1	R7	Resistor, Chip, 130 kΩ, 1/16−W, 1%	603	Std	Std
1	R8	Resistor, Chip, 750 kΩ, 1/16−W, 1%	603	Std	Std
1	U1	IC, (TFT) LCD supply	PWP24	TI	TPS65140PWP
1	−−	PCB, 2.45 In × 2.1 In × 0.062 In		Any	HPA031
3	−−	Shunt, 100−mil, black	0.100	3M	929950−00

4.1 Schematic

Figure 4−1. TPS65140EVM−031 Schematic for VIN = 3.3 V and VOUT1 = 10 V.



(This page has been left blank intentionally.)