TEXAS INSTRUMENTS

TPS70351EVM

Low-Dropout, Dual-Output Linear Regulator EVM For Using the TPS70351

User's Guide

October 2000

POWER MANAGEMENT PRODUCTS

SLVU036

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Preface

About This Manual

This user's guide describes the TPS70351EVM low-dropout, dual-output evaluation module (SLVP165). The SLVP165 provides a convenient method for evaluating the performance of a dual-output linear regulator.

How to Use This Manual

- ❑ Chapter 1 Introduction
- ❑ Chapter 2 EVM Adjustments and Test Points
- ❑ Chapter 3 Circuit Design
- ❑ Chapter 4 Test Results

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

- TPS70351 data sheets (literature number SLVS285)

Trademarks

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Chapter 1

Introduction

This user's guide describes the TPS70351EVM165 low-dropout, dual-output evaluation module (SLVP165B). LDOs provide ideal power supplies for rapidly transitioning DSP loads. The TPS703xx family of devices is designed to provide a complete power management solution for DSP, processor power, ASIC, FPGA, and digital applications where dual output voltage regulators are required. Easy programmability of the sequencing function makes this family ideal for any DSP applications with a power sequencing requirement. Differentiated features, such as SVS supervisory circuit, manual reset inputs, and enable function, provide a complete system solution. Moreover, with its low-quiescent current, low-dropout voltage, low-output noise, high PSRR, fast-transient response, and high accuracy compared to standard LDOs, the TPS703xx provides an ideal solution where standard linear regulators are too inefficient or too slow and where a switch converter solution or the source power supply is too noisy.

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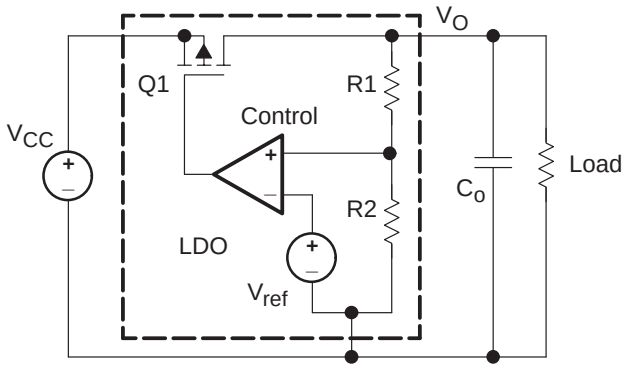
1.1 Low Dropout Voltage Linear Regulator Circuit Operation

In TI's low dropout voltage linear regulator topology, a PMOS transistor is used for the pass element. Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading.

The basic LDO regulator circuit includes the LDO and an output capacitor for stabilization. Figure 1–1 shows the circuit of a typical LDO application.

Figure 1–1. Typical LDO Application



In the LDO application shown in Figure 1–1, the LDO regulates the output voltage V_O.

If V_O falls below the regulation level, the controller increases the V_{SG} differential and the PMOS transistor conducts more current, resulting in an increase in V_O. If V_O exceeds the regulation level, the controller decreases the V_{SG} differential and the PMOS transistor conducts less current, resulting in a decrease in V_O. The PMOS pass element acts like an adjustable resistor. The more negative the gate becomes versus the source, the less the source-drain resistance becomes, resulting in higher current flow through the PMOS.

1.2 Design Strategy

The TI SLVP165B EVM provides a convenient method for evaluating the performance of TPS703xx dual-output linear regulators. The EVM provides proven, demonstrated reference designs and test modes to aid in evaluation. The board contains a power supply along with an onboard transient generator. The transient slew rate can be modified by changing two resistors. Jumpers allow settings of minimum/maximum load as well as device-enabling and power sequencing. There is enough room on the EVM to evaluate different types of output capacitors including ESR behaviors. Many test points allow the measuring of input, output, and dropout voltage.

The EVM contains a TPS70351. Regulator 1 provides an output voltage of 3.3 V and a maximum output current of 1 A. Regulator 2 provides an output voltage of 1.8 V and a maximum output current of 2 A.

Table 1–1 summarizes the TPS703xx family's features. See the TPS703xx datasheet, TI literature number SLVS285, for a further explanation of features.

Table 1–1. Summary of the TPS703xx LDO Family Features

Description	TPS703xx Feature
Maximum input voltage [V]	6
Maximum output current [A]	1/2
Typical quiescent current [μA]	185
Typical dropout voltage [mV]	160
Typical output noise [μVrms] (30 Hz ≤ f ≤ 50 kHz, C_O = 33 μF)	79/77
Accuracy over line, load, and temperature	2%
PSRR (at 1 kHz, C_O = 10 μF, T_J = 25°C)	65/60 dB
Package	24 pin TSSOP with PowerPAD™
Minimum output capacitor	> 47 μF (ceramic)
Available voltage option [V]	3.3/1.5, 3.3/1.2, 3.3/1.8, 3.3/2.5, and adj/adj
Performance advantage	Dual output LDO, power-up sequencing, DSP application, PG and RESET

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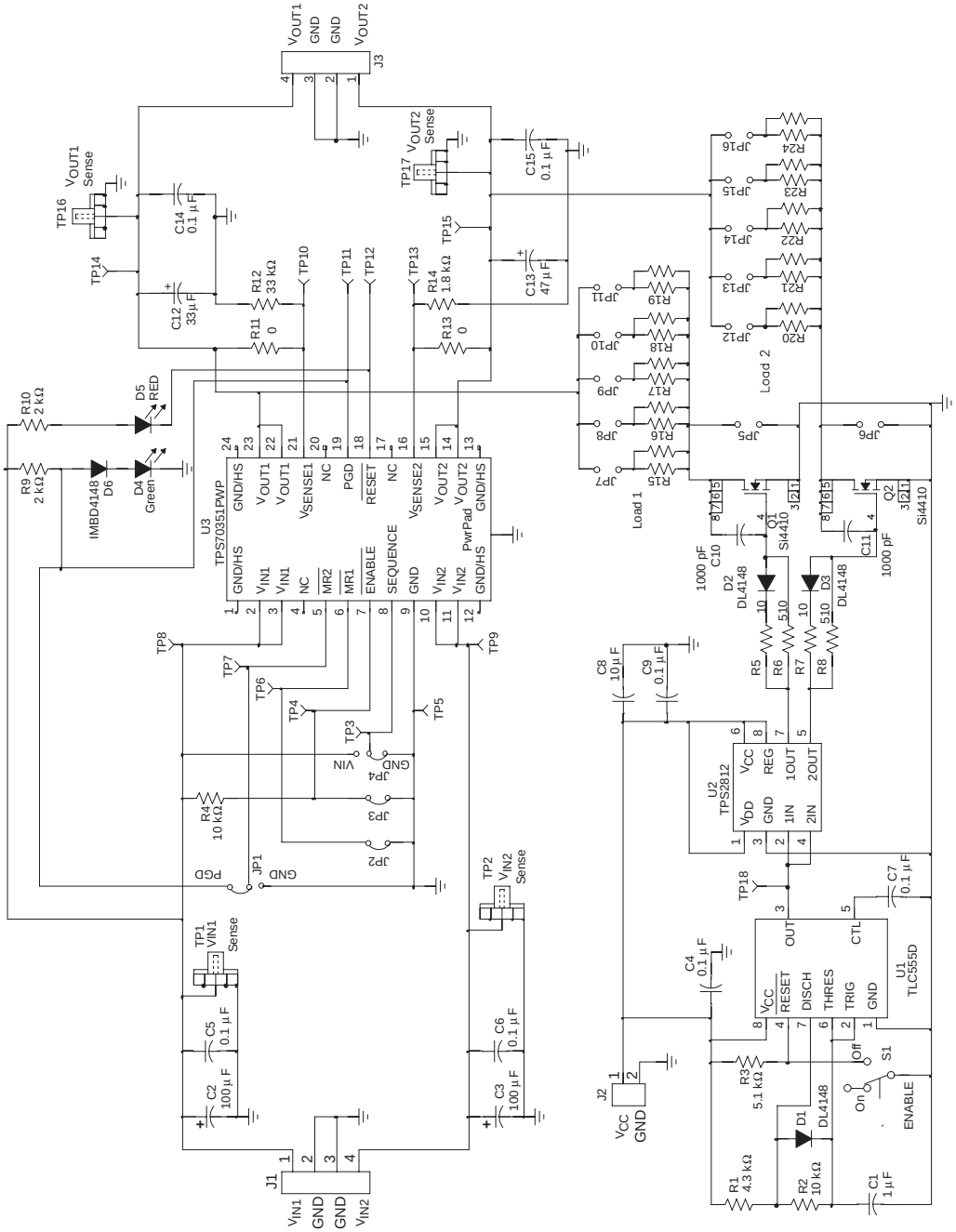
1.3 Schematic

Figure1–2 shows the SLVP165 EVM schematic diagram.

Figure 1–2. SLVP165B EVM Universal LDO Tester Schematic Diagram



1.4 Bill of Materials

Table 1–2 lists materials required for the SLVP165 EVM.

Table 1–2. SLVP165B EVM Bill of Materials

Ref Des	Qty	Part Number	Description	MFG	Size
C1	1	ECJ-2VF1C105Z	Capacitor, ceramic, 1.0 uF, 16 V, 80% – 20%, Y5V	Panasonic	805
C2 – 3	2	TPSD107M010R100	Capacitor, tantalum, 100 μF, 10 V, 100-mΩ, 20%	AVX	D Size
C4 – 7, 9, 14, 15	7	GRM39X7R104K016A	Capacitor, ceramic, 0.1 uF, 16 V, 10%, X7R	Murata	603
C8	1	GRM235Y5V106Z016A	Capacitor, ceramic, 10 μF, 16 V, 80%–20%, Y5 V	TDK	1210
C10, 11	2	GRM39X7R102K050A	Capacitor, ceramic, 1000 pF, 50 V, 10%, X7R	Murata	603
C12	1	10TPA33M	Capacitor, POSCAP, 33 μF, 10 V, 20%	Sanyo	C Size
C13	1	6TPA47M	Capacitor, POSCAP, 47 μF, 10 V, 20%	Sanyo	C Size
D1 – 3	3	1N4148	Diode, signal, 75 V, 300 mA	Diodes, Inc.	SOT–23
D4	1	SML-LX2832GC-TR	Diode. LED, green, 2.1 V, 25 mcd, SM	Lumex	1210
D5	1	SML-LX2832RC-TR	Diode. LED, red, 1.7 V, 40 mcd, SM	Lumex	1210
D6	1	IMBD4148	Diode, switching, 10 mA, 100 V, 350 mW	Vishay-Liteon	SOT–23
J1, 3	2	ED1516	Terminal block, 4-pin, 6-A, 3.5 mm	OST	
J2	1	ED1514	Terminal block, 2-pin, 6A, 3.5 mm	OST	
JP1, 4	2	PTC36SAAN	Header, 3-pin, 100 mil spacing (36 pin strip)	Sullins	
JP2, 3, 5 – 16	14	PTC36SAAN	Header, 2-pin, 100 mil spacing (36 pin strip)	Sullins	
Q1, 2	2	Si4410DY	MOSFET, N-ch, 30 V, 10 A, 13 mΩ	Siliconix	SO8
R1	1	Std	Resistor, chip, 4.3 kΩ, 1/16W, 5%		603
R2, 4	2	Std	Resistor, chip, 10 kΩ, 1/16W, 5%		603
R3	1	Std	Resistor, chip, 5.1 kΩ, 1/16W, 5%		603
R5, 7	2	Std	Resistor, chip, 10 Ω, 1/16W, 5%		603
R6, 8	2	Std	Resistor, chip, 510 Ω, 1/16W, 5%		603
R9, 10	2	Std	Resistor, chip, 2.0 kΩ, 1/16W, 5%		603
R11, 13	2	Std	Resistor, chip, 0 Ω, 1/16W, 5%		603
R12	1	Std	Resistor, chip, 3.3 kΩ, 1/16W, 5%		603
R14	1	Std	Resistor, chip, 1.8 kΩ, 1/16W, 5%		603

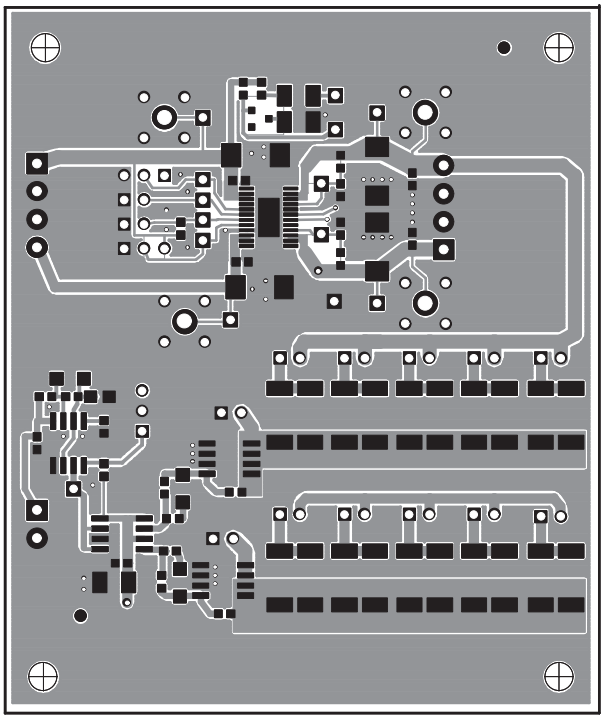
Table 1–2. SLVP165B EVM Bill of Materials (Continued)

Ref Des	Qty	Part Number	Description	MFG	Size
R15 – 19 R15A – 19A	10	ERJ–1WYJ33OU	Resistor, chip, 33 Ω, 1 W, 5%	Panasonic	2512
R20 – 24 R20A – 24A	10	ERJ–1WY100U	Resistor, chip, 10 Ω, 1 W, 5%	Panasonic	2512
S1	1	EG1218	Switch, 1P2T, slide, PC-mount, 200 mA	E–Switch	
TP1, 2, 16, 17	4	131–4244–00	Adaptor, 3.5-mm probe clip (or 131–5031–00)	Tektronix	
TP3 – 15, 18	14	240–345	Test point, red, 1 mm	Farnell	
U1	1	TLC555D	IC, timer, low-power, CMOS	TI	SO8
U2	1	TPS2812D	IC, MOSFET driver, dual channel buffer w/regulator	TI	SO8
U3	1	TPS70351PWP	IC, dual 1–A/2–A LDO regulator,	TI	PWP24
—	1	SLVP165, Rev. B	PCB, 2-layer, 2-oz, 3.49”(L) x 2.94”(W) x 0.062”(T)		

1.5 Board Layout

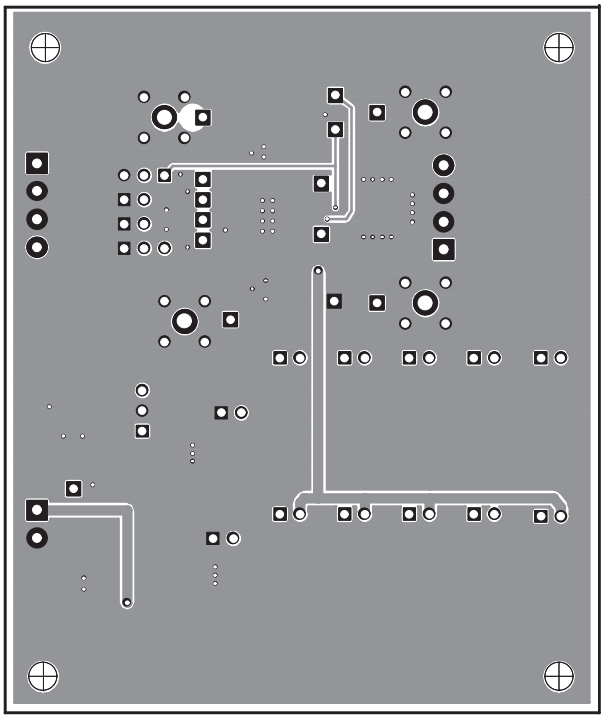
Figures 1–3 through 1-5 show the board layout for the SLVP165B EVM.

Figure 1–3. Top Layer



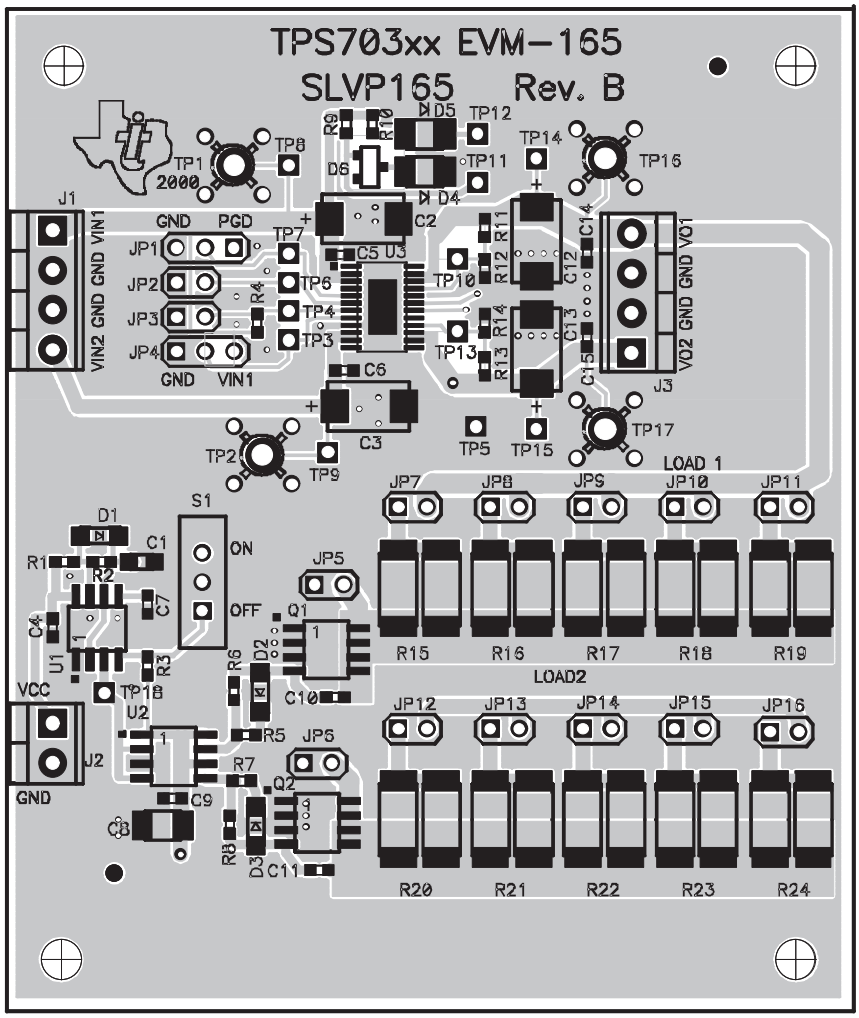
Top Layer

Figure 1–4. Bottom Layer (top view)



Bottom Layer

Figure 1–5. Assembly Drawing (top assembly)



Top Assembly

Chapter 2

EVM Adjustments and Test Points

This chapter explains the following EVM adjustment modes:

- Adjustment by switch and jumper
- Adjustment through changing components

Figure 2–1 shows the locations of the adjustment points on the board.

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2.1 Adjustment by Switch and Jumpers

S1 switches the transient generator on or off. Table 2–1 lists adjustments that can be made by jumpers.

Table 2–1. Jumper Functions

Jumper	Setting	Functional Description
JP1	Short 1-2 – $\overline{\text{MR2}}$ tied to GND	$\overline{\text{RESET}}$ follows $\overline{\text{MR2}}$
	Short 2-3 – $\overline{\text{MR2}}$ tied to PG_1	$\overline{\text{RESET}}$ will go high after a 120 ms delay when V_{OUT2} reaches 95% of its regulated voltage and when PG_1 goes high due to V_{OUT1} reaching 95% of its regulated voltage.
	Open	$\overline{\text{MR2}}$ is disabled
JP2	Shorted – $\overline{\text{MR1}}$ tied to GND	$\overline{\text{RESET}}$ follows $\overline{\text{MR1}}$
	Open	$\overline{\text{MR1}}$ is disabled
JP3	Shorted – $\overline{\text{EN}}$ tied to GND	Enable device outputs
	Open	Disable device outputs
JP4	Short 1-2 – SEQ tied to GND	SEQ low – regulator 1 powers up first with regulator 2 powering up when V_{OUT1} is 83% of max output voltage.
	Short 2-3 – SEQ tied to V_{IN}	SEQ high or left open – regulator 2 powers up first with regulator 1 powering up when V_{OUT2} is 83% of max output voltage
JP5	Shorted – bypass transient generator for regulator 1	Allows continuous load through onboard load resistors on regulator 1.
	Open – engage transient generator for regulator 1	Allows pulsed load through onboard load resistors on regulator 1.
JP6	Shorted – bypass transient generator for regulator 2	Allows continuous load through onboard load resistors on regulator 2.
	Open – engage transient generator for regulator 2	Allows pulsed load through onboard load resistors on regulator 2.
JP7 – JP11	Shorted – include resistor in parallel combination	Increase regulator 1 load from no load to max load.
	Open – remove resistor from parallel combination	Decrease regulator 1 load from max load to no load.
JP12 – JP16	Shorted – include resistor in parallel combination	Increase regulator 2 load from no load to max load.
	Open – remove resistor from parallel combination	Decrease regulator 2 load from max load to no load.

The TPS703xx datasheet, TI Literature number SLVS285, provides further explanation of alternative configurations using the SVS supervisory circuit, power good, manual reset, and enable inputs.

2.2 Adjustment Through Component Changes

Through minor soldering work, the onboard device can be changed to any of the fixed-voltage members of the TPS703xx LDO family. In addition, Table 2–2 summarizes the most common components which a user might wish to replace in order to more fully characterize the LDO.

Table 2–2. Commonly Changed Components

Component	Regulator 1	Regulator 2	EVM Value
Input capacitor	C2	C3	100 µF
Output capacitor	C12	C13	33 µF, 47 µF
Resistors controlling transient pulse generator pulse width and duty cycle (see Table 2-3)	R1, R2	R1, R2	4.3 kΩ, 10 kΩ
Resistor controlling load transient rise time†	R6	R8	510 Ω

† Larger resistance slows rise time.

Table 2–3 gives the equations for computing the resistor sizes necessary for changing the transient pulse width and/or duty cycle.

Table 2–3. Timing Equations

Timing Equations With Diode D1 for Low Duty Cycles	Timing Equations Without Diode D1
$R1 = \frac{t_{on}}{0.693 \times C}$	$R1 = \frac{t_{on} \times (2D - 1)}{0.693 \times D \times C}$
$R2 = \frac{t_{on} \times (1 - D)}{0.693 \times D \times C}$	$R2 = \frac{t_{on} \times (1 - D)}{0.693 \times D \times C}$

Note: t_{on} = desired load on-time [s]
D = on-time duty cycle
C = total capacitance in circuit (1 uF)
RH1, RH2 = Timer resistors value (refer to schematics) [Ω]

2.3 Test Setup

Figure 2–1 shows the test setup. Follow these steps for initial power up of the SLVP165:

1) Adjust the settings of jumpers to fit test requirements (see jumper functions in Table 2-1). Verify that the switch controlling the load transient generator is off, no external load is connected through J3 and that JP5 and JP6 are open to prevent loading through the onboard resistors.

2) Connect a 12-V lab power supply to the V_{CC} input and GND at J2. The polarity is printed on the board. A current limit of 100 mA should be adequate for the test and measure circuit.

3) Connect a second lab power supply (at least capable of supplying 2 A) to the J1 connector at V_{IN1}, V_{IN2}, GND1 and GND2. The polarity is printed on the board. Verify that the lab power supply output voltage limit is set to 6 V and that the output is set to 0 V.

4) Turn on the 12-V lab supply. Turn on the second power supply and ramp the input voltage up to the desired maximum but not higher than 6 V.

5) Verify that the output voltage (measured at the V_{OUT1} and V_{OUT2} pins respectively) has the desired value.

6) Table 2–4 shows the three recommended options for loading each regulator.

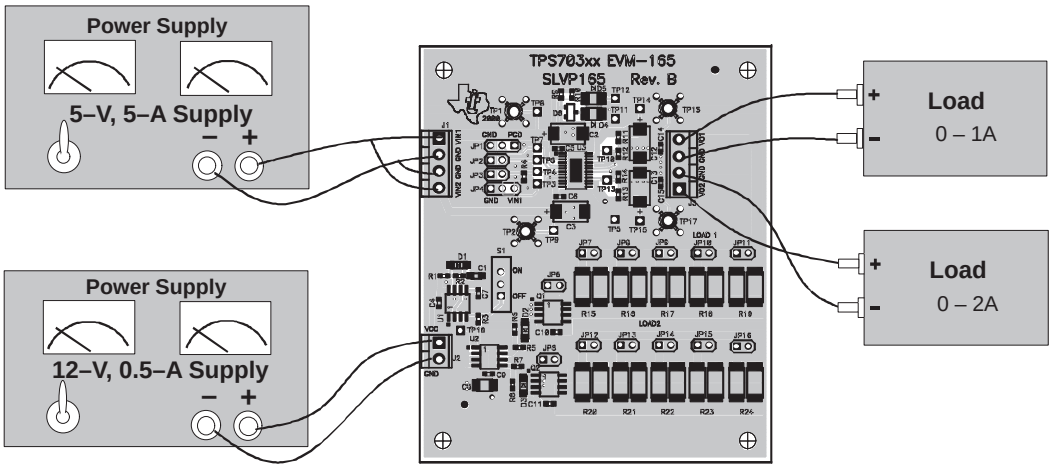
Table 2–4. Regulator Loading Options

Type	JP5–Regulator 1 JP6–Regulator 2	SW_1	External Load
Continuous load off-board	Open	Off	Connected
Continuous load onboard	Shorted	On/off	Not connected
Pulsed load onboard	Open	On	Not connected

Jumpers JP7 – JP11 and JP12 – JP16 vary the current through the onboard resistors from 0 to max load current for regulator 1 and regulator 2 respectively.

> Simultaneous and continuous operation of both regulator outputs at full load may exceed the power dissipation rating of the PWP package. For more information, refer to the thermal information section in the TPS703xx data sheet (literature number SLVS285).

Figure 2–1. Test Setup



Test Set–Up

Note: All wire pairs should be twisted.

Chapter 3

Circuit Design

This chapter describes the LDO circuit design procedure.

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3.1 ESR and Transient Response

LDOs typically require an external output capacitor for stability. In fast transient response applications, capacitors are used to support the load current while the LDO amplifier is responding. In most applications, one capacitor is used to support both functions.

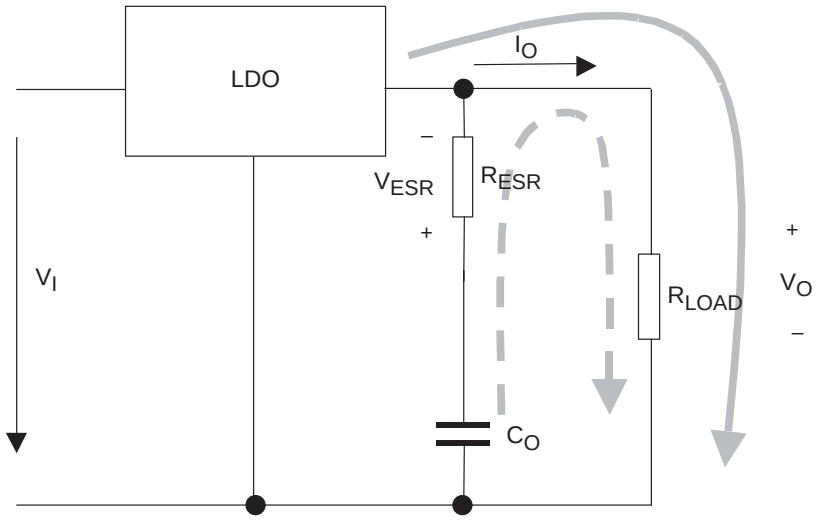
Besides its capacitance, every capacitor also contains parasitic impedances. These impedances are resistive as well as inductive. The resistive impedance is called equivalent series resistance (ESR), and the inductive impedance is called equivalent series inductance (ESL). The equivalent schematic diagram of any capacitor can therefore be drawn as shown in Figure 3–1.

Figure 3–1. ESR and ESL

In most cases one can neglect the effect of inductive impedance ESL. Therefore, the following application focuses mainly on the parasitic resistance ESR.

Figure 3–2 shows the output capacitor and its parasitic impedances in a typical LDO output stage.

Figure 3–2. LDO Output Stage With Parasitic Resistances ESR



In steady state (dc state condition), the load current is supplied by the LDO (solid arrow) and the voltage across the capacitor is the same as the output voltage ($V(C_0) = V_O$). This means no current is flowing into or out of the C_0 branch.

If I_O suddenly increases (transient condition), the LDO is not able to supply the sudden current need due to its response time (t_1 in Figure 3–3). Therefore, capacitor C_0 provides the current for the new load condition (dashed arrow). C_0 now acts like a battery with an internal resistance, R_{ESR}. Depending on the current demand at the output, a voltage drop will occur at R_{ESR}. This voltage is shown as V_{ESR} in Figure 3–2.

When C_O is conducting current to the load, initial voltage at the load will be $V_O = V(C_O) – V_{ESR}$. Due to the discharge of C_O, the output voltage V_O will drop continuously until the response time t_1 of the LDO is reached and the LDO will resume supplying the load. From this point, the output voltage starts rising again until it reaches the regulated voltage. This period is shown as t_2 in Figure 3–3.

The figure also shows the impact of different ESRs on the output voltage. The left brackets show different levels of ESRs where number 1 displays the lowest and number 3 displays the highest ESR.

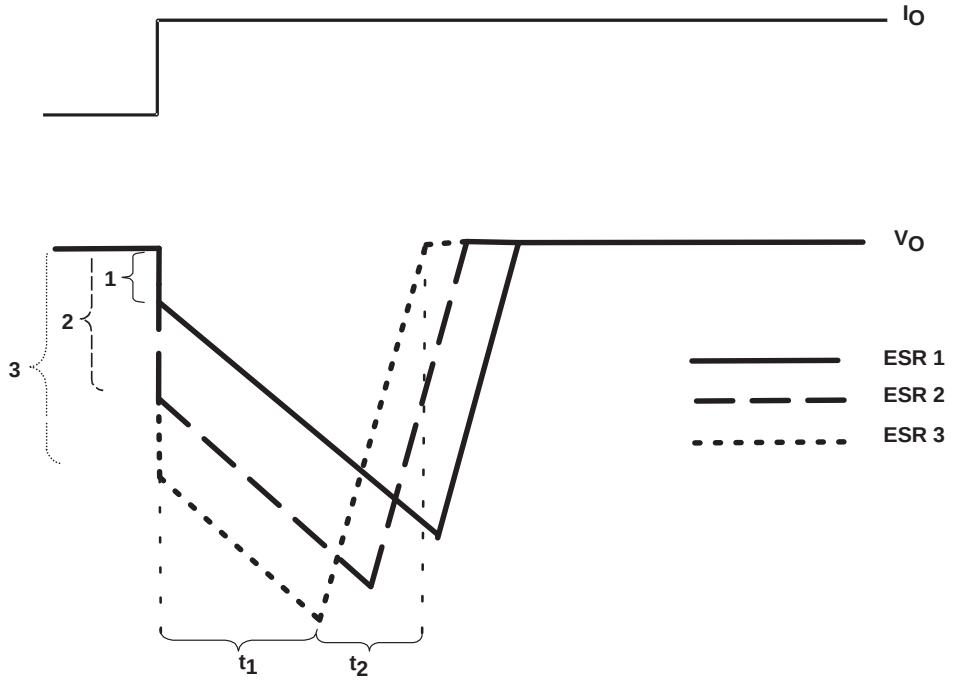
From above, the following conclusions can be drawn:

- The higher the ESR, the larger the droop at the beginning of load transient.
- The smaller the output capacitor, the faster the discharge time and the bigger the voltage droop during the LDO response period.

3.1.1 Conclusion

To minimize the transient output droop, capacitors must have a low ESR and be large enough to support the minimum output voltage requirement for a given LDO response time.

Figure 3–3. Correlation of Different ESRs and Their Influence to the Regulation of V_O at a Load Step From Low-to-High Output Current



Chapter 4

Test Results

This chapter presents laboratory test results for the TPS70351 LDO design.

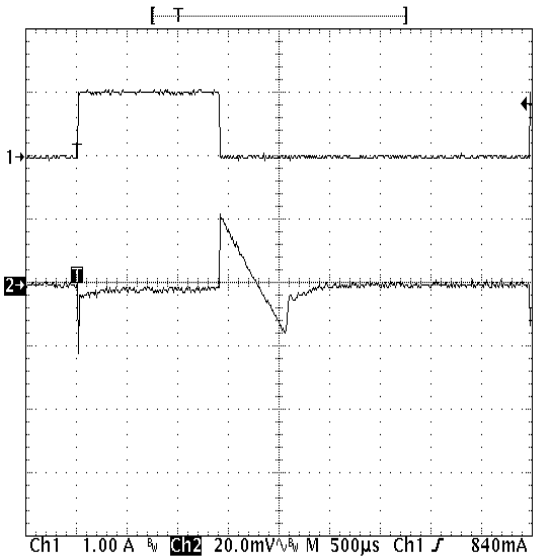
Topic **Page**

4.1 Test Results

Figures 4–1 through 4–10 show the results of various test conditions using the TPS70351 device.

In Figure 4–1, the onboard transient generator is used to pulse I_{OUT1} (CH1) on V_{OUT1} (CH2–AC) from 1 mA to 1 A. A current loop was added to the board to measure the load current.

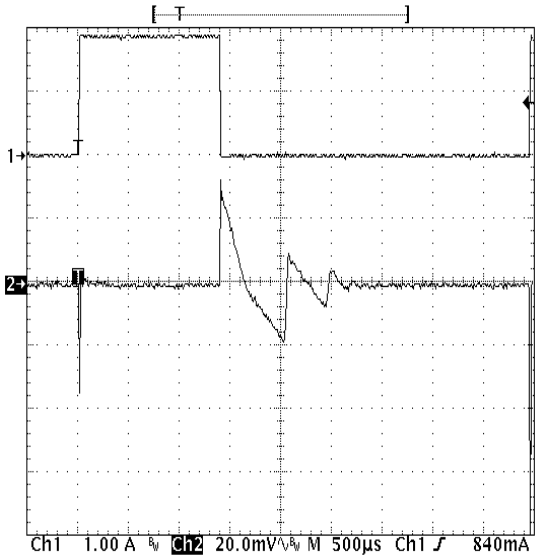
Figure 4–1. V_{OUT1} Load Transient



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} = 1 mA to 1 A
V_{OUT2} = no load

In Figure 4–2, the onboard transient generator is used to pulse I_{OUT2} (CH1) on V_{OUT2} (CH2–AC) from 1 mA to 2 A. A current loop was added to the board to measure the load current.

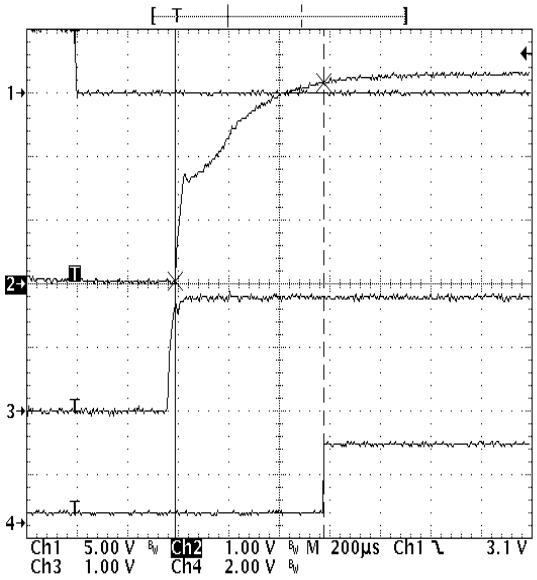
Figure 4–2. V_{OUT2} Load Transient



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} = no load
V_{OUT2} = 1 mA to 2 A

In Figure 4-3, $\overline{\text{ENABLE}}$ (CH1) is pulsed. When SEQ is high, V_{OUT1} (CH2) powers up after V_{OUT2} (CH3) reaches 85% of its regulated output. PG1 (CH4), which is tied to $\overline{\text{MR1}}$, goes high when V_{OUT1} reaches 95% of its regulated voltage.

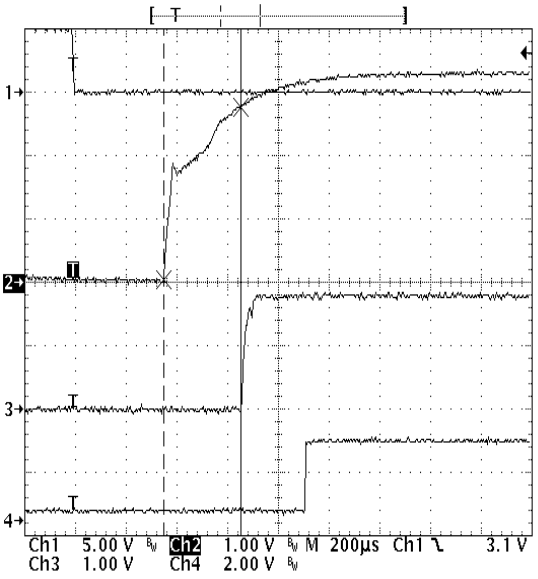
Figure 4–3. Timing When SEQUENCE Is High



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
I_{OUT1} = 0.6 A
I_{OUT2} = 1.1 A

In Figure 4-3, $\overline{\text{ENABLE}}$ (CH1) is pulsed. When SEQ is low, V_{OUT2} (CH3) powers up after V_{OUT1} (CH2) reaches 85% of its regulated output. PG1 (CH4), which is tied to $\overline{\text{MR1}}$, goes high when V_{OUT1} reaches 95% of its regulated voltage.

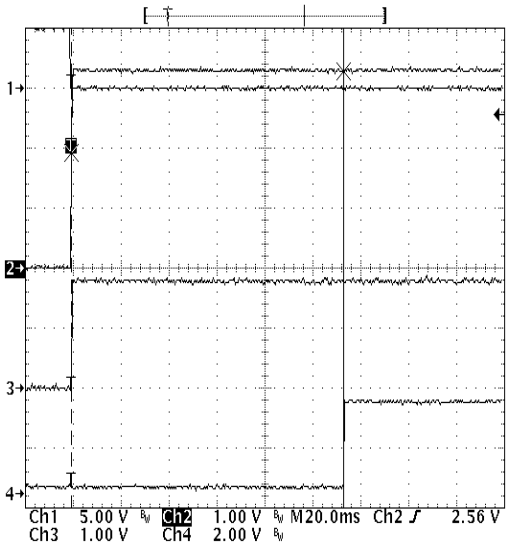
Figure 4–4. Timing When SEQUENCE Is Low



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
I_{OUT1} = 0.6 A
I_{OUT2} = 1.1 A

In Figure 4–5, $\overline{\text{ENABLE}}$ (CH1) is pulsed. SEQUENCE can be either low or high. With PG1 tied to $\overline{\text{MR1}}$, $\overline{\text{RESET}}$ (CH4) goes high 120 ms after both V_{OUT1} and V_{OUT2} have reached 95% of their respective regulated output voltages.

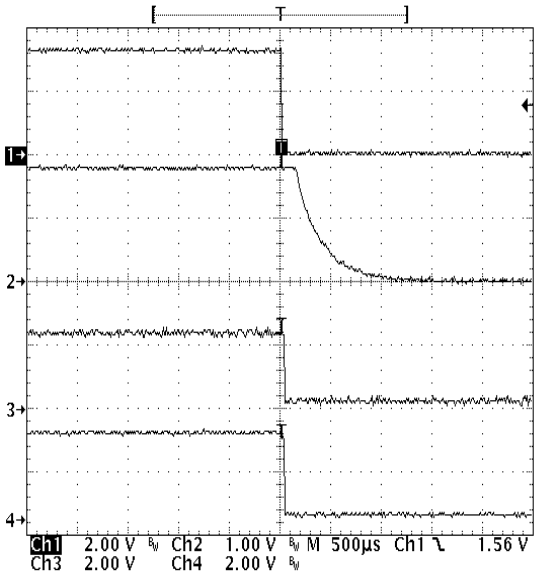
Figure 4–5. Timing Including $\overline{\text{RESET}}$



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
I_{OUT1} = 0.6 A
I_{OUT2} = 1.1 A

In Figure 4–6, V_{OUT1} (CH1) is pulsed into a shorted condition. Because SEQUENCE is low, V_{OUT2} (CH2) is disabled after the internal current limit circuitry disables V_{OUT1}. PG1 (CH3), which is tied to $\overline{\text{MR1}}$, goes low when V_{OUT1} falls below 95% of its regulated voltage. $\overline{\text{RESET}}$ (CH4) follows $\overline{\text{MR1}}$.

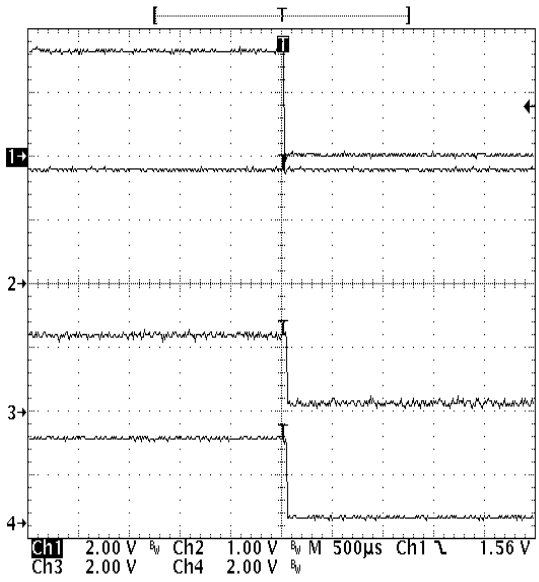
Figure 4–6. Timing When SEQUENCE Is Low, With a Fault on V_{OUT1}



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} (CH1) = no load to a shorted condition
V_{OUT2} (CH2) = 1 mA load

In Figure 4–7, V_{OUT1} (CH1) is pulsed into a shorted condition. Because SEQUENCE is high, V_{OUT2} (CH2) is not disabled after the internal current limit circuitry disables V_{OUT1}. PG1 (CH3), which is tied to $\overline{MR1}$, goes low when V_{OUT1} falls below 95% of its regulated voltage. $\overline{RESET}$ (CH4) follows $\overline{MR1}$.

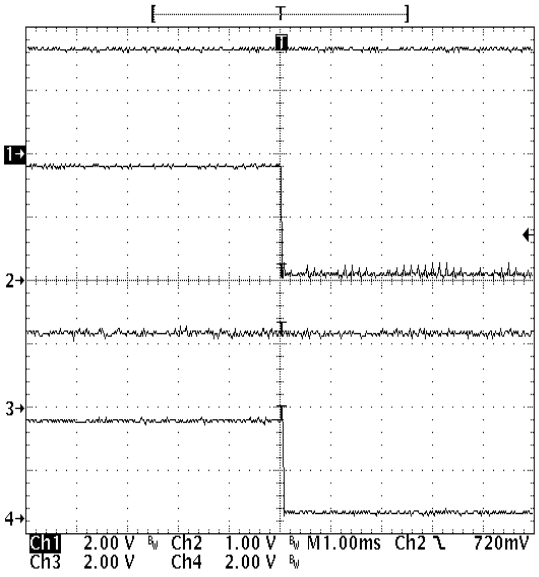
Figure 4–7. Timing When SEQUENCE Is High, With a Fault on V_{OUT1}



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} (CH1) = no load to a shorted condition
V_{OUT2} (CH2) = 1 mA load

In Figure 4–8, V_{OUT2} (CH2) is pulsed into a shorted condition. Because SEQUENCE is low, V_{OUT1} (CH1) is not disabled after the internal current limit circuitry disables V_{OUT2}. PG1 (CH3), which is tied to $\overline{MR1}$, stays high. $\overline{RESET}$ (CH4) goes low when V_{OUT2} falls below 95% of its regulated voltage.

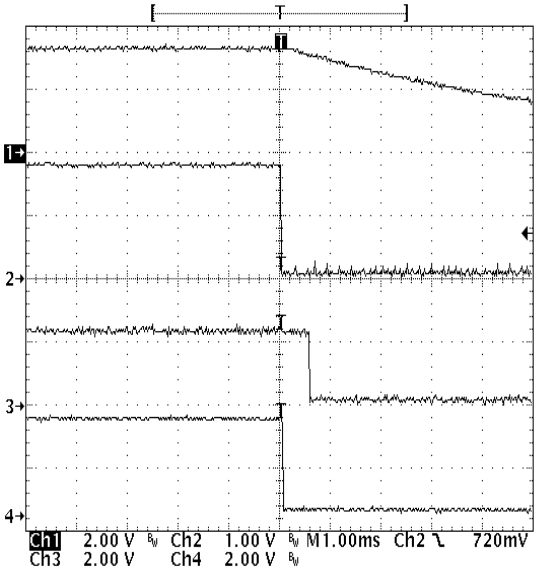
Figure 4–8. Timing When SEQUENCE Is Low, With a Fault on V_{OUT2}



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} (CH1) = 1 mA load
V_{OUT2} (CH2) = no load to a shorted condition

In Figure 4–9, V_{OUT2} is pulsed into a shorted condition. Because SEQUENCE is high, V_{OUT1} is disabled after the internal current limit circuitry disables V_{OUT2}. PG1 (CH3), which is tied to $\overline{MR1}$, goes low when V_{OUT1} falls below 95% of its regulated voltage. $\overline{RESET}$ (CH4) goes low when V_{OUT2} falls below 95% of its regulated voltage.

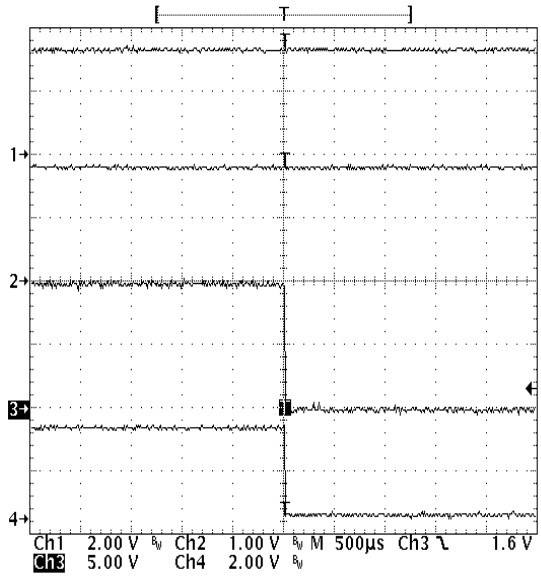
Figure 4–9. Timing When SEQUENCE Is High, With a Fault on V_{OUT2}



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} (CH1) = 1 mA load
V_{OUT2} (CH2) = no load to a shorted condition

In Figure 4–10, $\overline{MR}$ (CH3) is toggled low and $\overline{RESET}$ (CH4) follows $\overline{MR1}$. V_{OUT1} (CH1) and V_{OUT2} (CH2) are unaffected.

Figure 4–10. Timing When $\overline{MR}$ Is Toggled



V_{IN1} = 4.3 V
V_{IN2} = 2.8 V
V_{OUT1} (CH1) = 1 mA load
V_{OUT2} (CH2) = no load