Application Note

TPS546E25 and TPS546C25 Advanced Product Errata

ABSTRACT

This memo documents issues found with TPS546E25 and TPS546C25 advanced product silicon, which differ from the respective data sheets as mentioned in the errata items below. Each issue has a description, a system impact, a mitigation, and a disposition. The devices are 4V to 18V input, 50A and 35A step-down converters with PMBus® and telemetry, available in a 5x6mm or 4x5mm package. The preliminary data sheets are downloaded by clicking the following links.

- TPS546E25: 4V to 18V input, 50A step-down converter in 5x6mm QFN package
- TPS546C25: 4V to 18V input, 35A step-down converter in 4x5mm QFN package

Evaluation modules are available to aid in the development of the design and are orderable in the product folder of each device.

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Trademarks

PMBus® is a registered trademark of SMIF, Inc..
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1 Introduction

Although the PTPS546E25RXXR and PTPS546C25RXXR are functional, please be aware that the samples available are preliminary and the devices are not released to full production.

1. These samples are for evaluation only and are not intended for qualification testing or production.
2. ESD testing is still in progress. Please follow ESD precautions when handling the component.
3. Qualification testing is still in progress.

2 General

2.1 No Immediate Disable From Soft Start

- Description: If the device is turned off with the OPERATION register, the CPA bit from ON_OFF_CONFIG causes the device to use TOFF_DELAY and TOFF_FALL. The delay only takes effect when the CTRL in is used to disable the device.
- System Impact: The device shutdown is not immediate with the OPERATION register command.
- Workaround or Mitigation: None
- Disposition: Design fix planned for final silicon.

2.2 Power Stage Over Temperature Protect

- Description: The over-temperature protection integrated into the high-side and low-side MOSFETs can trigger at a lower than intended temperature, below 125°C when the VIN input voltage is greater than 13.5V.
- System Impact: The device can shutdown with die temperature of 90°C when operating above 13.5V input.
- Workaround/Mitigation: Limit testing to VIN less than 13.5V or die temperature less than 90°C.
- Disposition: Design fix planned for final silicon.

2.3 Negative Current Limit

- Description: The negative current limit is triggering approximately 2A lower than intended.
- System Impact: The device sinks more current than selected by the negative OC level.
- Workaround/Mitigation: None
- Disposition: Design fix planned for final silicon.

2.4 Programmable Reference DAC gain low

- Description: The gain of the programmable reference DAC used to set the output voltage is low. The gain is trimmed for offset at 0.6V. Output voltage set-point error increases as the reference voltage is programmed away from 0.6V up to 1mV per 100mV. Vref equals 501mV when programmed to 0.5V and 699mV when programmed to 0.7V.
- System Impact: Reduced output voltage set-point accuracy for high and low reference voltages.
- Workaround or Mitigation: None
- Disposition: Design fix planned for final silicon.

3 Security

3.1 Standard Write Protection Does Not Work on Secondary Device

- Description: When standard write protection is on, writing to blocked registers is ACK'd.
- System Impact: Blocked registers accept commands when unnecessary to on secondary devices.
- Workaround or Mitigation: None
- Disposition: Design fix planned for final silicon.

3.2 Device Does Not NACK Incorrect Passkey Per PMBus 1.5

- Description: When a passkey other than the correct passkey or all zeros is entered, the device does not NACK (not acknowledged) and IVD (invalide data) as per the PMBus 1.5 standard.
- System Impact: Incorrect NACK and IVD behavior.
- Workaround or Mitigation: Feature planned for final silicon.
- Disposition: Design fix planned for final silicon.

3.3 Device Does Not Alternate Between Lock and Unlock When Passkey is Written Multiple Times

- Description: When a passkey is initially set, the device does not lock until a STORE RESTORE cycle. This is incorrect behavior per the PMBus 1.5 specification.
- System Impact: Incorrect locking behavior when passkey is toggled.
- Workaround or Mitigation: To lock the device, a STORE RESTORE cycle is needed.
- Disposition: Design fix planned for final silicon.

4 Stacking Interface and Operation of P2_PLUS_Commands

4.1 Inconsistent P2_PLUS_*(various)* NACKing by Secondary Device

- Description: Some P2_PLUS commands that can be allowed are NACKed on secondary devices, but not all the time.
- System Impact: An incorrect fault response is signaled from these PS-PLUS commands, such as IOUT_CAL_OFFSET and OT_FAULT_RESPONSE. Other Commands include MFR_REVISION with P2_PLUS_WRITE, PINSTRAP_RESULT_OVR with P2_PLUS_WRITE, FUSION_ID1 with P2_PLUS_READ, ALERT_MASK_BYTE with P2_PLUS_WRITE.
- Workaround or Mitigation: Use the unique address for the secondary device instead of P2_PLUS for the specified commands, or ignore faults when using P2_PLUS commands to the specified commands on secondary devices.
- Disposition: Design fix planned for final silicon.

4.2 IOUT_OC_FAULT_LIMIT Not Readable on Secondary Device Via P2_PLUS_READ

- Description: A P2_PLUS_READ to IOUT_OC_FAULT_LIMIT with PHASE = 0x01 is ACKing all bytes, but is not responding with any data.
- System Impact: Reading the IOUT_OC_FAULT_LIMIT with P2_PLUS_READ is not possible.
- Workaround or Mitigation: Do not use P2_PLUS_READ and read the register directly.
- Disposition: Design fix planned for final silicon.

4.3 STACK_CONFIG Writable When Should be Read Only

- Description: STACK_CONFIG is Read or Write for some bits, and ACK writes but ignores the write value.
- System Impact: A write is accepted due to the ACK, but is ignored.
- Workaround or Mitigation: Treat the STACK_CONFIG register as read only, and properly configure the stack configuration through pinstrap only.
- Disposition: Design fix planned for final silicon where all bits are read only and writes are NACK'd with an ivd response.

4.4 Secondary Device ACK's Write to Some Read-Only Registers

- Description: PHASE, IOUT_OC_LV_FAULT_RESPONSE, IOUT_OC_LV_FAULT_LIMIT, STATUS_BYTE, and STATUS_WORD ACK writes to these read only registers on the secondary device.
- System Impact: Improper ACK
- Workaround or Mitigation: None, as the write is not accepted even though an ACK is sent.
- Disposition: Design fix planned for final silicon.

4.5 Secondary Device NACKs All P2_PLUS_WRITE Commands With PHASE = 0xFF

- Description: Secondary devices NACK P2_PLUS_WRITEs for a variety of different commands (with PHASE = 0xFF) on the second command frame.
- System Impact: Improper NACK
- Workaround or Mitigation: Use the unique address for the secondary device instead of P2_PLUS for the specified commands, or ignore faults when using P2_PLUS commands to the specified commands on secondary devices.
- Disposition: Design fix planned for final silicon.

4.6 Secondary Asserts IVD for P2_PLUS_READ of ALERT_MASK_*(various)* With PHASE = 0xFF

- Description: When a P2_PLUS_READ command with PHASE = 0xFF is issued, primary device correctly responds with data and secondary NACKs as expected. However, the secondary device is asserting IVD and SMBAlert from this transaction when the device must be ignoring.
- System Impact: Improper assertion of IVD and SMBAlert
- Workaround or Mitigation: Use the unique address for the secondary device instead of P2_PLUS for the specified commands, or ignore faults when using P2_PLUS commands to the specified commands on secondary devices.
- Disposition: Design fix planned for final silicon.

4.7 Secondary Device NACKing P2_PLUS_*(various)* With Valid PHASE

- Description: The secondary device NACKs all P2_PLUS_*(various)* commands with PHASE = 0x01 (valid). However, in other test cases, the device ACKs as expected.
- System Impact: Inconsistent response to P2_PLUS_ commands.
- Workaround or Mitigation: Use the unique address for the secondary device instead of P2_PLUS for the specified commands, or ignore faults when using P2_PLUS commands to the specified commands on secondary devices.
- Disposition: Design fix planned for final silicon.

4.8 Invalid PAGE is ACKed for P2_PLUS_READ Command

- Description: If the P2_PLUS_READ command is issued with invalid PAGE, valid PHASE (0x00), and valid PMBus command code, the primary device ACKs the transaction and responds with data when the device must NACK.
- System Impact: Improper ACK.
- Workaround or Mitigation: Do not use P2_PLUS_READ command or verify that the PAGE is correct.
- Disposition: Design fix planned for final silicon.

5 PMBUS

5.1 READ_IOUT Data Format is Not Correct

- Description: The data format for READ_IOUT is incorrectly using an unsigned 11-bit mantissa to represent current values from 0LSB to 2047LSB.
- System Impact: READ_IOUT values greater than mid-scale (16A for TPS546B25 and 32A for TPS546C25/E25) decode at negative values using LINEAR11 decoding.
- Workaround or Mitigation: Custom Decoding of READ_IOUT using 11-bit unsigned mantissa or correcting negative values by adding 64A to any negative values reported by READ_IOUT.
- Disposition: Design fix planned for final silicon, which changes the fixed exponent for READ_IOUT to -5 (TPS546B25/TPS546C25) or -4 (TPS546E25).

5.2 OPERATION Not changing VOUT_SOURCE When OFF = b’1

- Description: Bit 6 of OPERATION (OFF bit) is combined with Rail Enable for MARGIN selection by OPERATION [5:2] so that MARGIN is ignored when OPERATOIN [6] = b’1.
- System Impact: Vout control can not change from VOUT_COMMAND to VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW when desired.
- Workaround or Mitigation: When writing OPERATION for MARGIN_HIGH or MARGIN_LOW, set OPERATION[7:6] to b’10.
- Disposition: Design fix planned for final silicon.

5.3 PIN_DETECT_OVERRIDE Power-On Source Control Inverted

- Description: Advance product silicon has this definition of bits in PIN_DETECT_OVERRIDE inverted.
  - 0b = Initialize command value from Pin Detection Table on Power On or RESTORE_USER_ALL
  - 1b = Initialize command value from NVM source on Power On or RESTORE_USER_ALL
- System Impact: Can cause confusion or errors as firmware moves between products.
- Workaround or Mitigation: Use current definition for programming samples.
- Disposition: Design fix planned for final silicon correcting bit definitions b’0 = Restore from NVM and b’1 = Restore from Pin Detection.

5.4 PIN_DETECT_OVERRIDE Bit 15 OVRD_STACK is Not Working Correctly

- Description: Bit 15 of (D8) PIN_DETECT_OVERRIDE disables Pin Detection when set to 1b.
- System Impact: Can cause confusion or errors as firmware moves between products.
- Workaround or Mitigation: Do not use PIN_DETECT_OVERRIDE bit 15.
- Disposition: Design fix planned for final silicon correcting bit definition to OVRD_STACK.

5.5 STATUS_OTHER FRST_2_ALRT Does Not Assert STATUS_BYTE or STATUS_WORD Other Bit 0

- Description: When FRST_2_ALRT STATUS_OTHER is asserted, this does not show up in STATUS_BYTE or STATUS_WORD bit 0.
- System Impact: Improper propagation of status bit
- Workaround or Mitigation: If you get a PMBus ALERT and you do not see a bit set in STATUS_WORD or STATUS_BYTE, check (7Fh) STATUS_OTHER.
- Disposition: Design fix planned for final silicon.

5.6 Clamping VOUT by VREF Range Not setting VOUT_MAX_MIN in STATUS_VOUT

- Description: If the Output voltage is programmed above the maximum range of the reference DAC voltage, the output voltage is clamped to 0.75V / VOUT_SCALE_LOOP, but the VOUT_MAX_MIN bit in STATUS_VOUT is not set.
- System Impact: No status warning bit set indicating that the programmed VOUT was not achieved.
- Workaround or Mitigation: Use the correct VOUT_SCALE_LOOP value to set output voltage. Check VOUT using READ_VOUT after setting VOUT.
- Disposition: Design fix planned for final silicon.

6 Summary

Although the PTPS546E25RXXR and PTPS546C25RXXR are functional, please be aware that the samples available are preliminary and the devices are not released to full production. Please address any questions to the TI E2E design support forum.

7 References

- Texas Instruments, TPS546E25 4V to 18V Input, 50A, 4 × Stackable, Synchronous Buck Converter With PMBus® and Telemetry data sheet
- Texas Instruments, TPS546C25 4V to 18V Input, 35A, 4 × Stackable, Synchronous Buck Converter With PMBus® and Telemetry data sheet

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