Radiation Report

TPS7H4013-SEP Total Ionizing Dose (TID) Radiation Report

ABSTRACT

This report discusses the results of the TID testing for the Texas Instruments TPS7H4013-SEP 4.5V to 14V input, 3A radiation tolerant synchronous buck converter.

The study was done to determine TID effects under high dose rate (HDR) up to 50krad(Si) after 84h anneal at room temperature (resulting in an effective dose rate of 165mrad(Si)/s).

The results show that all samples passed within the specified limits up to 50krad(Si).

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Trademarks

1 Device Information

1.1 Product Description

The TPS7H4013-SEP is a 14V, 3A synchronous buck converter optimized for use in a space environment. High efficiency and reduced component count are achieved through peak current mode control.

The wide voltage range of the TPS7H4013-SEP enables the device to be used as a point of load regulator to convert directly from a 12V or 5V rail. The output voltage start-up ramp is controlled by the SS_TR pin. Power sequencing is possible with the EN and PWRGD pins. The device can be configured with up to four devices in parallel without an external clock for increased current capabilities. Additionally, various features are included such as differential remote sensing, selectable current limit, a flexible fault input pin, and configurable compensation.

1.2 Device Details

Table 1-1 lists the device information used in the TID HDR characterization.

Table 1-1. Device and Exposure Details

TID Exposure Details	
TI Device	TPS7H4013-SEP
Package	44-pin HTSSOP (DDW)
TI Part Name	TPS7H4013MDDWTSEP
Technology	LBC7 (Linear BiCMOS 7)
Assembly Lot Number	5397451
Quantity Tested	HDR: 30 Devices • Five biased and five unbiased units at 20krad (Si) levels • Five biased and five unbiased units at 30krad (Si) levels • Five biased and five unbiased units at 50krad (Si) levels • Five control/correlation units with no exposure
HDR Radiation Facility	Texas Instruments, Dallas, TX
HDR Dose Level	50krad(Si)
HDR Dose Rate	156.71 rads(Si)/s ionizing radiation dose rate
HDR Radiation Source	Gamma cell Co-60
Irradiation Temperature	Ambient, room temperature controlled to 25°C (±6°C) per MIL-STD-883 and MIL-STD-750.

50krad biased and unbiased devices were annealed for 84 hours at room temperature with their respective bias condition resulting in an effective dose rate of 165mrad(Si)/s.

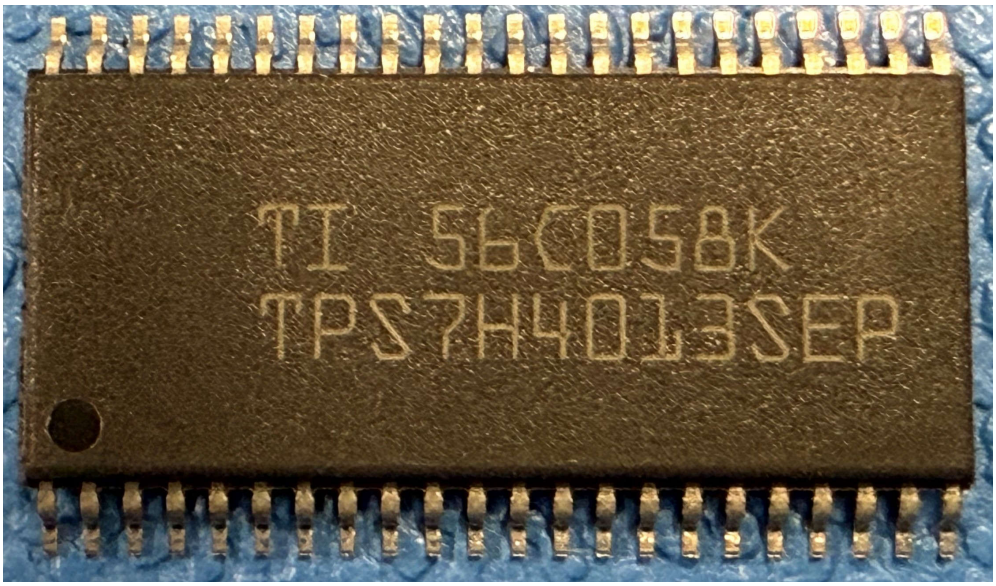

Figure 1-1. TPS7H4013-SEP Device Used in Exposure (Front)

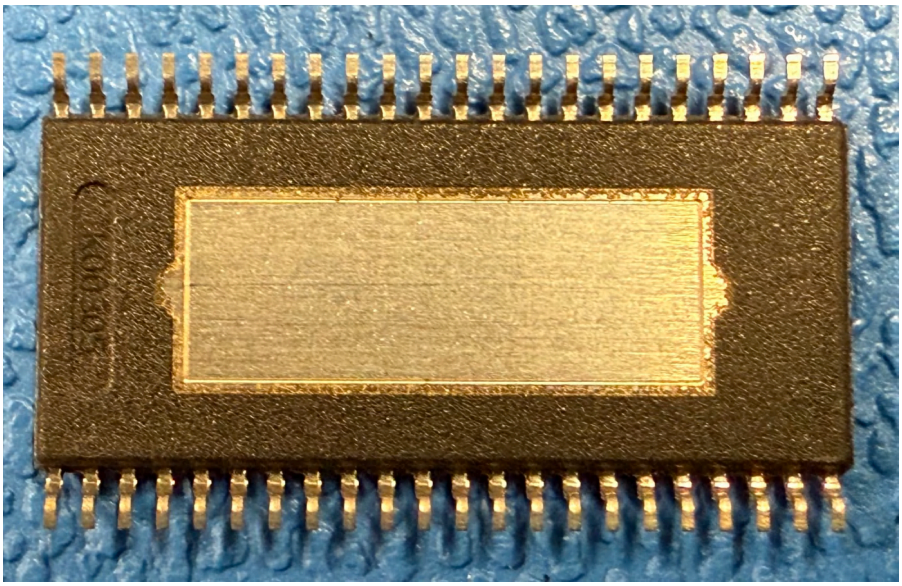

Figure 1-2. TPS7H4013-SEP Device Used in Exposure (Back)

2 Total Dose Test Setup

2.1 Test Overview

The TPS7H4013-SEP was tested according to MIL-STD-883, Test Method 1019.9. For this testing, Condition A was used. The product was irradiated up to the target radiation level, and then put through full electrical parametric testing on the production Automated Test Equipment (ATE). All devices remained functional passing all parametric test limits.

2.2 Test Description and Facilities

The TPS7H4013-SEP HDR exposure was performed on biased and unbiased devices in a Co-60 gamma cell at TI facility in Dallas, Texas. The unattenuated dose rate of this cell was 156.71rads(Si)/s. The 50krad(Si) biased devices were annealed with the respective biased condition for 84 hours and retested. The effective dose rate for these devices was 165mrad(Si)/s. ATE test limits are set per data sheet electrical limits based on qualification and characterization data.

2.3 Test Setup Details

The devices under HDR exposure were tested in two conditions, biased and unbiased, as described in the following sections.

2.3.1 Unbiased

For the unbiased HDR condition, the exposure was performed with all pins grounded.

2.3.2 Biased

Figure 2-1 shows the diagram for HDR exposure with biased condition.

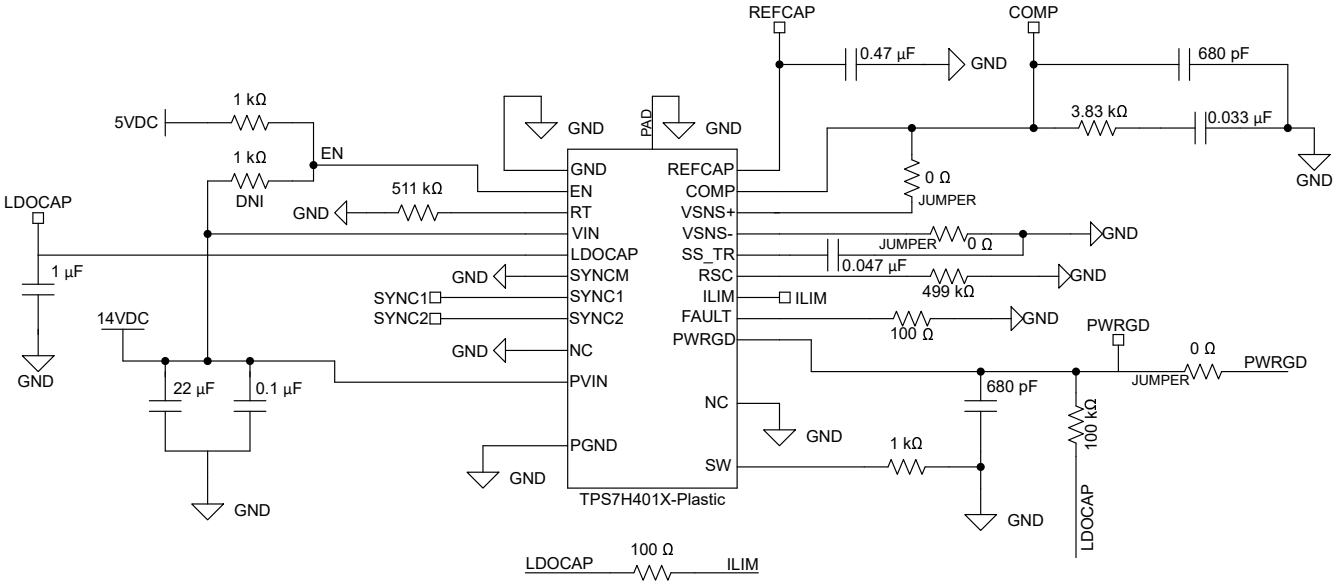

Figure 2-1. TPS7H4013-SEP Bias Diagram

2.4 Biased Test Configuration and Condition

HDR devices were stressed up to 50 krad(Si) for biased and unbiased conditions.

Table 2-1. HDR: Biased Device Information

Total Samples: 15		
Exposure Levels		
20 krad(Si)	30krad(Si)	50krad(Si)
1, 2, 3, 4, 5	11, 12, 13, 14, 15	77, 78, 79, 80, 81

Table 2-2. HDR: Unbiased Device Information

Total Samples: 15		
Exposure Levels		
20krad(Si)	30krad(Si)	50krad(Si)
6, 7, 8, 9, 10	16, 17, 18, 19, 20	27, 28, 29, 30, 31

3 TID Characterization Test Results

3.1 TID Characterization Summary Results

The parametric data for the TPS7H4013-SEP passes up to 50krad(Si) HDR TID irradiation. The drifts of the electrical parameters through HDR were within the data sheet limits.

Overall, the TPS7H4013-SEP showed a strong degree of hardness to HDR TID irradiation up to 50krad(Si) for both biased and unbiased exposure conditions. The measurements taken post-irradiation for each sample set showed a marginal shift for most parameters at each dose level for both biased and unbiased. The parameters that did show a greater degree of change pre- and post- irradiation were still within the electrical performance characteristics specified in the data sheet electrical parameters. See Data Sheet Electrical Parameter Characteristics for electrical parameters. Test numbers are listed only for parameters tested for TID.

See Appendix for HDR report up to 50krad(Si).

3.2 Data Sheet Electrical Parameter Characteristics

Over 4.5V ≤ VIN ≤ 14V, PVIN = VIN, VSNS- = 0V, open loop configuration, IOUT = 0A, TA = 25°C, unless otherwise noted.

Table 3-1. Data Sheet Electrical Parameter Characteristics

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
V_{UVLOR_PVIN}	PVIN internal UVLO rising threshold			1, 2, 3	3.2	3.4	3.6	V
$V_{UVLOHYST\_PVIN}$	PVIN internal UVLO hysteresis			1, 2, 3	425	450	500	mV
V_{UVLOR_VIN}	VIN internal UVLO rising threshold			1, 2, 3	3.4	3.6	3.8	V
$V_{UVLOHYST\_VIN}$	VIN internal UVLO hysteresis			1, 2, 3	140	155	170	mV
I_{SHDN_VIN}	VIN shutdown supply current	V_{EN} = 0V	VIN = 4.5V	1, 2, 3		2	2.9	mA
			VIN = 14V	1, 2, 3		2	3	
I_{SHDN_PVIN}	PVIN shutdown supply current	V_{EN} = 0V	PVIN = 4.5V	1, 2, 3		2.6	3.5	mA
			PVIN = 14V	1, 2, 3		3.5	4.7	
I_{Q_VIN}	VIN operating quiescent current (non switching)	V_{EN} = 7V, VSNS+ = 1V		1, 2, 3		2.6	5	mA
ENABLE								
$V_{EN(rising)}$	Enable rising threshold (turn-on)			1, 2, 3	0.555	0.61	0.655	V
$V_{EN(falling)}$	Enable falling threshold (turn-off)			1, 2, 3	0.455	0.51	0.554	V
$t_{EN(delay)}$	Enable propogation delay	EN high to SW high, SS pin open		1, 2, 3		52	100	µs
$I_{EN(LKG)}$	Enable input leakage current	V_{EN} = 7V		1, 2, 3		2	100	nA

Table 3-1. Data Sheet Electrical Parameter Characteristics (continued)

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE AND SENSE								
V_{REF}	Internal voltage reference (including error amplifier VIO)	See datasheet	T_A = –55°C	3	0.594	0.598	0.603	V
			T_A = 25°C	1	0.596	0.6	0.603	
			T_A = 125°C	2	0.597	0.6	0.604	
$V_{REF(internal)}$	Internal voltage reference (without error amplifier included)	$V_{REF(internal)} = V_{SS\_TR}$		1, 2, 3	0.593	0.6	0.606	V
V_{BG}	Bandgap voltage (voltage at the REFCAP pin)	C_{REFCAP} = 470nF		1, 2, 3	1.184	1.2	1.222	V
$I_{VSNS+(LKG)}$	VSNS+ input leakage current	VSNS+ = 0.6V		1, 2, 3		10	30	nA
ERROR AMPLIFIER								
V_{IO}	Error amplifier input offset voltage	VSNS+ = 0.6V		1, 2, 3	–2.9		2.9	mV
g_{mEA}	Error amplifier transconductance	–10µA < I_{COMP} < 10µA, V_{COMP} = 1V	T_A = –55°C	11	1400	2050	2700	µS
			T_A = 25°C	9	1200	1650	2100	
			T_A = 125°C	10	1000	1250	1500	
EA_{DC}	Error amplifier DC gain	VSNS+ = 0.6V				11500		V/V
EA_{ISRC}	Error amplifier source	V_{COMP} = 1V, 100mV input overdrive		1, 2, 3	90	125	200	µA
EA_{ISNK}	Error amplifier sink	V_{COMP} = 1V, 100mV input overdrive		1, 2, 3	90	125	200	µA
EA_{Ro}	Error amplifier output resistance					7		MΩ
EA_{BW}	Error amplifier bandwidth	Unity gain bandwidth				9		MHz
g_{mps}	Power stage transconductance	V_{COMP} = 0.75V	TPS7H4013, HTSSOP	1, 2, 3	3.5	6.2	9.2	S
OVERCURRENT PROTECTION								
I_{OC_HS1}	High-side switch current limit threshold 1(4)	R_{SHORT} = 100mΩ	TPS7H4013, HTSSOP	1, 2, 3		5.6	7.7	A
I_{OC_HS2}	High-side switch current limit threshold 2	VIN = 12V, R_{SHORT} ≈ 4mΩ	TPS7H4013, HTSSOP	1, 2, 3		6.8		A

Table 3-1. Data Sheet Electrical Parameter Characteristics (continued)

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
$I_{OC\_LS(sink)}$	Low-side switch sinking overcurrent threshold	T_A = –55°C		3		2		A
		T_A = 25°C		1		1.9		A
		T_A = 125°C		2		1.7		A
$COMP_{SHDN}$	COMP shutdown voltage			1, 2, 3	1.7	1.9	2.1	V
$t_{COMP(delay)}$	COMP shutdown delay			9, 10, 11		30		µs
SOFT START AND TRACKING								
t_{SS}	Soft start time	V_{SS_TR} from 10% to 90%, $V_{OUT(set)}$ = 3.3V	CSS = 5.6nF	9, 10, 11		1.5		ms
			CSS = 22nF	9, 10, 11	4.7	5.8	7.3	
			CSS = 100nF	9, 10, 11		24.7		
$R_{SS(discharge)}$	Soft start discharge pull-down resistor			1, 2, 3	200	442	700	Ω
$SS_{startup}$	Maximum voltage on SS before startup(5)					20		mV
SLOPE COMPENSATION								
SC	Slope compensation, TPS74013	f_{SW} = 100kHz, VIN = 12V	RSC = 499kΩ			–0.5		A/µs
			RSC = 1.5MΩ			–0.2		
		f_{SW} = 500kHz, VIN = 12V	RSC = 100kΩ			–2.8		A/µs
			RSC = 499kΩ			–1.2		
			RSC = 1.5MΩ			–0.8		
		f_{SW} = 1000kHz, VIN = 12V	RSC = 100kΩ			–4		A/µs
			RSC = 499kΩ			–2		
			RSC = 1.5MΩ			–1.5		
MINIMUM ON TIME AND DEAD TIME								
$t_{on(min)}$	Minimum on time	50% to 50% of VIN, I_{SW} = 2A	VIN = 4.5V	9, 10, 11		210	235	ns
			VIN = 5V	9, 10, 11		213	250	
			VIN = 12V	9, 10, 11		199	250	
			VIN = 14V	9, 10, 11		199	250	
$t_{off(min)}$	Minimum off time	I_{SW} = 2A				306		ns
t_{dead}	Dead time					70		ns
SWITCHING FREQUENCY AND SYNCHRONIZATION								
f_{SW}	RT programmed switching frequency	R_{RT} = 511kΩ		4, 5, 6	90	100	120	kHz
		R_{RT} = 90.9kΩ		4, 5, 6	450	500	550	kHz
		R_{RT} = 40.2kΩ	VIN = 4.5V	4, 5, 6	850	1000	1150	kHz
			5 ≤ VIN ≤ 14	4, 5, 6	870	1000	1170	

Table 3-1. Data Sheet Electrical Parameter Characteristics (continued)

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
t_{SYNC_D}	SYNC1 to SW delay	SYNC1 input	VIN = 4.5V	9, 10, 11	150	256	390	ns
			5V ≤ VIN ≤ 14V	9, 10, 11	160	240	310	
			VIN = 12V, IOUT = 3A			246		
$V_{SYNC1(IH)}$	SYNC1 input high threshold			1, 2, 3			1.7	V
$V_{SYNC1(IL)}$	SYNC1 input low threshold			1, 2, 3	0.7			V
f_{SYNC}	SYNC1 input frequency range			4, 5, 6	100		1000	kHz
D_{SYNC}	SYNC1 input duty cycle range	External clock duty cycle		4, 5, 6	40%		60%	
$t_{CLK\_E\_I}$	External clock to internal clock detection time	RT populated		9, 10, 11		2	5	$(1/f_{sw})$ s
$t_{CLK\_I\_E}$	Internal clock to external clock detection time	RT populated		9, 10, 11		1	2	$(1/f_{sw})$ s
POWER GOOD AND THERMAL SHUTDOWN								
$PWRGD_{LOW\_F\%}$	PWRGD falling threshold (fault), low	Threshold for PWRGD (VSNS+ as percent of V_{REF})	VSNS+ falling	1, 2, 3	89%	92%	95%	
$PWRGD_{LOW\_R\%}$	PWRGD rising threshold (good), low	Threshold for PWRGD (VSNS+ as percent of V_{REF})	VSNS+ rising	1, 2, 3	92%	95%	98%	
$PWRGD_{HIGH\_R\%}$	PWRGD rising threshold (fault), high	Threshold for PWRGD (VSNS+ as percent of V_{REF})	VSNS+ rising	1, 2, 3	105%	108%	112%	
$PWRGD_{HIGH\_F\%}$	PWRGD falling threshold (good), high	Threshold for PWRGD (VSNS+ as percent of V_{REF})	VSNS+ falling	1, 2, 3	102%	105%	109%	
$I_{PWRGD(LKG)}$	Output high leakage	VSNS+ = V_{REF}, V_{PWRGD} = 7V		1, 2, 3		50	500	nA
$V_{PWRGD(OL)}$	Power good output low	$I_{PWRGD(SINK)}$ = 0mA to 2mA		1, 2, 3		250	300	mV

Table 3-1. Data Sheet Electrical Parameter Characteristics (continued)

PARAMETER		TEST CONDITIONS		SUB-GROUP	MIN	TYP	MAX	UNIT
V_{INMIN_PWRGD}	Minimum VIN for valid PWRGD output	Measured when V_{PWRGD} ≤ 0.5V at 100µA		1, 2, 3		1	2	V
$T_{SD(enter)}$	Thermal shutdown enter temperature					175		°C
$T_{SD(exit)}$	Thermal shutdown exit temperature					140		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis					35		°C
MOSFET								
$R_{DS\_ON\_HS}$	High-side switch resistance at I_{HS} = 3A, TPS7H4013, HTSSOP	PVIN = 4.5V	T_A = –55°C	3		28	41	mΩ
			T_A = 25°C	1		36	47	
			T_A = 125°C	2		46	62	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		26	38	mΩ
			T_A = 25°C	1		33	46	
			T_A = 125°C	2		41	56	
$R_{DS\_ON\_LS}$	Low-side switch resistance at I_{LS} = 3A, TPS7H4013, HTSSOP	PVIN = 4.5V	T_A = –55°C	3		20	31	mΩ
			T_A = 25°C	1		28	39	
			T_A = 125°C	2		41	50	
		5V ≤ PVIN ≤ 14V	T_A = –55°C	3		20	29	mΩ
			T_A = 25°C	1		27	37	
			T_A = 125°C	2		39	48	

4 Applicable and Reference Documents

4.1 Applicable Documents

- Texas Instruments, *TPS7H401X-SP and TPS7H401X-SEP 4.5V to 14V Input, 3A and 6A Radiation Hardened Synchronous Buck Converter,* data sheet.
- Texas Instruments, *TPS7H4013-SEP (TPS7H4013EVM-CVAL) Evaluation Module User's Guide,* user's guide.

4.2 Reference Documents

Texas Instruments total ionizing dose radiation (total dose) test procedure follows the standards put forth in MIL-STD-883 TM 1019. The document can be found at the DLA website.

A Appendix A: HDR Results

This appendix contains the HDR TID report data. The following decoder serves as a reference guide for the test parameters shown in the appendix:

NCAT|HEADER/PIN/V_VIN/I_LOAD/R_RT/CONDITION/@SPEC_ID_PARM

Please reference Table A-1 for an example implementation of this decoder.

Table A-1. Decoder Implementation, Example Test: IDD|STATIC/VIN/14////@VIN_SHDN_CURR_14V

Test Category	Header	Pin Name	Input Voltage	Load Current	Frequency Set Resistor Value	Condition	Specification Identifier
IDD	STATIC	VIN	14V	N/A	N/A	N/A	@VIN_SHDN_CURR_14

Note that the absence of identifiers in a parameter name indicates that the identifier is not applicable. For instance, this test does not have the device driving an external load, and thus no load current is specified.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (November 2025) to Revision A (December 2025)	Page
• Corrected device information	2
• Updated appendix data	12

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