Radiation Report

UC1834-SP Total Ionizing Dose (TID) Lookahead Radiation Report

ABSTRACT

This report discusses the results of the Total Ionizing Dose (TID) testing for the Texas Instruments high efficiency linear regulator UC1834-SP. The study was done to determine TID effects under low dose rate (LDR) up to 40 krad(Si). The results show that all samples passed within the specified limits up to 40 krad(Si).

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Trademarks

1 Device Information

1.1 Product Description

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high-gain amplifier and 200-mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of the regulator can be implemented. A current sense amplifier with a low, adjustable threshold can be used to sense and limit currents in either the positive or negative supply lines.

1.2 Device Details

Table 1-1 lists the device information used in the initial TID LDR characterization.

Table 1-1. Device and Exposure Details

TID LDR Details: 30 krad(Si) and 40 krad(Si)	
Package	16-pin J
Technology	JI-PWR-1
Quantity Tested	20
LDR Radiation Facility	VPT Rad, Chelmsford, MA
LDR Dose Level	30 krad(Si), 40 krad(Si)
LDR Dose Rate	0.01 rad(Si)/s
LDR Radiation Source	Gamma cell Co60 (JLS-81-22)
Irradiation Temperature	Ambient, room temperature

Figure 1-1. UC1834-SP Device Used in Exposure

2 Total Dose Test Setup

2.1 Test Overview

The UC1834 was tested according to MIL-STD-883, Test Method 1019.9. For this testing, Condition D was used. For this test, one group was irradiated up to a radiation level of 30 krad(Si)/s, and the other group was irradiated up to a radiation level of 40 krad(Si)/s, and then put through electrical parametric testing on the Automated Test Equipment (ATE). Post irradiation testing showed that the devices were functional, passing all parametric tests.

2.2 Test Description and Facilities

The UC1834 LDR exposure was performed on biased and unbiased devices in a Co60 gamma cell under a 10-mrad(Si)/s exposure rate. The dose rate of the irradiator used in the exposure ranges from < 10 mrad(Si)/s to a maximum of approximately 84 rad(Si)/s, determined by the distance from the source. For the LDR exposure (10 mrad(Si)/s), the test box was positioned approximately 2 m from the source.

The exposure boards are housed in a lead-aluminum box (as specified in MIL-STD-883 TM 1019.9) to harden the gamma spectrum and minimize dose enhancement effects. The irradiator calibration is maintained by Logmire Laboratories using Thermoluminescence Dosimeters (TLDs) traceable to the National Institute of Standards and Technology (NIST) and the dosimetry was verified using TLDs prior to the radiation exposures. After exposure, the devices were packed in dry ice (per MIL-STD-883 Method 1019.9 section 3.10) and returned to TI Dallas for a post radiation electrical evaluation using Texas Instruments production Automated Test Equipment (ATE). ATE test limits are set per SMD electrical limits based on initial qualification and characterization data. Post-radiation measurements were taken within 30 minutes of removing the devices from the dry ice container. The devices were allowed to reach room temperature prior to electrical post-radiation measurements.

2.3 Test Setup Details

The devices under LDR exposure were irradiated in both biased and unbiased conditions. Both conditions are described as follows.

1. **Unbiased** - - For the unbiased LDR conditions, the exposure was performed with all pins grounded.
2. **Biased** - - *Figure 2-1* shows the diagram for LDR exposure with biased condition.

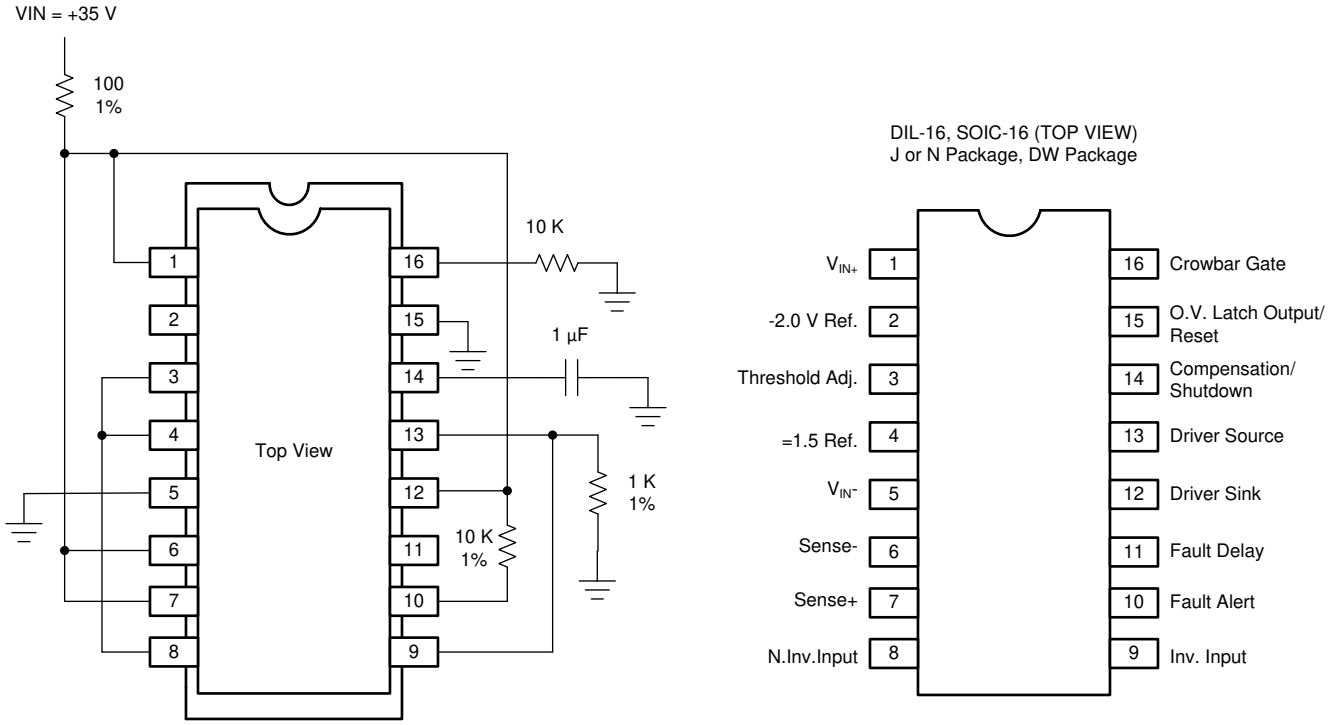

Figure 2-1. Bias Diagram Used in TID Exposure

2.4 Test Configuration and Condition

LDR devices were stressed at 30 krad(Si) and 40 krad(Si) for biased and unbiased conditions.

Table 2-1. LDR = 30- and 40-krad(Si)/s Biased Device Information

Total Samples: 10	
Exposure Levels:	
30 krad(Si)	40 krad(Si)
17, 18, 19, 20, 21	11, 12, 13, 14, 15

Table 2-2. LDR = 30- and 40-krad(Si)/s Unbiased Device Information

Total Samples: 10	
Exposure Levels:	
30 krad(Si)	40 krad(Si)
1, 2, 3, 4, 5	6, 7, 8, 9, 10

3 Total Ionizing Dose Characterization Test Results

The parametric data for the UC1834 passes up to 40-krad(Si) LDR TID.

The drift of SMD electrical parameters through LDR were within the pre-rad characterization limits.

See Appendix A for graphs and drifts.

3.1 Specification Compliance Matrix

Unless otherwise stated, these specifications apply for TA = −55°C to +125°C. VIN+ = 15 V, VIN− = 0 V, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1834-SP Datasheet				Test(s)
		MIN	TYP	MAX	UNIT	
Turn-on Characteristics						
Standby Supply Current			5.5	7	mA	Standby Supply Current
+1.5 V Reference						
Output Voltage	T_j = 25°C	1.485	1.5	1.515	V	+1.5V Reference Voltage
Line Regulation	V_{in+} = 5 to 35V		1	10	mV	+1.5V Ref Line Reg Vin5 to 35V
Load Regulation	I_{out} = 0 to 2mA		1	10	mV	+1.5V REF Load Reg Iout2ma
–2 V Reference (Note 2)						
Output Voltage (Referenced to V_{in+})	Tj+ = 25°C	-2.04	-2	-1.96	V	-2.0V Reference Vin15V
Line Regulation	V_{in+} = 5 to 35V		1.5	15	mV	-2.0V Ref Line Reg Vin5 to 35V
Output Impedance			2.3		kΩ	-2.0V Ref Zout
Error Amplifier Section						
Input Offset Voltage	V_{cm} = 1.5V		1	6	mV	E/A Input Offset V Vin15V Vcm1.5V
Input Bias Current	V_{cm} = 1.5V		-1	-4	µA	E/A Input Bias I Vin15V Vcm1.5V E/A Input Bias Current (-Input) E/A Input Bias Current (+Input)
Input Offset Current	V_{cm} = 1.5V		0.1	1	µA	E/A Input Bias Offset Vin15V Vcm1.5V
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{in+} , Pin 13, 20Ω to V_{IN-}	50	65		dB	E/A Avol OutP14 SinkVin Source20ohms
CMRR	V_{CM} = 0.5 to 33V, V_{IN+}= 35V	60	80		dB	E/A CMRR Vcm0.5 to 35V
PSRR	V_{IN+}= 5 to 35V, V_{CM}= 1.5V	70	100		dB	E/A PSRR Vin5 to 35V Vcm1.5V
Driver Section						
Maximum Output Current		200	350		mA	Driver Max Current Vin15V Vcm1.5V
Saturation Voltage	I_{out} = 100 mA		0.5	1.2	V	VSaturation Vin15V Vcm1.5V I100ma
Output Leakage Current	Pin 12 = 35V,Pin 13 =V_{in+}, Pin 14 = V_{IN-}		0.1	50	µA	Drv Leakage I Sink35V P13,P14Vin- Drv Leakage @35V E/A Shutdown Drv Leakage @35V; Latch Shutdown
Shutdown Input Voltage at Pin 14	I_{OUT} ≤ 100µA, Pin 13 = V_{IN-}, Pin 12 = V_{in+}	0.4	1		V	Shutdown Input V Iout<100ua

3.1 Specification Compliance Matrix (continued)

Unless otherwise stated, these specifications apply for TA = −55°C to +125°C. VIN+ = 15 V, VIN− = 0 V, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1834-SP Datasheet				Test(s)
		MIN	TYP	MAX	UNIT	
Shutdown Input Current at Pin 14	Pin 14 = V_{IN-}, Pin 12 = V_{IN+},I_{OUT}≤ 100µA, Pin 13 = V_{IN-}		-100	-150	µA	Shutdown Input Current @0V
Fault Amplifier Section						
Under-and Over-Voltage Fault Threshold	V_{CM} = 1.5V, @ E/A Inputs	120	150	180	mV	UV Fault Threshold Vcm1.5V OV Fault Threshold Vcm1.5V
Common Mode Sensitivity	V_{IN+} = 35V, V_{CM} = 1.5 to 33V		-0.4	-0.8	%/V	UV Thold Cmv Sens Vcm1.5-33V Vin35V OV Thold Cmv Sens Vcm1.5-33V Vin35V
Supply Sensitivity	V_{CM} = 1.5V, V_{IN+} = 5 to 35V		-0.5	-1.0	%/V	UV Supply Sens Vcm1.5V Vin5-35V OV Supply Sens Vcm1.5V Vin5-35V
Fault Delay		30	45	60	ms/µF	Fault Delay
Fault Alert Output Current		2	5		mA	Fault Alert Output Current
Fault Alert Saturation Voltage	I_{out} = 1mA		0.2	0.5	V	Fault Alert Saturation Iout1ma
O.V. Latch Output Current		2	4		mA	OV Latch Output Current
O.V. Latch Saturation Voltage	I_{out} = 1mA		1.0	1.3	V	OV Latch Saturation Voltage Iout1ma
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	V	OV Latch Out Reset Voltage
Crowbar Gate Current		-100	-175		mA	Crowbar Gate Current
Crowbar Gate Leakage Current	V_{IN+} = 35V, Pin 16 = V_{in-}		-0.5	-50	µA	Crowbar Gate Leakage Vin35V P16Vin-
Current Sense Amplifier Section						
Threshold Voltage	Pin 4 Open, V_{CM} =V_{IN+} or V_{IN-}	130	150	170	mV	CS Thold VcmVin+ Adjopen CS Thold VcmVin- Adjopen
	Pin 4 = 0.5V, V_{CM} =V_{IN+} or V_{IN-}	40	50	60		CS Thold Adj0.5V VcmVin+ CS Thold Adj0.5V VcmVin-
Threshold Supply Sensitivity	Pin 4 Open, V_{CM} = V_{IN-}, V_{IN+} = 5 to 35V		-0.1	-0.3	%/V	CS Supply Sens Adjopen Vin5-35V
Adj. Input Current	Pin 4 = 0.5V		-2	-10	µA	CS Thold Adj Input Current Adj0.5V
Sense Input Bias Current	V_{CM} = V_{IN+}		100	200	µA	Sense Input Bias Current VcmVin+
	V_{CM} = V_{IN-}		-100	-200		Sense Input Bias Current VcmVin-

4 Applicable and Reference Documents

4.1 Applicable Documents

- *UC1834 Radiation-Hardness-Assured High Efficiency Linear Regulator* data sheet

4.2 Reference Documents

Texas Instruments total ionizing dose radiation (total dose) test procedure follows the standards put forth in MIL-STD-883 TM 1019. The document can be found at the DLA website.

A TID Data

Table A-1. Bias vs Unbias Mapping

Note: All devices were tested at either 30 krad(Si)/s or 40 krad(Si)/s. The biased devices are labeled "31" and "41" in the data in order to create separation between biased and unbiased devices. The purpose of this table is to map the biased and unbiased devices.

krad(Si)	Description	Unit #
30	30-krad(Si) UNBIASED	1, 2, 3, 4, 5
31	30-krad(Si) BIASED	17, 18, 19, 20, 21
40	40-krad(Si) UNBIASED	6, 7, 8, 9, 10
41	40-krad(Si) BIASED	11, 12, 13, 14, 15

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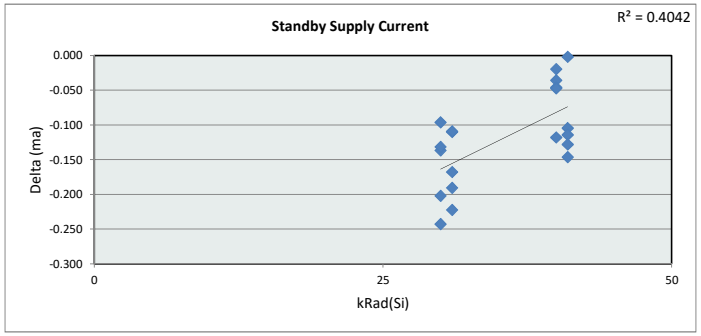
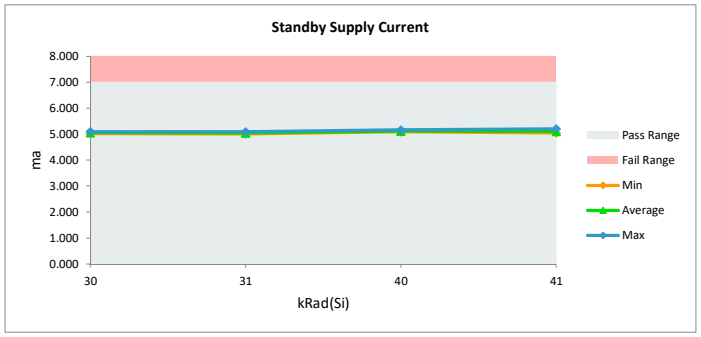
	Standby Supply Current		
Test Site			
Tester			
Test Number			
Unit	mA	ma	
Max Limit	7	7	
Min Limit	0	0	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	5.235	5.098	-0.137
30	2	5.170	5.039	-0.132
30	3	5.142	5.045	-0.096
30	4	5.266	5.023	-0.243
30	5	5.257	5.055	-0.202
40	6	5.122	5.102	-0.020
40	7	5.199	5.163	-0.036
40	8	5.222	5.104	-0.118
40	9	5.171	5.125	-0.046
40	10	5.137	5.090	-0.047
31	17	5.199	5.089	-0.110
31	18	5.230	5.007	-0.222
31	19	5.194	5.026	-0.168
31	20	5.141	5.031	-0.109
31	21	5.237	5.046	-0.190
41	11	5.203	5.201	-0.002
41	12	5.218	5.072	-0.146
41	13	5.209	5.104	-0.104
41	14	5.156	5.042	-0.114
41	15	5.222	5.094	-0.128
	Max	5.266	5.201	-0.002
	Average	5.196	5.078	-0.119
	Min	5.122	5.007	-0.243
	Std Dev	0.042	0.049	0.066



	Standby Supply Current			
Test Site				
Tester				
Test Number				
Max Limit	7	ma		
Min Limit	0	ma		
kRad(Si)	30	31	40	41
LL	0.000	0.000	0.000	0.000
Min	5.023	5.007	5.090	5.042
Average	5.052	5.040	5.117	5.103
Max	5.098	5.089	5.163	5.202
UL	7.000	7.000	7.000	7.000



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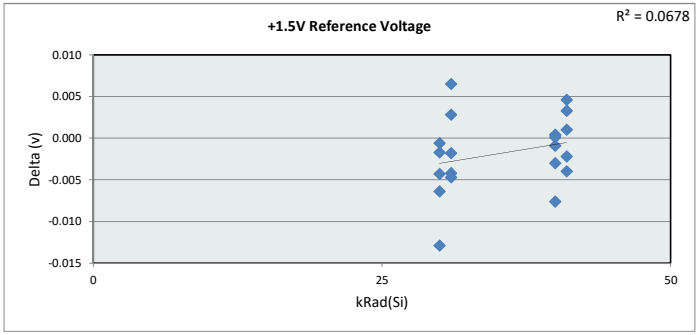
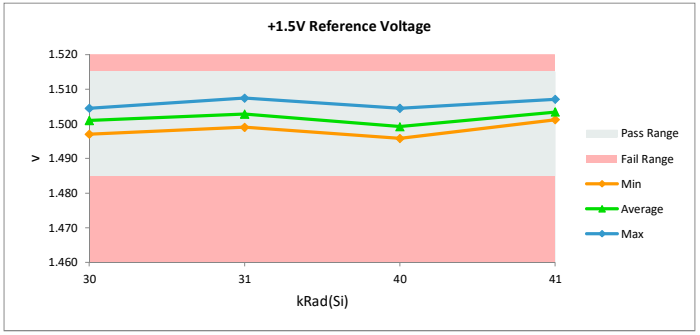
	+1.5V Reference Voltage		
Test Site			
Tester			
Test Number			
Unit	V	v	
Max Limit	1.515	1.515	
Min Limit	1.485	1.485	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	1.503	1.503	-0.001
30	2	1.507	1.500	-0.006
30	3	1.502	1.501	-0.002
30	4	1.510	1.497	-0.013
30	5	1.509	1.505	-0.004
40	6	1.496	1.496	0.000
40	7	1.505	1.505	-0.001
40	8	1.503	1.500	-0.003
40	9	1.503	1.496	-0.008
40	10	1.499	1.499	0.000
31	17	1.498	1.504	0.007
31	18	1.506	1.504	-0.002
31	19	1.503	1.499	-0.004
31	20	1.504	1.499	-0.005
31	21	1.505	1.507	0.003
41	11	1.503	1.507	0.005
41	12	1.499	1.502	0.003
41	13	1.502	1.503	0.001
41	14	1.503	1.501	-0.002
41	15	1.508	1.504	-0.004
	Max	1.510	1.507	0.007
	Average	1.503	1.502	-0.002
	Min	1.496	1.496	-0.013
	Std Dev	0.004	0.003	0.004



	+1.5V Reference Voltage			
Test Site				
Tester				
Test Number				
Max Limit	1.515	v		
Min Limit	1.485	v		
kRad(Si)	30	31	40	41
LL	1.485	1.485	1.485	1.485
Min	1.497	1.499	1.496	1.501
Average	1.501	1.503	1.499	1.503
Max	1.505	1.507	1.505	1.507
UL	1.515	1.515	1.515	1.515



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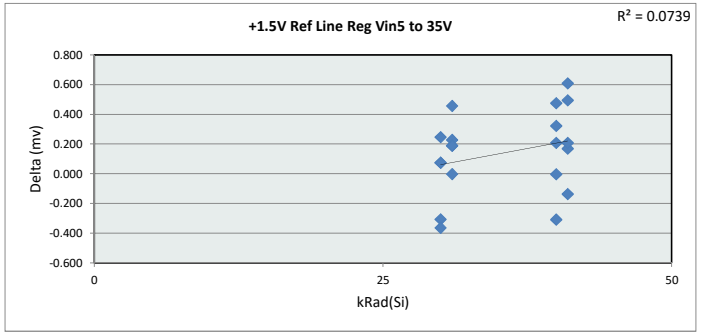
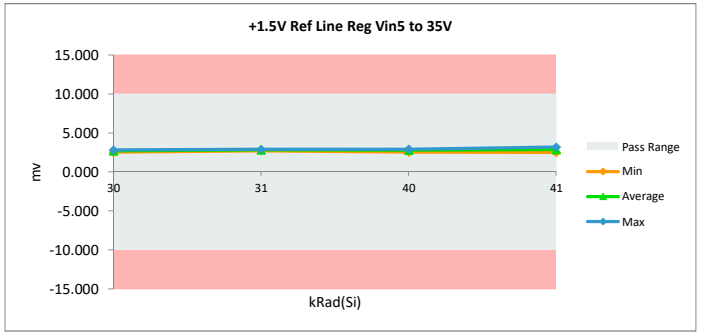
	+1.5V Ref Line Reg Vin5 to 35V		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	10	10	
Min Limit	-10	-10	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	2.749	2.823	0.075
30	2	2.577	2.823	0.246
30	3	2.844	2.537	-0.307
30	4	2.901	2.537	-0.364
30	5	2.749	2.823	0.075
40	6	2.863	2.555	-0.308
40	7	2.577	2.898	0.321
40	8	2.768	2.765	-0.003
40	9	2.443	2.917	0.474
40	10	2.691	2.898	0.207
31	17	2.672	2.899	0.227
31	18	2.730	2.728	-0.002
31	19	2.634	2.823	0.189
31	20	2.443	2.899	0.456
31	21	2.653	2.842	0.189
41	11	2.443	2.937	0.493
41	12	2.730	2.898	0.169
41	13	2.653	2.517	-0.136
41	14	2.577	3.184	0.607
41	15	2.672	2.879	0.207
	Max	2.901	3.184	0.607
	Average	2.668	2.809	0.141
	Min	2.443	2.517	-0.364
	Std Dev	0.132	0.166	0.272



	+1.5V Ref Line Reg Vin5 to 35V			
Test Site				
Tester				
Test Number				
Max Limit	10	mv		
Min Limit	-10	mv		
kRad(Si)	30	31	40	41
LL	-10.000	-10.000	-10.000	-10.000
Min	2.537	2.728	2.555	2.517
Average	2.709	2.838	2.807	2.883
Max	2.823	2.900	2.917	3.184
UL	10.000	10.000	10.000	10.000



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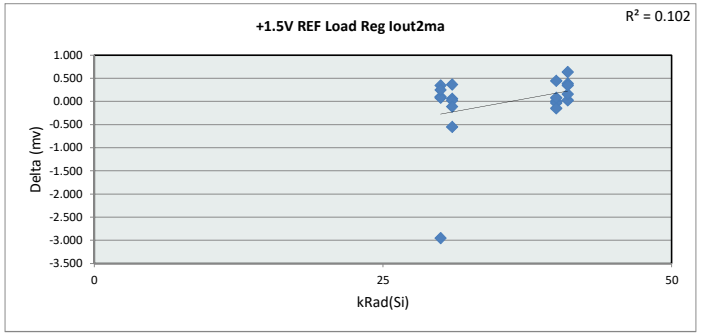
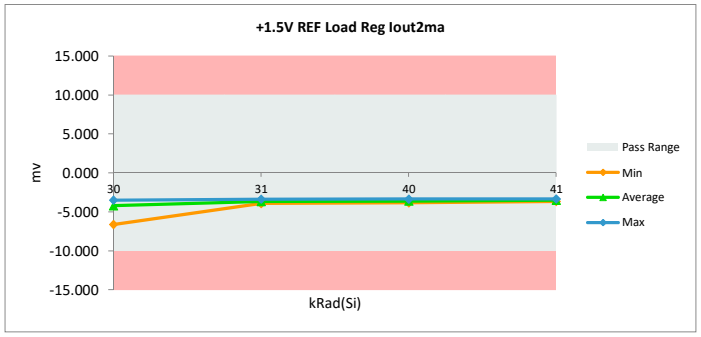
	+1.5V REF Load Reg Iout2ma		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	10	10	
Min Limit	-10	-10	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-3.588	-3.491	0.097
30	2	-3.665	-6.619	-2.954
30	3	-3.837	-3.491	0.346
30	4	-3.970	-3.891	0.079
30	5	-3.837	-3.586	0.250
40	6	-3.837	-3.833	0.004
40	7	-3.627	-3.661	-0.034
40	8	-3.512	-3.661	-0.149
40	9	-3.646	-3.566	0.080
40	10	-3.798	-3.356	0.442
31	17	-3.722	-3.663	0.059
31	18	-3.741	-3.376	0.365
31	19	-3.760	-3.739	0.021
31	20	-3.531	-3.644	-0.112
31	21	-3.378	-3.930	-0.551
41	11	-3.665	-3.642	0.023
41	12	-3.970	-3.337	0.633
41	13	-3.837	-3.451	0.385
41	14	-3.818	-3.661	0.157
41	15	-3.875	-3.528	0.347
	Max	-3.378	-3.337	0.633
	Average	-3.731	-3.756	-0.026
	Min	-3.970	-6.619	-2.954
	Std Dev	0.154	0.694	0.736



	+1.5V REF Load Reg Iout2ma			
Test Site				
Tester				
Test Number				
Max Limit	10	mv		
Min Limit	-10	mv		
kRad(Si)	30	31	40	41
LL	-10.000	-10.000	-10.000	-10.000
Min	-6.619	-3.930	-3.833	-3.661
Average	-4.216	-3.670	-3.615	-3.524
Max	-3.491	-3.376	-3.356	-3.337
UL	10.000	10.000	10.000	10.000



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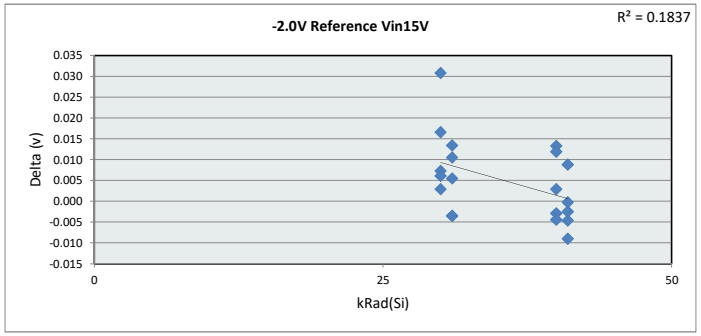
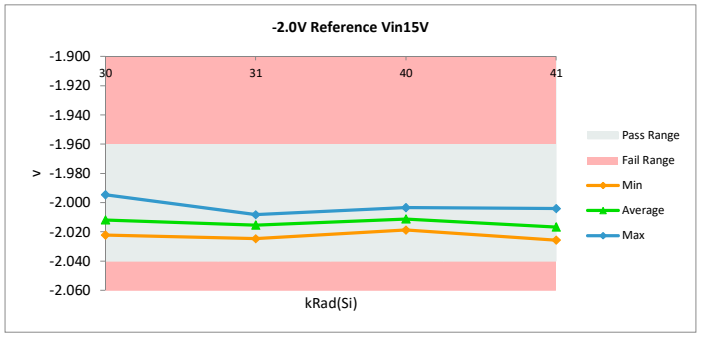
	-2.0V Reference Vin15V		
Test Site			
Tester			
Test Number			
Unit	V	v	
Max Limit	-1.96	-1.96	
Min Limit	-2.04	-2.04	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-2.030	-2.022	0.007
30	2	-2.027	-2.011	0.017
30	3	-2.016	-2.013	0.003
30	4	-2.026	-1.995	0.031
30	5	-2.025	-2.019	0.006
40	6	-2.006	-2.003	0.003
40	7	-2.027	-2.013	0.013
40	8	-2.016	-2.019	-0.003
40	9	-2.023	-2.011	0.012
40	10	-2.005	-2.009	-0.004
31	17	-2.015	-2.019	-0.003
31	18	-2.030	-2.025	0.006
31	19	-2.020	-2.010	0.010
31	20	-2.012	-2.015	-0.003
31	21	-2.022	-2.008	0.013
41	11	-2.023	-2.026	-0.003
41	12	-2.010	-2.015	-0.005
41	13	-2.015	-2.015	0.000
41	14	-2.013	-2.004	0.009
41	15	-2.015	-2.024	-0.009
	Max	-2.005	-1.995	0.031
	Average	-2.019	-2.014	0.005
	Min	-2.030	-2.026	-0.009
	Std Dev	0.008	0.008	0.009

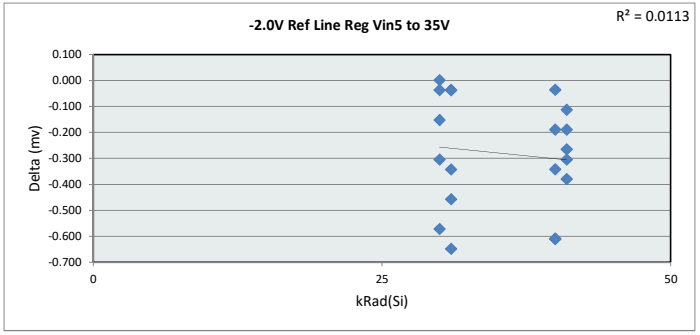


	-2.0V Reference Vin15V			
Test Site				
Tester				
Test Number				
Max Limit	-1.96	v		
Min Limit	-2.04	v		
kRad(Si)	30	31	40	41
LL	-2.040	-2.040	-2.040	-2.040
Min	-2.022	-2.025	-2.019	-2.026
Average	-2.012	-2.015	-2.011	-2.017
Max	-1.995	-2.008	-2.004	-2.004
UL	-1.960	-1.960	-1.960	-1.960

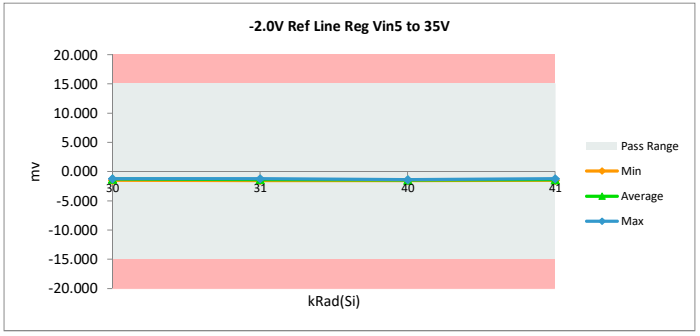


UC1834-SP TID Report

	-2.0V Ref Line Reg Vin5 to 35V		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	15	15	
Min Limit	-15	-15	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-1.222	-1.259	-0.037
30	2	-0.916	-1.221	-0.304
30	3	-1.069	-1.221	-0.152
30	4	-1.222	-1.221	0.001
30	5	-0.916	-1.488	-0.571
40	6	-1.260	-1.449	-0.189
40	7	-1.527	-1.563	-0.036
40	8	-0.802	-1.411	-0.609
40	9	-0.764	-1.373	-0.609
40	10	-1.069	-1.411	-0.342
31	17	-1.184	-1.221	-0.037
31	18	-0.764	-1.221	-0.457
31	19	-1.260	-1.297	-0.037
31	20	-1.184	-1.526	-0.342
31	21	-0.878	-1.526	-0.648
41	11	-1.069	-1.449	-0.380
41	12	-1.222	-1.411	-0.189
41	13	-1.222	-1.335	-0.113
41	14	-1.222	-1.487	-0.265
41	15	-0.916	-1.220	-0.304
	Max	-0.764	-1.220	0.001
	Average	-1.084	-1.365	-0.281
	Min	-1.527	-1.563	-0.648
	Std Dev	0.203	0.122	0.213

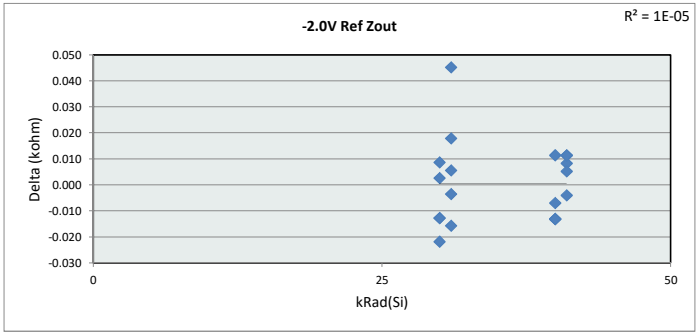


	-2.0V Ref Line Reg Vin5 to 35V			
Test Site				
Tester				
Test Number				
Max Limit	15	mv		
Min Limit	-15	mv		
kRad(Si)	30	31	40	41
LL	-15.000	-15.000	-15.000	-15.000
Min	-1.488	-1.526	-1.563	-1.487
Average	-1.282	-1.358	-1.441	-1.380
Max	-1.221	-1.221	-1.373	-1.220
UL	15.000	15.000	15.000	15.000

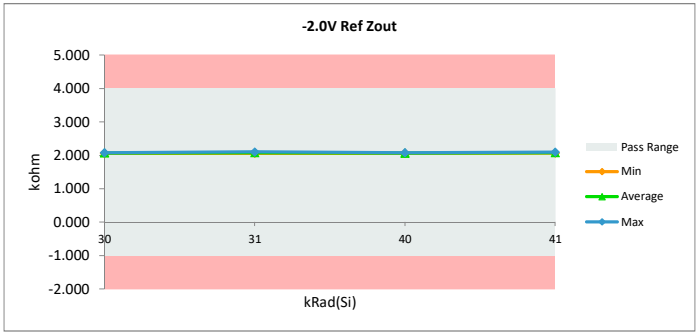


UC1834-SP TID Report

	-2.0V Ref Zout		
Test Site			
Tester			
Test Number			
Unit	kohm	kohm	
Max Limit	4	4	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	2.082	2.060	-0.022
30	2	2.085	2.073	-0.013
30	3	2.092	2.079	-0.013
30	4	2.064	2.067	0.003
30	5	2.067	2.076	0.009
40	6	2.079	2.066	-0.013
40	7	2.070	2.063	-0.007
40	8	2.067	2.078	0.011
40	9	2.076	2.063	-0.013
40	10	2.076	2.063	-0.013
31	17	2.064	2.060	-0.003
31	18	2.076	2.082	0.006
31	19	2.061	2.079	0.018
31	20	2.095	2.079	-0.016
31	21	2.058	2.103	0.045
41	11	2.073	2.069	-0.004
41	12	2.067	2.075	0.008
41	13	2.064	2.075	0.011
41	14	2.082	2.094	0.011
41	15	2.070	2.075	0.005
	Max	2.095	2.103	0.045
	Average	2.073	2.074	0.001
	Min	2.058	2.060	-0.022
	Std Dev	0.010	0.011	0.016

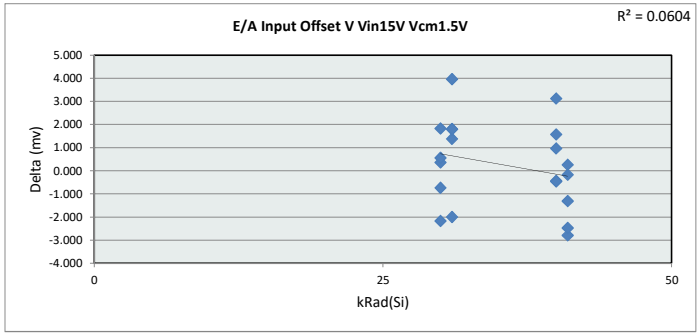


	-2.0V Ref Zout			
Test Site				
Tester				
Test Number				
Max Limit	4	kohm		
Min Limit	-1	kohm		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	2.061	2.061	2.063	2.069
Average	2.071	2.081	2.067	2.078
Max	2.079	2.103	2.078	2.094
UL	4.000	4.000	4.000	4.000

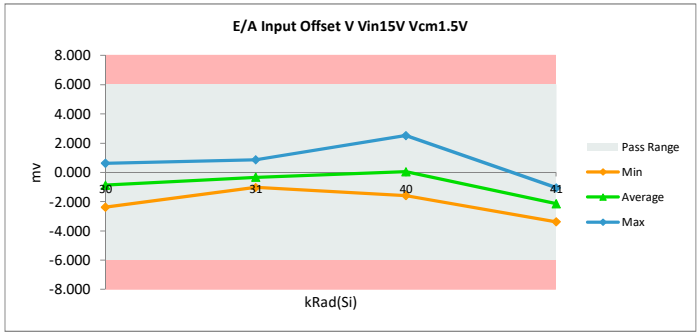


UC1834-SP TID Report

	E/A Input Offset V Vin15V Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	6	6	
Min Limit	-6	-6	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-1.184	-1.918	-0.734
30	2	0.268	0.625	0.358
30	3	-1.015	-0.458	0.557
30	4	-0.216	-2.387	-2.171
30	5	-2.048	-0.218	1.831
40	6	-1.124	-0.155	0.969
40	7	-0.611	2.516	3.127
40	8	-0.940	-1.372	-0.433
40	9	-1.115	-1.579	-0.464
40	10	-0.758	0.813	1.571
31	17	-4.640	-0.679	3.961
31	18	-1.473	-0.096	1.377
31	19	-0.938	0.864	1.802
31	20	-2.824	-1.026	1.798
31	21	1.273	-0.724	-1.997
41	11	-0.579	-3.375	-2.796
41	12	-0.371	-2.843	-2.472
41	13	-0.078	-1.383	-1.306
41	14	-0.880	-1.052	-0.172
41	15	-2.342	-2.082	0.260
	Max	1.273	2.516	3.961
	Average	-1.080	-0.826	0.253
	Min	-4.640	-3.375	-2.796
	Std Dev	1.229	1.403	1.851

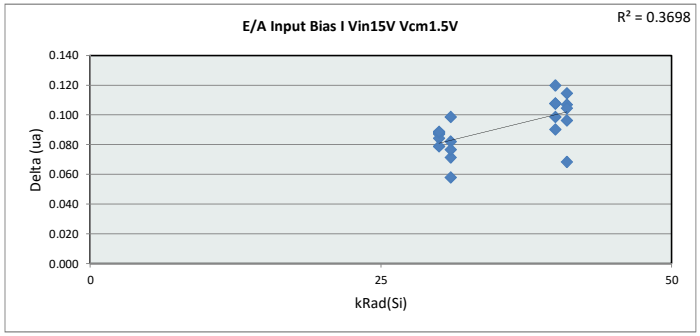


	E/A Input Offset V Vin15V Vcm			
Test Site				
Tester				
Test Number				
Max Limit	6	mv		
Min Limit	-6	mv		
kRad(Si)	30	31	40	41
LL	-6.000	-6.000	-6.000	-6.000
Min	-2.387	-1.026	-1.580	-3.375
Average	-0.871	-0.332	0.044	-2.147
Max	0.625	0.864	2.516	-1.052
UL	6.000	6.000	6.000	6.000

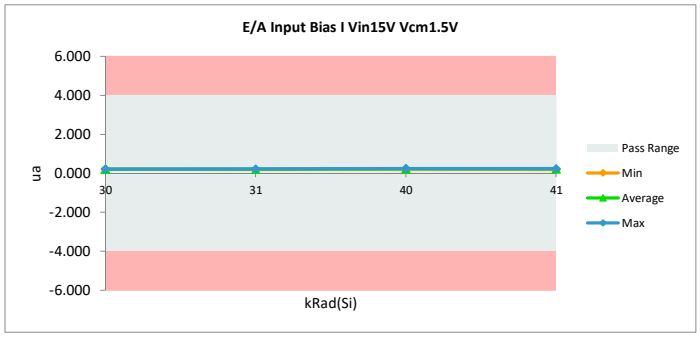


UC1834-SP TID Report

	E/A Input Bias I Vin15V Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	4	4	
Min Limit	-4	-4	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.132	0.219	0.087
30	2	0.128	0.213	0.084
30	3	0.130	0.218	0.088
30	4	0.133	0.212	0.079
30	5	0.130	0.219	0.089
40	6	0.121	0.229	0.108
40	7	0.130	0.220	0.090
40	8	0.132	0.231	0.099
40	9	0.130	0.238	0.108
40	10	0.128	0.248	0.120
31	17	0.128	0.210	0.082
31	18	0.126	0.225	0.099
31	19	0.126	0.198	0.071
31	20	0.126	0.203	0.077
31	21	0.132	0.190	0.058
41	11	0.128	0.196	0.068
41	12	0.131	0.245	0.114
41	13	0.126	0.233	0.107
41	14	0.128	0.224	0.096
41	15	0.128	0.233	0.105
	Max	0.133	0.248	0.120
	Average	0.129	0.220	0.091
	Min	0.121	0.190	0.058
	Std Dev	0.003	0.016	0.016

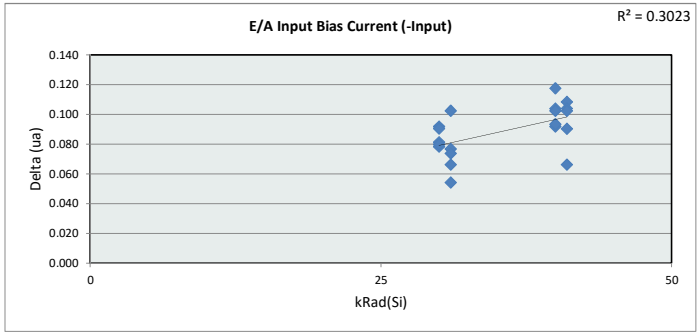


	E/A Input Bias I Vin15V Vcm1.			
Test Site				
Tester				
Test Number				
Max Limit	4	ua		
Min Limit	-4	ua		
kRad(Si)	30	31	40	41
LL	-4.000	-4.000	-4.000	-4.000
Min	0.212	0.190	0.220	0.196
Average	0.216	0.205	0.233	0.226
Max	0.219	0.225	0.248	0.245
UL	4.000	4.000	4.000	4.000

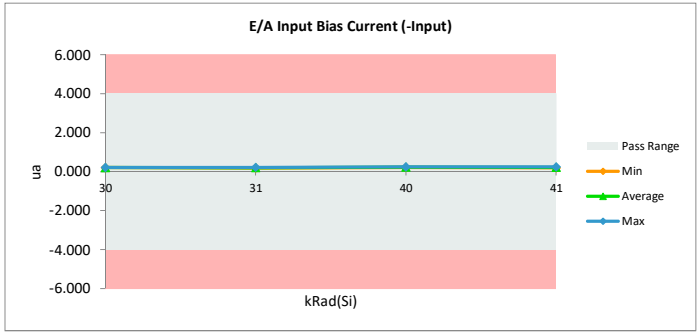


UC1834-SP TID Report

	E/A Input Bias Current (-Input)		
Test Site			
Tester			
Test Number			
Unit	mA	ua	
Max Limit	4	4	
Min Limit	-4	-4	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.132	0.213	0.081
30	2	0.130	0.208	0.078
30	3	0.124	0.216	0.092
30	4	0.128	0.208	0.080
30	5	0.127	0.217	0.090
40	6	0.124	0.228	0.104
40	7	0.127	0.219	0.092
40	8	0.136	0.229	0.093
40	9	0.128	0.231	0.102
40	10	0.127	0.244	0.117
31	17	0.128	0.205	0.077
31	18	0.118	0.220	0.102
31	19	0.130	0.196	0.066
31	20	0.124	0.198	0.074
31	21	0.134	0.189	0.054
41	11	0.128	0.195	0.066
41	12	0.133	0.241	0.108
41	13	0.125	0.229	0.104
41	14	0.128	0.219	0.090
41	15	0.130	0.232	0.102
	Max	0.136	0.244	0.117
	Average	0.128	0.217	0.089
	Min	0.118	0.189	0.054
	Std Dev	0.004	0.016	0.016

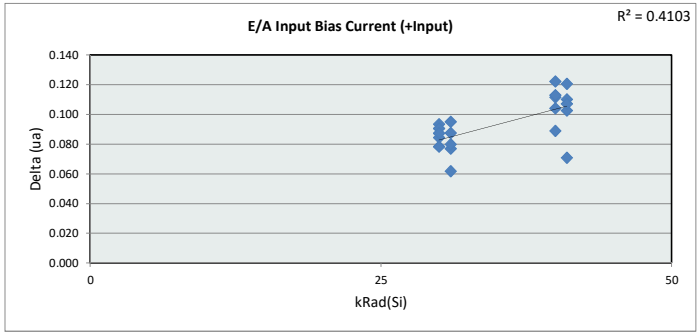


	E/A Input Bias Current (-Input			
Test Site				
Tester				
Test Number				
Max Limit	4	ua		
Min Limit	-4	ua		
kRad(Si)	30	31	40	41
LL	-4.000	-4.000	-4.000	-4.000
Min	0.208	0.189	0.219	0.195
Average	0.213	0.202	0.230	0.223
Max	0.217	0.220	0.244	0.241
UL	4.000	4.000	4.000	4.000

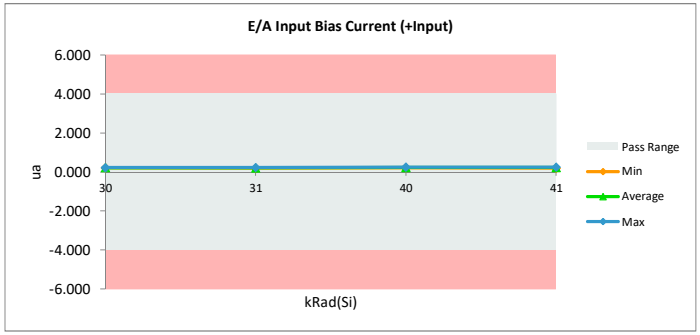


UC1834-SP TID Report

	E/A Input Bias Current (+Input)		
Test Site			
Tester			
Test Number			
Unit		ua	
Max Limit	4	4	
Min Limit	-4	-4	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.132	0.225	0.093
30	2	0.127	0.217	0.090
30	3	0.136	0.220	0.084
30	4	0.138	0.216	0.078
30	5	0.133	0.220	0.087
40	6	0.118	0.229	0.111
40	7	0.133	0.222	0.089
40	8	0.128	0.232	0.104
40	9	0.132	0.244	0.113
40	10	0.128	0.250	0.122
31	17	0.127	0.214	0.087
31	18	0.134	0.229	0.095
31	19	0.122	0.199	0.077
31	20	0.128	0.208	0.080
31	21	0.130	0.192	0.062
41	11	0.127	0.198	0.071
41	12	0.128	0.249	0.120
41	13	0.127	0.237	0.110
41	14	0.127	0.229	0.102
41	15	0.127	0.234	0.107
	Max	0.138	0.250	0.122
	Average	0.129	0.223	0.094
	Min	0.118	0.192	0.062
	Std Dev	0.005	0.016	0.017

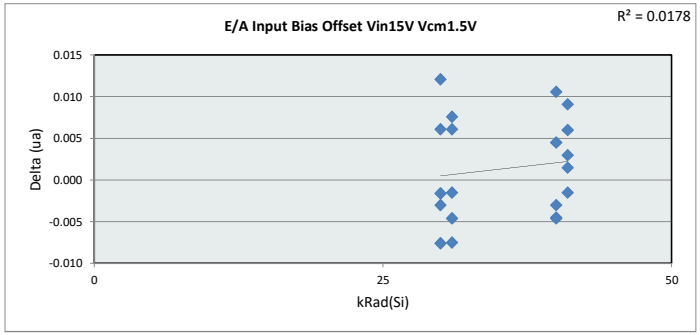


	E/A Input Bias Current (+Inpu			
Test Site				
Tester				
Test Number				
Max Limit	4	ua		
Min Limit	-4	ua		
kRad(Si)	30	31	40	41
LL	-4.000	-4.000	-4.000	-4.000
Min	0.216	0.192	0.222	0.198
Average	0.220	0.209	0.236	0.229
Max	0.225	0.229	0.251	0.249
UL	4.000	4.000	4.000	4.000

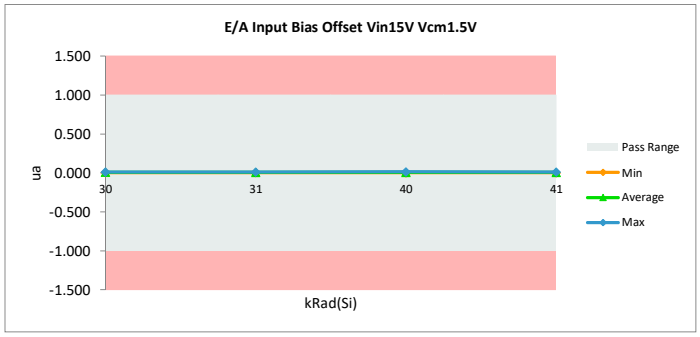


UC1834-SP TID Report

	E/A Input Bias Offset Vin15V Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	1	1	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.000	0.012	0.012
30	2	0.003	0.009	0.006
30	3	0.012	0.004	-0.008
30	4	0.009	0.007	-0.002
30	5	0.006	0.003	-0.003
40	6	0.006	0.002	-0.005
40	7	0.006	0.003	-0.003
40	8	0.008	0.003	-0.005
40	9	0.003	0.014	0.011
40	10	0.002	0.006	0.005
31	17	0.002	0.009	0.008
31	18	0.017	0.009	-0.007
31	19	0.008	0.003	-0.005
31	20	0.004	0.011	0.006
31	21	0.004	0.003	-0.001
41	11	0.002	0.003	0.002
41	12	0.004	0.007	0.003
41	13	0.002	0.007	0.006
41	14	0.002	0.011	0.009
41	15	0.003	0.002	-0.002
	Max	0.017	0.014	0.012
	Average	0.005	0.006	0.001
	Min	0.000	0.002	-0.008
	Std Dev	0.004	0.004	0.006

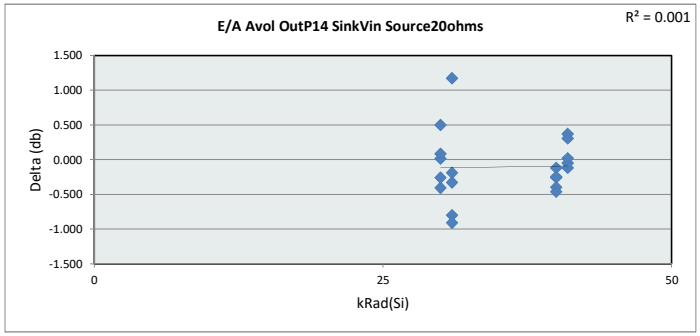


	E/A Input Bias Offset Vin15V V			
Test Site				
Tester				
Test Number				
Max Limit	1	ua		
Min Limit	-1	ua		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	0.003	0.003	0.002	0.002
Average	0.007	0.007	0.005	0.006
Max	0.012	0.011	0.014	0.011
UL	1.000	1.000	1.000	1.000

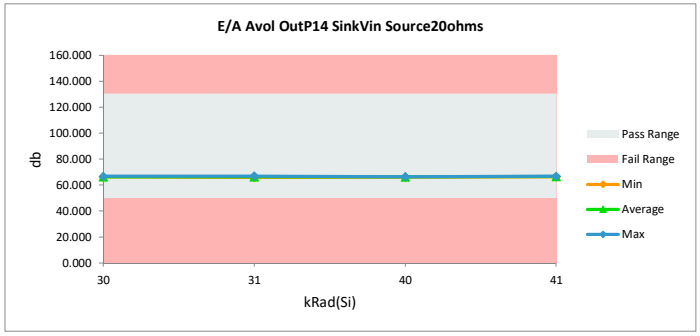


UC1834-SP TID Report

	E/A Avol OutP14 SinkVin Source20ohms		
Test Site			
Tester			
Test Number			
Unit	dB	db	
Max Limit	130	130	
Min Limit	50	50	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	66.243	66.741	0.498
30	2	66.516	66.256	-0.260
30	3	66.799	66.392	-0.407
30	4	66.310	66.324	0.014
30	5	66.447	66.530	0.083
40	6	66.586	66.330	-0.256
40	7	66.310	66.063	-0.247
40	8	66.586	66.467	-0.119
40	9	66.727	66.330	-0.397
40	10	66.656	66.195	-0.461
31	17	66.516	66.189	-0.327
31	18	66.727	65.926	-0.801
31	19	66.447	66.256	-0.191
31	20	67.165	66.256	-0.909
31	21	65.784	66.957	1.173
41	11	66.447	66.818	0.372
41	12	66.447	66.330	-0.117
41	13	66.378	66.330	-0.048
41	14	66.586	66.891	0.305
41	15	66.586	66.606	0.020
	Max	67.165	66.957	1.173
	Average	66.513	66.409	-0.104
	Min	65.784	65.926	-0.909
	Std Dev	0.268	0.273	0.460

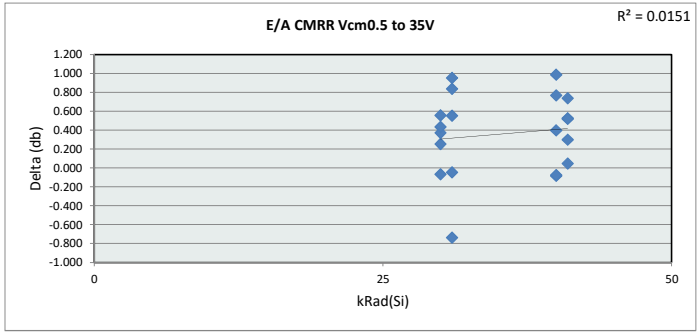


	E/A Avol OutP14 SinkVin Sourc			
Test Site				
Tester				
Test Number				
Max Limit	130	db		
Min Limit	50	db		
kRad(Si)	30	31	40	41
LL	50.000	50.000	50.000	50.000
Min	66.256	65.926	66.063	66.330
Average	66.448	66.317	66.277	66.595
Max	66.741	66.957	66.467	66.891
UL	130.000	130.000	130.000	130.000

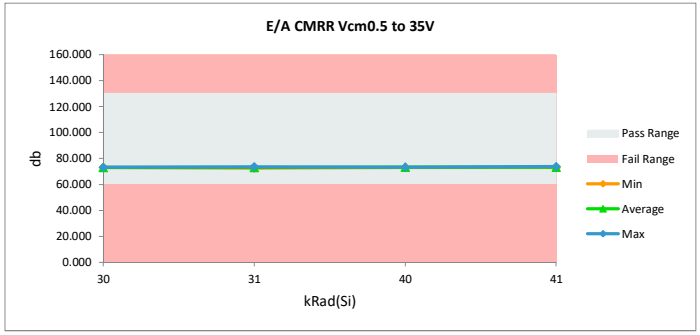


UC1834-SP TID Report

	E/A CMRR Vcm0.5 to 35V		
Test Site			
Tester			
Test Number			
Unit	dB	db	
Max Limit	130	130	
Min Limit	60	60	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	72.556	73.111	0.555
30	2	73.008	73.260	0.252
30	3	73.309	73.241	-0.068
30	4	72.672	73.044	0.372
30	5	72.628	73.062	0.434
40	6	72.970	73.367	0.397
40	7	72.413	73.399	0.986
40	8	72.599	73.367	0.767
40	9	73.122	73.038	-0.084
40	10	73.231	73.155	-0.076
31	17	72.420	72.971	0.551
31	18	72.716	72.668	-0.048
31	19	72.356	73.191	0.835
31	20	73.524	72.786	-0.738
31	21	72.672	73.624	0.951
41	11	72.556	73.081	0.525
41	12	72.556	73.075	0.519
41	13	72.753	73.050	0.297
41	14	73.046	73.781	0.736
41	15	72.962	73.008	0.046
	Max	73.524	73.781	0.986
	Average	72.804	73.164	0.360
	Min	72.356	72.668	-0.738
	Std Dev	0.325	0.258	0.427

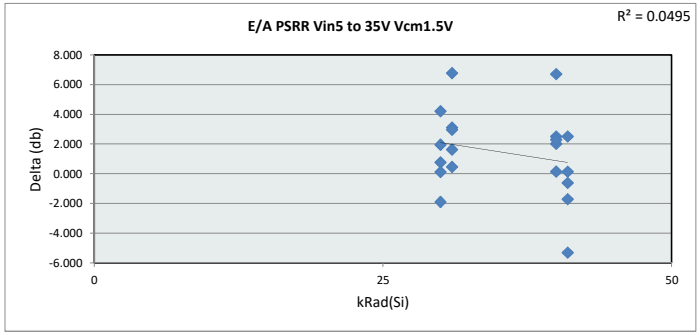


	E/A CMRR Vcm0.5 to 35V			
Test Site				
Tester				
Test Number				
Max Limit	130	db		
Min Limit	60	db		
kRad(Si)	30	31	40	41
LL	60.000	60.000	60.000	60.000
Min	73.044	72.668	73.038	73.008
Average	73.144	73.048	73.265	73.199
Max	73.260	73.624	73.399	73.781
UL	130.000	130.000	130.000	130.000

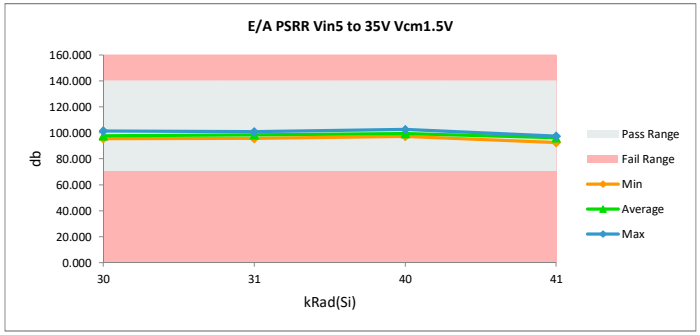


UC1834-SP TID Report

	E/A PSRR Vin5 to 35V Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	dB	db	
Max Limit	140	140	
Min Limit	70	70	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	95.844	97.798	1.954
30	2	97.255	101.456	4.201
30	3	96.639	97.400	0.761
30	4	97.647	95.752	-1.896
30	5	95.420	95.540	0.120
40	6	95.844	98.358	2.514
40	7	95.844	102.557	6.713
40	8	97.129	97.271	0.142
40	9	96.639	98.652	2.013
40	10	97.647	99.942	2.294
31	17	92.542	95.645	3.103
31	18	95.844	98.804	2.960
31	19	94.081	100.857	6.776
31	20	95.736	96.192	0.456
31	21	98.489	100.118	1.629
41	11	97.782	92.483	-5.299
41	12	97.384	96.774	-0.610
41	13	98.489	96.774	-1.714
41	14	95.016	97.530	2.514
41	15	96.880	97.019	0.139
	Max	98.489	102.557	6.776
	Average	96.408	97.846	1.439
	Min	92.542	92.483	-5.299
	Std Dev	1.471	2.355	2.809

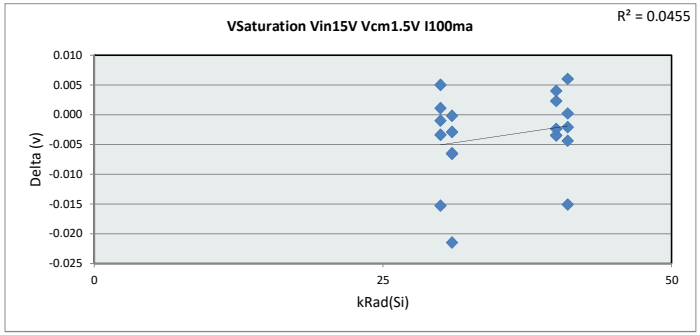


	E/A PSRR Vin5 to 35V Vcm1.5V			
Test Site				
Tester				
Test Number				
Max Limit	140	db		
Min Limit	70	db		
kRad(Si)	30	31	40	41
LL	70.000	70.000	70.000	70.000
Min	95.540	95.645	97.271	92.483
Average	97.589	98.323	99.356	96.116
Max	101.457	100.857	102.557	97.530
UL	140.000	140.000	140.000	140.000

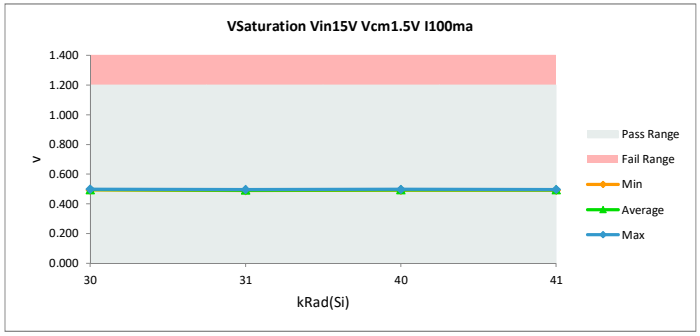


UC1834-SP TID Report

	VSaturation Vin15V Vcm1.5V I100ma		
Test Site			
Tester			
Test Number			
Unit	V	v	
Max Limit	1.2	1.2	
Min Limit	0	0	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.494	0.495	0.001
30	2	0.497	0.496	-0.001
30	3	0.497	0.494	-0.003
30	4	0.513	0.498	-0.015
30	5	0.492	0.497	0.005
40	6	0.496	0.498	0.002
40	7	0.499	0.495	-0.004
40	8	0.496	0.493	-0.003
40	9	0.488	0.492	0.004
40	10	0.498	0.496	-0.002
31	17	0.501	0.495	-0.007
31	18	0.496	0.493	-0.003
31	19	0.497	0.490	-0.007
31	20	0.512	0.490	-0.021
31	21	0.497	0.496	0.000
41	11	0.507	0.492	-0.015
41	12	0.495	0.491	-0.004
41	13	0.496	0.496	0.000
41	14	0.496	0.494	-0.002
41	15	0.491	0.497	0.006
	Max	0.513	0.498	0.006
	Average	0.498	0.494	-0.003
	Min	0.488	0.490	-0.021
	Std Dev	0.006	0.003	0.007

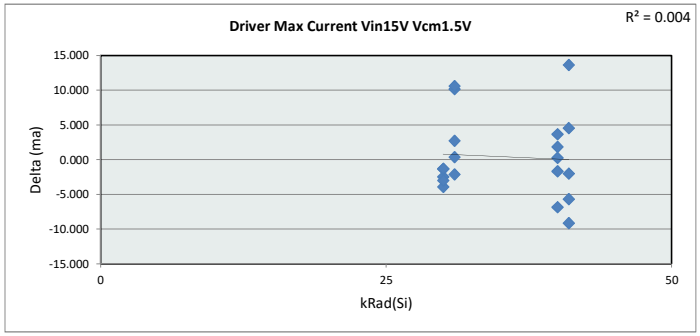


	VSaturation Vin15V Vcm1.5V I			
Test Site				
Tester				
Test Number				
Max Limit	1.2	v		
Min Limit	0	v		
kRad(Si)	30	31	40	41
LL	0.000	0.000	0.000	0.000
Min	0.494	0.490	0.492	0.491
Average	0.496	0.493	0.495	0.494
Max	0.498	0.496	0.498	0.497
UL	1.200	1.200	1.200	1.200

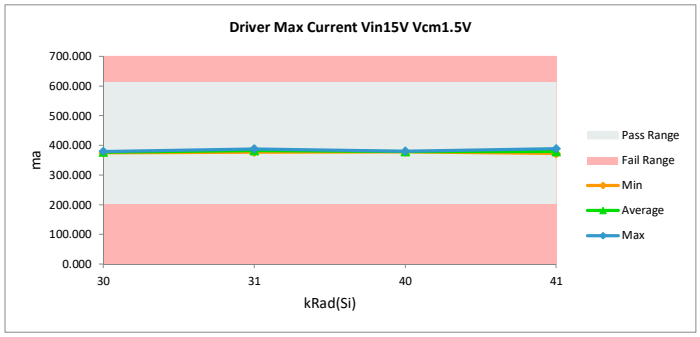


UC1834-SP TID Report

	Driver Max Current Vin15V Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	mA	ma	
Max Limit	610	610	
Min Limit	200	200	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	380.505	376.584	-3.921
30	2	378.263	375.778	-2.486
30	3	380.734	379.388	-1.346
30	4	377.653	374.643	-3.010
30	5	379.390	378.063	-1.326
40	6	379.427	377.745	-1.682
40	7	376.026	379.671	3.645
40	8	378.278	380.119	1.841
40	9	384.996	378.141	-6.855
40	10	379.075	379.343	0.268
31	17	373.301	383.466	10.165
31	18	376.823	377.194	0.371
31	19	377.209	387.795	10.586
31	20	386.175	384.059	-2.116
31	21	376.797	379.502	2.705
41	11	374.799	388.450	13.651
41	12	382.386	376.694	-5.693
41	13	379.380	377.365	-2.015
41	14	375.003	379.538	4.535
41	15	381.354	372.213	-9.141
	Max	386.175	388.450	13.651
	Average	378.879	379.287	0.409
	Min	373.301	372.213	-9.141
	Std Dev	3.249	4.031	5.857

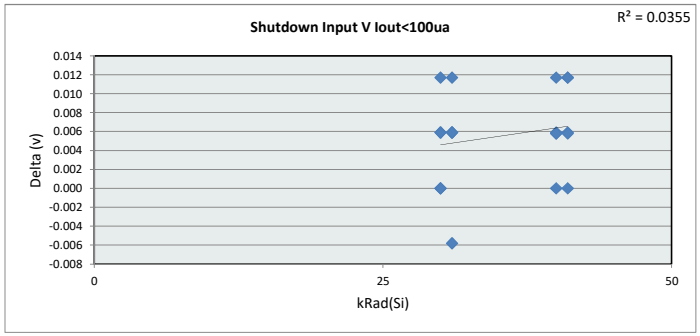


	Driver Max Current Vin15V Vcm			
Test Site				
Tester				
Test Number				
Max Limit	610	ma		
Min Limit	200	ma		
kRad(Si)	30	31	40	41
LL	200.000	200.000	200.000	200.000
Min	374.643	377.194	377.745	372.213
Average	376.891	382.403	379.004	378.852
Max	379.388	387.795	380.119	388.450
UL	610.000	610.000	610.000	610.000

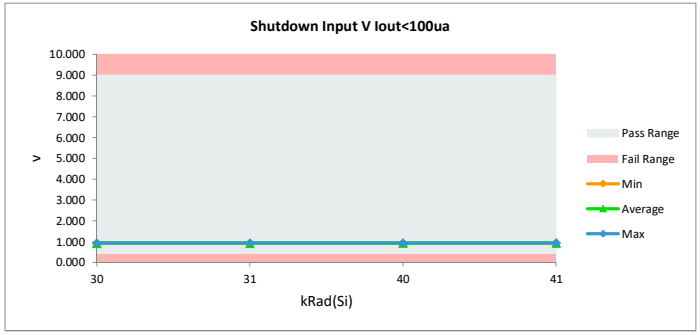


UC1834-SP TID Report

	Shutdown Input V Iout<100ua		
Test Site			
Tester			
Test Number			
Unit	V	v	
Max Limit	9	9	
Min Limit	0.4	0.4	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.917	0.929	0.012
30	2	0.923	0.923	0.000
30	3	0.923	0.923	0.000
30	4	0.917	0.923	0.006
30	5	0.917	0.923	0.006
40	6	0.923	0.923	0.000
40	7	0.917	0.923	0.006
40	8	0.917	0.929	0.012
40	9	0.923	0.929	0.006
40	10	0.923	0.929	0.006
31	17	0.917	0.923	0.006
31	18	0.917	0.923	0.006
31	19	0.917	0.929	0.012
31	20	0.929	0.923	-0.006
31	21	0.917	0.923	0.006
41	11	0.917	0.923	0.006
41	12	0.917	0.929	0.012
41	13	0.923	0.929	0.006
41	14	0.923	0.935	0.012
41	15	0.923	0.923	0.000
	Max	0.929	0.935	0.012
	Average	0.920	0.926	0.006
	Min	0.917	0.923	-0.006
	Std Dev	0.004	0.004	0.005

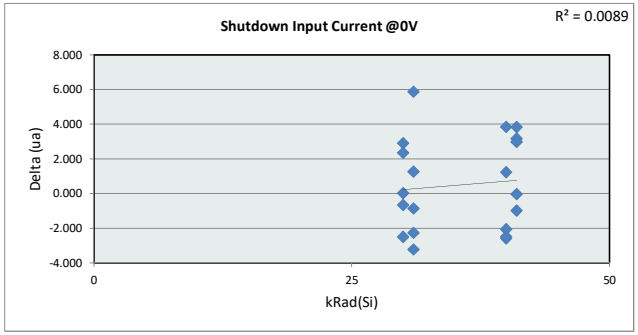


	Shutdown Input V Iout<100ua			
Test Site				
Tester				
Test Number				
Max Limit	9	v		
Min Limit	0.4	v		
kRad(Si)	30	31	40	41
LL	0.400	0.400	0.400	0.400
Min	0.923	0.923	0.923	0.923
Average	0.924	0.924	0.926	0.928
Max	0.929	0.929	0.929	0.935
UL	9.000	9.000	9.000	9.000

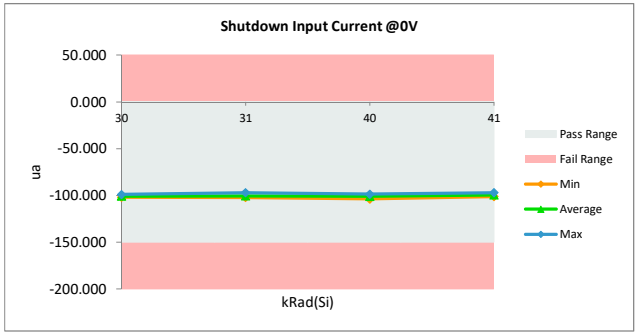


UC1834-SP TID Report

	Shutdown Input Current @0V		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	0	-0.0001	
Min Limit	-150	-150	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-101.347	-98.992	2.355
30	2	-100.899	-101.559	-0.660
30	3	-99.424	-101.918	-2.494
30	4	-102.682	-99.773	2.909
30	5	-101.556	-101.523	0.033
40	6	-98.379	-100.964	-2.585
40	7	-101.682	-103.735	-2.053
40	8	-102.454	-98.604	3.850
40	9	-101.689	-100.459	1.230
40	10	-98.679	-101.166	-2.487
31	17	-98.967	-102.196	-3.229
31	18	-101.099	-101.956	-0.857
31	19	-102.413	-101.142	1.271
31	20	-98.322	-100.581	-2.259
31	21	-102.891	-97.013	5.878
41	11	-101.121	-101.147	-0.026
41	12	-102.677	-99.508	3.169
41	13	-99.555	-100.538	-0.983
41	14	-100.911	-97.072	3.839
41	15	-101.596	-98.614	2.982
	Max	-98.322	-97.013	5.878
	Average	-100.917	-100.423	0.494
	Min	-102.891	-103.735	-3.229
	Std Dev	1.506	1.715	2.678

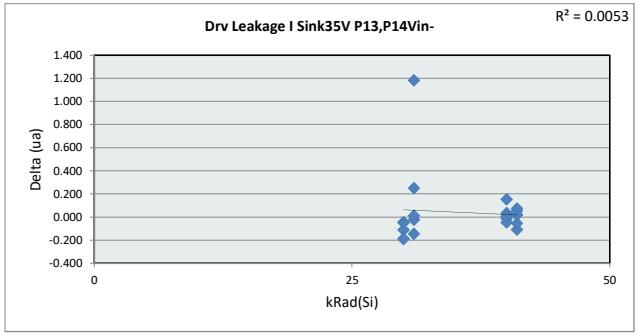


	Shutdown Input Current @0V			
Test Site				
Tester				
Test Number				
Max Limit	-0.0001	ua		
Min Limit	-150	ua		
kRad(Si)	30	31	40	41
LL	-150.000	-150.000	-150.000	-150.000
Min	-101.918	-102.196	-103.735	-101.147
Average	-100.753	-100.578	-100.986	-99.376
Max	-98.992	-97.013	-98.604	-97.072
UL	0.000	0.000	0.000	0.000

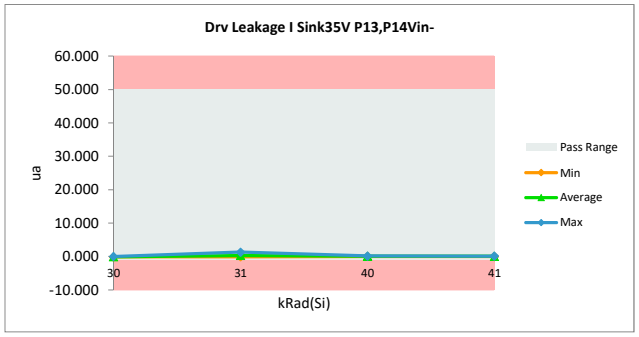


UC1834-SP TID Report

	Drv Leakage I Sink35V P13,P14Vin-		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	50	50	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.004	-0.040	-0.044
30	2	0.038	-0.072	-0.110
30	3	-0.010	-0.056	-0.047
30	4	0.029	-0.159	-0.187
30	5	0.099	-0.090	-0.190
40	6	0.042	0.029	-0.013
40	7	0.123	0.077	-0.046
40	8	0.080	0.114	0.034
40	9	-0.015	0.138	0.153
40	10	0.052	0.058	0.005
31	17	0.057	0.307	0.250
31	18	0.067	-0.079	-0.145
31	19	0.076	0.055	-0.022
31	20	-0.024	-0.011	0.013
31	21	0.114	1.295	1.182
41	11	0.090	-0.018	-0.109
41	12	0.040	-0.014	-0.054
41	13	0.014	0.068	0.054
41	14	0.029	0.048	0.019
41	15	0.037	0.110	0.073
	Max	0.123	1.295	1.182
	Average	0.047	0.088	0.041
	Min	-0.024	-0.159	-0.190
	Std Dev	0.042	0.302	0.289

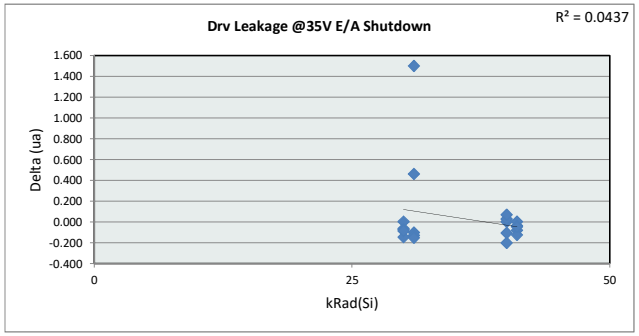


	Drv Leakage I Sink35V P13,P1			
Test Site				
Tester				
Test Number				
Max Limit	50	ua		
Min Limit	-1	ua		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	-0.159	-0.079	0.029	-0.018
Average	-0.084	0.313	0.083	0.039
Max	-0.040	1.295	0.138	0.110
UL	50.000	50.000	50.000	50.000

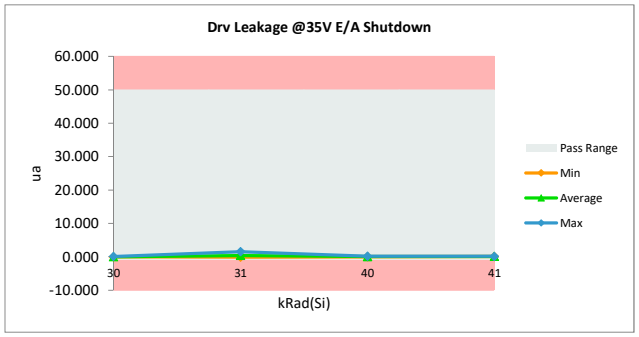


UC1834-SP TID Report

	Drv Leakage @35V E/A Shutdown		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	50	50	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.045	-0.019	-0.064
30	2	0.094	0.100	0.006
30	3	0.166	0.021	-0.145
30	4	0.045	-0.026	-0.071
30	5	0.082	0.000	-0.083
40	6	0.116	0.119	0.003
40	7	0.085	0.114	0.029
40	8	0.216	0.016	-0.199
40	9	0.154	0.050	-0.104
40	10	0.118	0.190	0.072
31	17	0.099	0.561	0.462
31	18	0.099	0.000	-0.099
31	19	0.118	-0.010	-0.128
31	20	0.073	-0.076	-0.149
31	21	0.037	1.537	1.500
41	11	0.082	0.088	0.005
41	12	0.197	0.119	-0.078
41	13	0.227	0.105	-0.123
41	14	0.175	0.140	-0.035
41	15	0.094	0.050	-0.044
	Max	0.227	1.537	1.500
	Average	0.116	0.154	0.038
	Min	0.037	-0.076	-0.199
	Std Dev	0.056	0.351	0.370

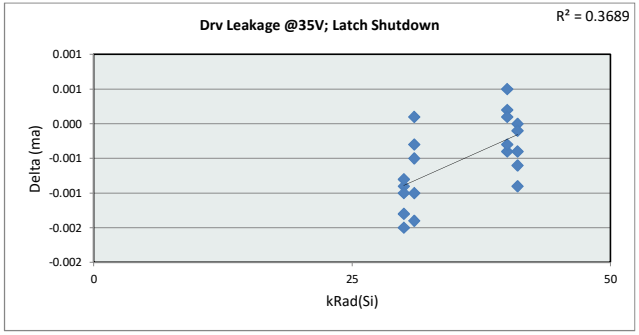


	Drv Leakage @35V E/A Shutdo			
Test Site				
Tester				
Test Number				
Max Limit	50	ua		
Min Limit	-1	ua		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	-0.027	-0.076	0.017	0.050
Average	0.015	0.402	0.098	0.100
Max	0.100	1.537	0.190	0.140
UL	50.000	50.000	50.000	50.000

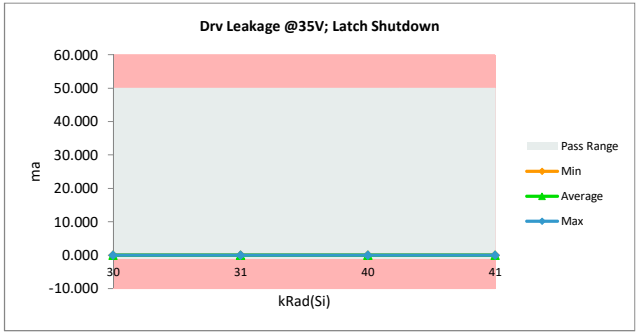


UC1834-SP TID Report

	Drv Leakage @35V; Latch Shutdown		
Test Site			
Tester			
Test Number			
Unit	mA	ma	
Max Limit	50	50	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.001	-0.001	-0.001
30	2	0.001	0.000	-0.001
30	3	0.001	-0.001	-0.001
30	4	0.001	0.000	-0.001
30	5	0.000	0.000	-0.001
40	6	0.000	0.001	0.000
40	7	0.000	0.000	0.000
40	8	0.000	0.001	0.000
40	9	0.001	0.001	0.000
40	10	0.001	0.000	0.000
31	17	0.000	0.000	0.000
31	18	0.000	-0.001	-0.001
31	19	0.000	-0.001	-0.001
31	20	0.000	-0.001	0.000
31	21	0.001	0.001	0.000
41	11	-0.001	-0.001	0.000
41	12	0.000	-0.001	-0.001
41	13	0.000	0.000	0.000
41	14	0.000	0.000	0.000
41	15	0.001	0.000	-0.001
	Max	0.001	0.001	0.000
	Average	0.000	0.000	-0.001
	Min	-0.001	-0.001	-0.001
	Std Dev	0.000	0.001	0.001

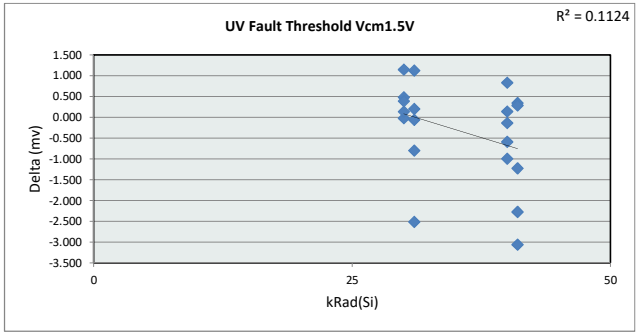


	Drv Leakage @35V; Latch Shut			
Test Site				
Tester				
Test Number				
Max Limit	50	ma		
Min Limit	-1	ma		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	-0.001	-0.001	0.000	-0.001
Average	0.000	0.000	0.001	0.000
Max	0.000	0.001	0.001	0.000
UL	50.000	50.000	50.000	50.000

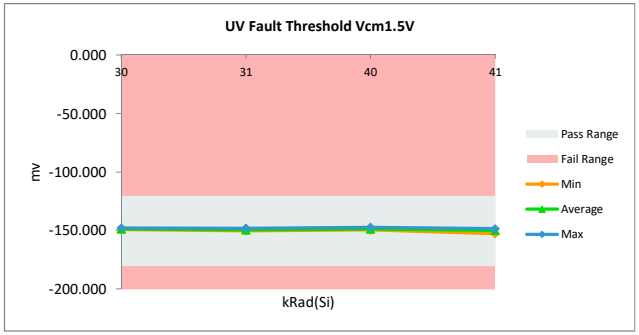


UC1834-SP TID Report

	UV Fault Threshold Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	-120	-120	
Min Limit	-180	-180	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-148.248	-147.769	0.479
30	2	-149.327	-149.350	-0.023
30	3	-148.844	-148.710	0.134
30	4	-149.442	-148.297	1.145
30	5	-149.266	-148.880	0.386
40	6	-147.841	-147.978	-0.137
40	7	-148.413	-149.002	-0.589
40	8	-149.304	-149.167	0.137
40	9	-148.221	-147.391	0.830
40	10	-148.604	-149.601	-0.997
31	17	-147.827	-150.341	-2.514
31	18	-149.425	-150.229	-0.804
31	19	-149.277	-148.154	1.123
31	20	-149.382	-149.183	0.199
31	21	-149.849	-149.911	-0.062
41	11	-149.588	-152.651	-3.063
41	12	-148.512	-149.740	-1.228
41	13	-147.599	-149.874	-2.275
41	14	-148.746	-148.406	0.340
41	15	-149.526	-149.243	0.283
	Max	-147.599	-147.391	1.145
	Average	-148.862	-149.194	-0.332
	Min	-149.849	-152.651	-3.063
	Std Dev	0.669	1.157	1.172

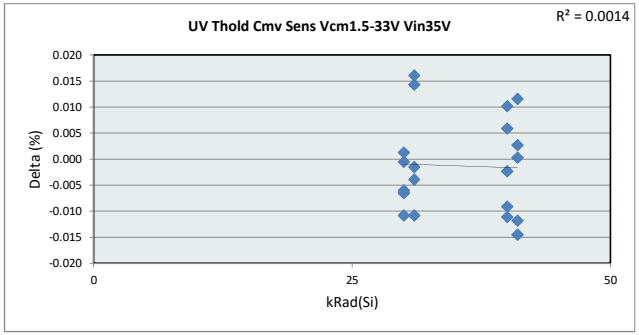


	UV Fault Threshold Vcm1.5V			
Test Site				
Tester				
Test Number				
Max Limit	-120	mv		
Min Limit	-180	mv		
kRad(Si)	30	31	40	41
LL	-180.000	-180.000	-180.000	-180.000
Min	-149.350	-150.341	-149.601	-152.651
Average	-148.601	-149.564	-148.628	-149.983
Max	-147.769	-148.154	-147.391	-148.406
UL	-120.000	-120.000	-120.000	-120.000

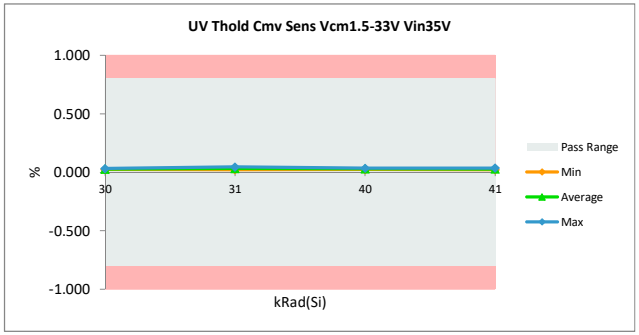


UC1834-SP TID Report

	UV Thold Cmv Sens Vcm1.5-33V Vin35V		
Test Site			
Tester			
Test Number			
Unit	%	%	
Max Limit	0.8	0.8	
Min Limit	-0.8	-0.8	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.031	0.024	-0.007
30	2	0.035	0.029	-0.006
30	3	0.034	0.033	0.000
30	4	0.026	0.027	0.001
30	5	0.040	0.029	-0.011
40	6	0.032	0.029	-0.002
40	7	0.026	0.036	0.010
40	8	0.028	0.034	0.006
40	9	0.041	0.032	-0.009
40	10	0.036	0.025	-0.011
31	17	0.025	0.023	-0.001
31	18	0.029	0.025	-0.004
31	19	0.026	0.040	0.014
31	20	0.043	0.032	-0.011
31	21	0.030	0.046	0.016
41	11	0.024	0.036	0.012
41	12	0.027	0.027	0.000
41	13	0.034	0.022	-0.012
41	14	0.034	0.037	0.003
41	15	0.037	0.022	-0.014
	Max	0.043	0.046	0.016
	Average	0.032	0.030	-0.001
	Min	0.024	0.022	-0.014
	Std Dev	0.006	0.006	0.009

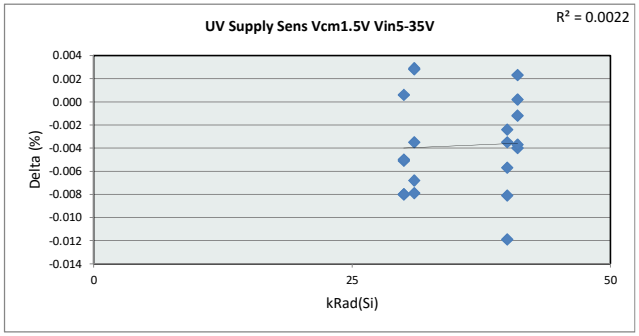


	UV Thold Cmv Sens Vcm1.5-33			
Test Site				
Tester				
Test Number				
Max Limit	0.8	%		
Min Limit	-0.8	%		
kRad(Si)	30	31	40	41
LL	-0.800	-0.800	-0.800	-0.800
Min	0.024	0.023	0.025	0.022
Average	0.028	0.033	0.031	0.029
Max	0.033	0.046	0.036	0.037
UL	0.800	0.800	0.800	0.800

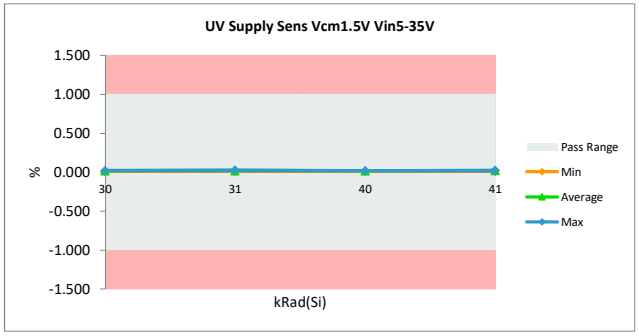


UC1834-SP TID Report

	UV Supply Sens Vcm1.5V Vin5-35V		
Test Site			
Tester			
Test Number			
Unit	%	%	
Max Limit	1	1	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.024	0.019	-0.005
30	2	0.019	0.019	0.001
30	3	0.024	0.016	-0.008
30	4	0.027	0.022	-0.005
30	5	0.027	0.019	-0.008
40	6	0.022	0.019	-0.003
40	7	0.023	0.021	-0.002
40	8	0.030	0.018	-0.012
40	9	0.023	0.017	-0.006
40	10	0.024	0.016	-0.008
31	17	0.026	0.029	0.003
31	18	0.024	0.021	-0.003
31	19	0.029	0.021	-0.008
31	20	0.016	0.019	0.003
31	21	0.025	0.018	-0.007
41	11	0.028	0.024	-0.004
41	12	0.029	0.025	-0.004
41	13	0.022	0.022	0.000
41	14	0.026	0.024	-0.001
41	15	0.019	0.021	0.002
	Max	0.030	0.029	0.003
	Average	0.024	0.021	-0.004
	Min	0.016	0.016	-0.012
	Std Dev	0.004	0.003	0.004

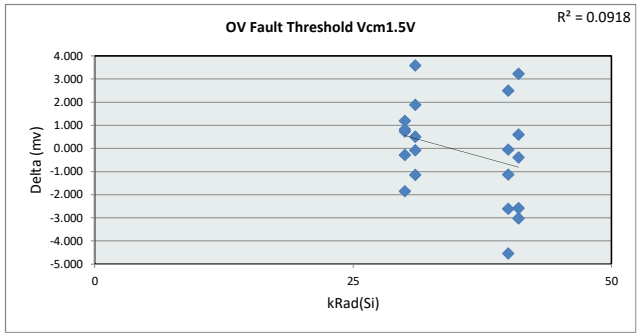


	UV Supply Sens Vcm1.5V Vin5-			
Test Site				
Tester				
Test Number				
Max Limit	1	%		
Min Limit	-1	%		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	0.017	0.018	0.016	0.021
Average	0.019	0.022	0.018	0.023
Max	0.022	0.029	0.021	0.025
UL	1.000	1.000	1.000	1.000

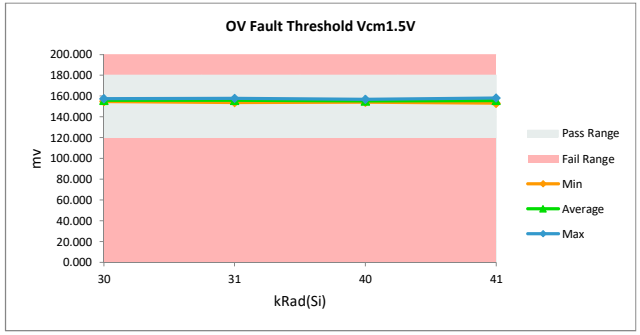


UC1834-SP TID Report

	OV Fault Threshold Vcm1.5V		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	180	180	
Min Limit	120	120	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	155.577	156.307	0.731
30	2	156.979	155.132	-1.848
30	3	154.686	155.881	1.195
30	4	155.173	154.890	-0.282
30	5	156.651	157.470	0.818
40	6	155.328	155.276	-0.052
40	7	154.514	157.011	2.496
40	8	156.337	155.209	-1.127
40	9	159.571	155.035	-4.536
40	10	156.721	154.107	-2.614
31	17	154.915	153.769	-1.146
31	18	154.355	157.943	3.588
31	19	156.041	157.927	1.886
31	20	155.350	155.271	-0.079
31	21	155.068	155.576	0.509
41	11	156.165	155.772	-0.393
41	12	155.017	158.247	3.230
41	13	156.187	156.788	0.601
41	14	156.111	153.090	-3.021
41	15	157.615	155.038	-2.577
	Max	159.571	158.247	3.588
	Average	155.918	155.787	-0.131
	Min	154.355	153.090	-4.536
	Std Dev	1.229	1.420	2.120

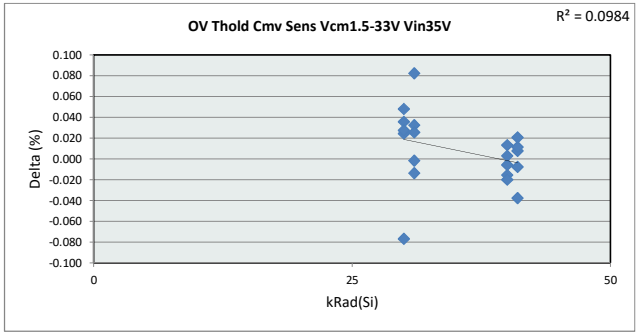


	OV Fault Threshold Vcm1.5V			
Test Site				
Tester				
Test Number				
Max Limit	180	mv		
Min Limit	120	mv		
kRad(Si)	30	31	40	41
LL	120.000	120.000	120.000	120.000
Min	154.890	153.769	154.107	153.090
Average	155.936	156.097	155.328	155.787
Max	157.470	157.943	157.011	158.247
UL	180.000	180.000	180.000	180.000

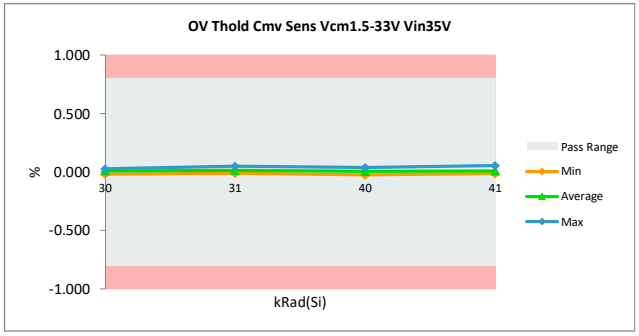


UC1834-SP TID Report

	OV Thold Cmv Sens Vcm1.5-33V Vin35V		
Test Site			
Tester			
Test Number			
Unit	%	%	
Max Limit	0.8	0.8	
Min Limit	-0.8	-0.8	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.058	-0.019	-0.077
30	2	-0.010	0.014	0.024
30	3	-0.025	0.023	0.048
30	4	-0.009	0.027	0.035
30	5	-0.027	0.000	0.027
40	6	0.008	-0.008	-0.016
40	7	-0.005	-0.025	-0.020
40	8	0.025	0.038	0.013
40	9	0.038	0.033	-0.006
40	10	-0.014	-0.011	0.003
31	17	-0.009	-0.011	-0.002
31	18	-0.032	0.000	0.032
31	19	-0.033	0.049	0.082
31	20	-0.009	0.017	0.025
31	21	0.024	0.011	-0.014
41	11	-0.008	0.000	0.008
41	12	0.008	0.000	-0.008
41	13	-0.006	0.006	0.011
41	14	0.033	0.054	0.021
41	15	0.024	-0.014	-0.038
	Max	0.058	0.054	0.082
	Average	0.002	0.009	0.008
	Min	-0.033	-0.025	-0.077
	Std Dev	0.025	0.022	0.033

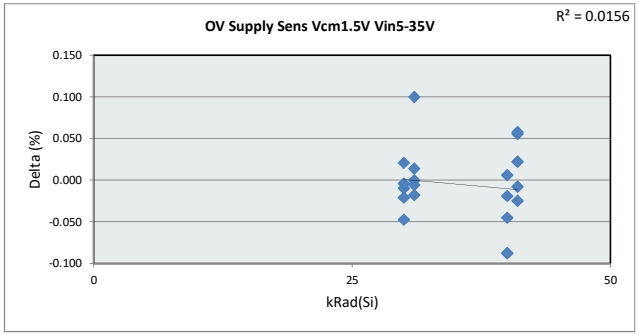


	OV Thold Cmv Sens Vcm1.5-33			
Test Site				
Tester				
Test Number				
Max Limit	0.8	%		
Min Limit	-0.8	%		
kRad(Si)	30	31	40	41
LL	-0.800	-0.800	-0.800	-0.800
Min	-0.019	-0.011	-0.025	-0.014
Average	0.009	0.013	0.005	0.009
Max	0.027	0.049	0.038	0.054
UL	0.800	0.800	0.800	0.800

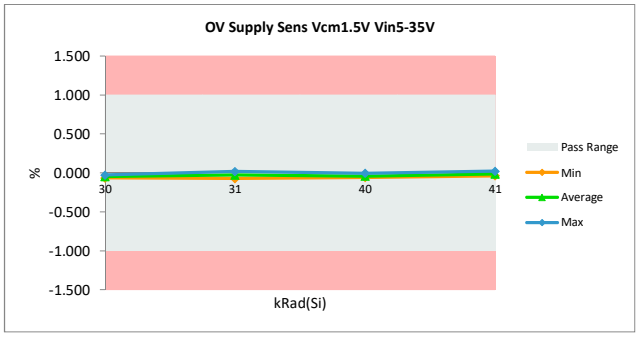


UC1834-SP TID Report

	OV Supply Sens Vcm1.5V Vin5-35V		
Test Site			
Tester			
Test Number			
Unit	%	%	
Max Limit	1	1	
Min Limit	-1	-1	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-0.018	-0.039	-0.021
30	2	-0.074	-0.054	0.021
30	3	-0.018	-0.065	-0.048
30	4	-0.035	-0.045	-0.010
30	5	-0.024	-0.028	-0.004
40	6	-0.004	-0.050	-0.045
40	7	0.038	-0.050	-0.088
40	8	-0.027	-0.046	-0.019
40	9	0.029	-0.058	-0.088
40	10	-0.010	-0.004	0.006
31	17	-0.053	-0.053	0.000
31	18	-0.066	-0.072	-0.006
31	19	-0.082	0.018	0.100
31	20	-0.029	-0.015	0.014
31	21	0.000	-0.018	-0.018
41	11	-0.012	-0.037	-0.025
41	12	-0.086	-0.028	0.058
41	13	-0.015	-0.023	-0.008
41	14	-0.001	0.022	0.022
41	15	-0.060	-0.004	0.055
	Max	0.038	0.022	0.100
	Average	-0.027	-0.032	-0.005
	Min	-0.086	-0.072	-0.088
	Std Dev	0.034	0.026	0.045

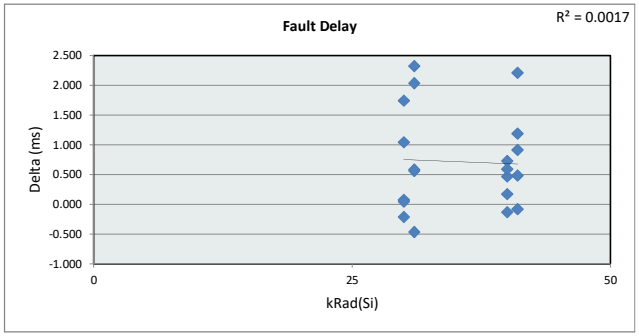


	OV Supply Sens Vcm1.5V Vin5-			
Test Site				
Tester				
Test Number				
Max Limit	1	%		
Min Limit	-1	%		
kRad(Si)	30	31	40	41
LL	-1.000	-1.000	-1.000	-1.000
Min	-0.065	-0.072	-0.059	-0.037
Average	-0.046	-0.028	-0.042	-0.014
Max	-0.028	0.018	-0.004	0.022
UL	1.000	1.000	1.000	1.000

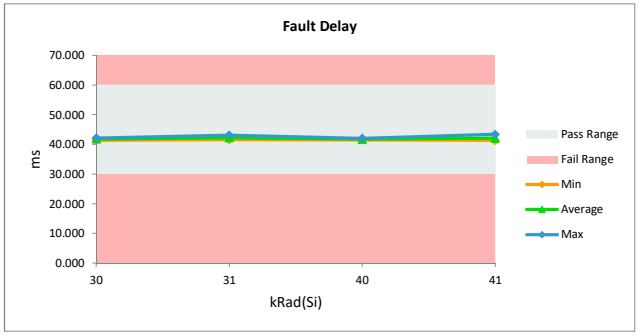


UC1834-SP TID Report

	Fault Delay		
Test Site			
Tester			
Test Number			
Unit	mS	ms	
Max Limit	60	60	
Min Limit	30	30	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	41.322	41.395	0.073
30	2	41.678	41.723	0.045
30	3	41.949	41.735	-0.214
30	4	41.075	42.118	1.042
30	5	40.414	42.154	1.740
40	6	41.552	42.017	0.466
40	7	41.284	41.453	0.169
40	8	41.338	42.066	0.728
40	9	41.305	41.895	0.590
40	10	41.698	41.564	-0.134
31	17	40.631	42.665	2.034
31	18	41.171	41.731	0.560
31	19	41.011	41.593	0.582
31	20	42.421	41.954	-0.467
31	21	40.804	43.125	2.321
41	11	40.707	41.892	1.185
41	12	41.264	41.746	0.482
41	13	41.210	42.123	0.913
41	14	41.153	43.361	2.208
41	15	41.444	41.361	-0.083
	Max	42.421	43.361	2.321
	Average	41.272	41.984	0.712
	Min	40.414	41.361	-0.467
	Std Dev	0.462	0.531	0.825

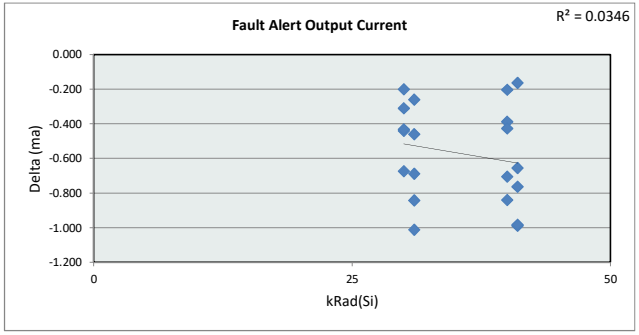


	Fault Delay			
Test Site				
Tester				
Test Number				
Max Limit	60	ms		
Min Limit	30	ms		
kRad(Si)	30	31	40	41
LL	30.000	30.000	30.000	30.000
Min	41.395	41.593	41.453	41.361
Average	41.825	42.214	41.799	42.097
Max	42.154	43.125	42.066	43.361
UL	60.000	60.000	60.000	60.000

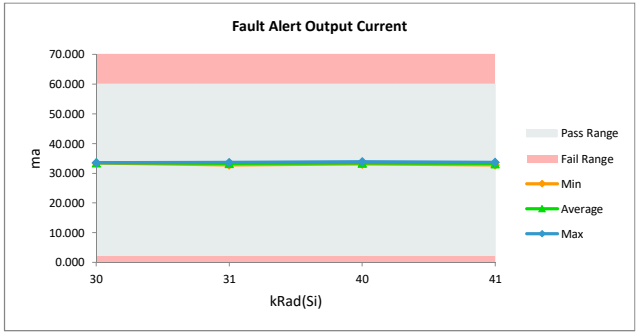


UC1834-SP TID Report

	Fault Alert Output Current		
Test Site			
Tester			
Test Number			
Unit	mA	ma	
Max Limit	60	60	
Min Limit	2	2	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	33.809	33.607	-0.201
30	2	34.271	33.598	-0.674
30	3	33.862	33.422	-0.441
30	4	33.861	33.551	-0.310
30	5	34.014	33.581	-0.433
40	6	33.789	33.084	-0.705
40	7	33.932	33.092	-0.840
40	8	34.047	33.659	-0.388
40	9	34.343	33.917	-0.426
40	10	33.799	33.595	-0.204
31	17	33.866	33.605	-0.261
31	18	34.176	33.333	-0.843
31	19	33.961	33.273	-0.688
31	20	34.086	33.626	-0.460
31	21	33.847	32.835	-1.012
41	11	33.650	32.887	-0.763
41	12	34.269	33.614	-0.655
41	13	33.881	33.717	-0.165
41	14	33.821	32.832	-0.988
41	15	34.412	33.429	-0.983
	Max	34.412	33.917	-0.165
	Average	33.985	33.413	-0.572
	Min	33.650	32.832	-1.012
	Std Dev	0.211	0.314	0.279

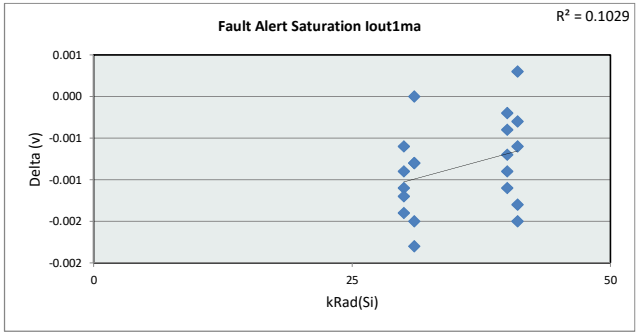


	Fault Alert Output Current			
Test Site				
Tester				
Test Number				
Max Limit	60	ma		
Min Limit	2	ma		
kRad(Si)	30	31	40	41
LL	2.000	2.000	2.000	2.000
Min	33.422	32.835	33.084	32.832
Average	33.552	33.334	33.470	33.296
Max	33.608	33.626	33.917	33.717
UL	60.000	60.000	60.000	60.000

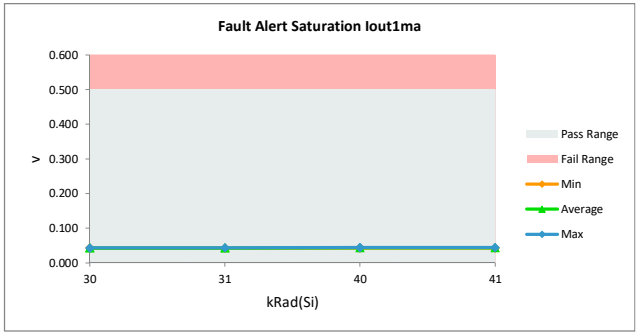


UC1834-SP TID Report

	Fault Alert Saturation Iout1ma		
Test Site			
Tester			
Test Number			
Unit	V	v	
Max Limit	0.5	0.5	
Min Limit	0	0	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.044	0.043	-0.001
30	2	0.043	0.043	-0.001
30	3	0.044	0.043	-0.001
30	4	0.044	0.043	-0.001
30	5	0.044	0.043	-0.001
40	6	0.044	0.044	0.000
40	7	0.044	0.044	0.000
40	8	0.044	0.043	-0.001
40	9	0.044	0.043	-0.001
40	10	0.044	0.043	-0.001
31	17	0.044	0.043	-0.001
31	18	0.044	0.043	-0.001
31	19	0.044	0.044	0.000
31	20	0.044	0.043	-0.001
31	21	0.044	0.042	-0.002
41	11	0.045	0.044	0.000
41	12	0.044	0.043	-0.001
41	13	0.044	0.043	-0.001
41	14	0.044	0.043	-0.002
41	15	0.043	0.044	0.000
	Max	0.045	0.044	0.000
	Average	0.044	0.043	-0.001
	Min	0.043	0.042	-0.002
	Std Dev	0.000	0.000	0.001

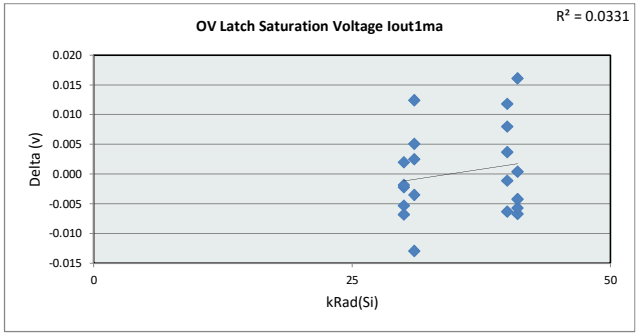


	Fault Alert Saturation Iout1ma			
Test Site				
Tester				
Test Number				
Max Limit	0.5	v		
Min Limit	0	v		
kRad(Si)	30	31	40	41
LL	0.000	0.000	0.000	0.000
Min	0.043	0.042	0.043	0.043
Average	0.043	0.043	0.044	0.043
Max	0.043	0.044	0.044	0.044
UL	0.500	0.500	0.500	0.500

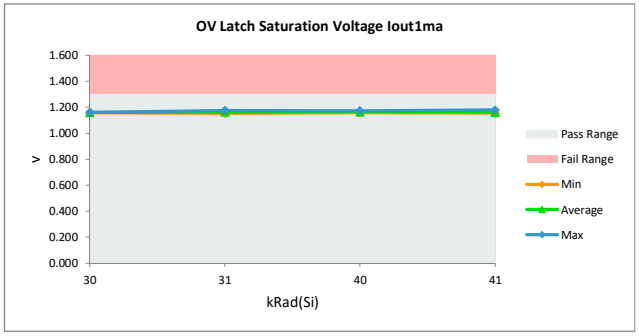


UC1834-SP TID Report

	OV Latch Saturation Voltage Iout1ma		
Test Site			
Tester			
Test Number			
Unit	V	v	
Max Limit	1.3	1.3	
Min Limit	0	0	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	1.166	1.160	-0.005
30	2	1.158	1.160	0.002
30	3	1.162	1.159	-0.002
30	4	1.165	1.158	-0.007
30	5	1.162	1.160	-0.002
40	6	1.159	1.171	0.012
40	7	1.165	1.173	0.008
40	8	1.165	1.159	-0.006
40	9	1.156	1.160	0.004
40	10	1.159	1.158	-0.001
31	17	1.166	1.171	0.005
31	18	1.160	1.156	-0.003
31	19	1.163	1.176	0.012
31	20	1.159	1.162	0.003
31	21	1.167	1.154	-0.013
41	11	1.163	1.179	0.016
41	12	1.164	1.157	-0.007
41	13	1.165	1.159	-0.006
41	14	1.158	1.154	-0.004
41	15	1.159	1.160	0.000
	Max	1.167	1.179	0.016
	Average	1.162	1.162	0.000
	Min	1.156	1.154	-0.013
	Std Dev	0.003	0.007	0.007

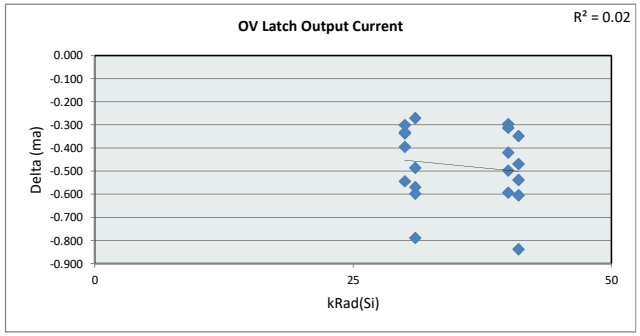


	OV Latch Saturation Voltage Io			
Test Site				
Tester				
Test Number				
Max Limit	1.3	v		
Min Limit	0	v		
kRad(Si)	30	31	40	41
LL	0.000	0.000	0.000	0.000
Min	1.158	1.154	1.158	1.154
Average	1.160	1.164	1.164	1.162
Max	1.160	1.176	1.173	1.179
UL	1.300	1.300	1.300	1.300

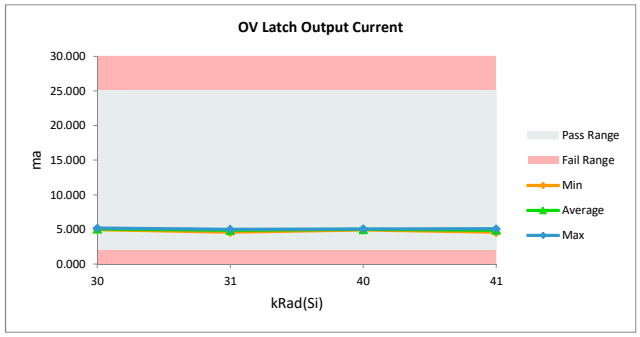


UC1834-SP TID Report

	OV Latch Output Current		
Test Site			
Tester			
Test Number			
Unit	mA	ma	
Max Limit	25	25	
Min Limit	2	2	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	5.496	5.195	-0.301
30	2	5.385	5.048	-0.337
30	3	5.309	4.978	-0.332
30	4	5.541	4.997	-0.544
30	5	5.497	5.102	-0.395
40	6	5.370	5.074	-0.297
40	7	5.535	5.037	-0.497
40	8	5.515	4.923	-0.592
40	9	5.382	4.962	-0.420
40	10	5.351	5.038	-0.313
31	17	5.473	4.904	-0.569
31	18	5.491	5.005	-0.486
31	19	5.536	4.939	-0.597
31	20	5.263	4.992	-0.271
31	21	5.367	4.579	-0.788
41	11	5.515	4.911	-0.604
41	12	5.461	4.924	-0.537
41	13	5.443	4.974	-0.469
41	14	5.414	4.577	-0.837
41	15	5.430	5.082	-0.348
	Max	5.541	5.195	-0.271
	Average	5.439	4.962	-0.477
	Min	5.263	4.577	-0.837
	Std Dev	0.081	0.150	0.160

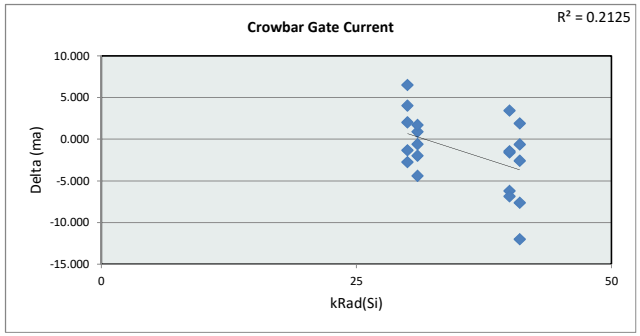


	OV Latch Output Current			
Test Site				
Tester				
Test Number				
Max Limit	25	ma		
Min Limit	2	ma		
kRad(Si)	30	31	40	41
LL	2.000	2.000	2.000	2.000
Min	4.978	4.579	4.923	4.577
Average	5.064	4.884	5.007	4.894
Max	5.195	5.006	5.074	5.082
UL	25.000	25.000	25.000	25.000

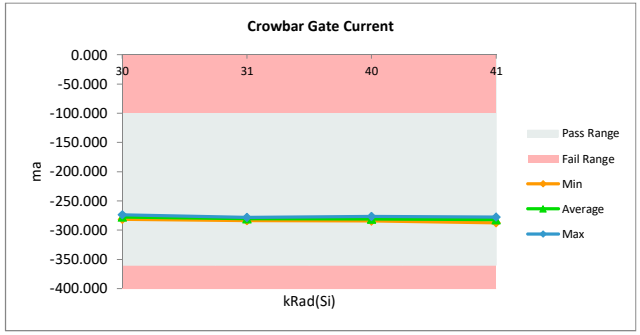


UC1834-SP TID Report

	Crowbar Gate Current		
Test Site			
Tester			
Test Number			
Unit	mA	ma	
Max Limit	-100	-100	
Min Limit	-360	-360	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-278.705	-281.445	-2.740
30	2	-277.886	-279.221	-1.335
30	3	-280.404	-276.366	4.038
30	4	-278.484	-276.465	2.019
30	5	-280.202	-273.711	6.491
40	6	-278.228	-284.439	-6.211
40	7	-277.597	-284.462	-6.865
40	8	-279.945	-276.526	3.419
40	9	-278.341	-279.948	-1.607
40	10	-278.857	-280.309	-1.452
31	17	-277.746	-278.352	-0.606
31	18	-279.731	-278.827	0.904
31	19	-279.205	-283.617	-4.412
31	20	-281.014	-279.322	1.692
31	21	-280.159	-282.150	-1.991
41	11	-275.540	-287.551	-12.011
41	12	-279.429	-277.550	1.879
41	13	-277.817	-280.413	-2.596
41	14	-278.494	-286.136	-7.642
41	15	-277.970	-278.599	-0.629
	Max	-275.540	-273.711	6.491
	Average	-278.788	-280.270	-1.483
	Min	-281.014	-287.551	-12.011
	Std Dev	1.266	3.579	4.417

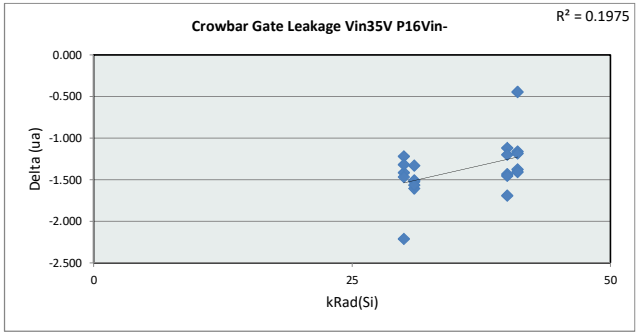


	Crowbar Gate Current			
Test Site				
Tester				
Test Number				
Max Limit	-100	ma		
Min Limit	-360	ma		
kRad(Si)	30	31	40	41
LL	-360.000	-360.000	-360.000	-360.000
Min	-281.445	-283.617	-284.462	-287.551
Average	-277.442	-280.454	-281.137	-282.050
Max	-273.711	-278.352	-276.526	-277.550
UL	-100.000	-100.000	-100.000	-100.000

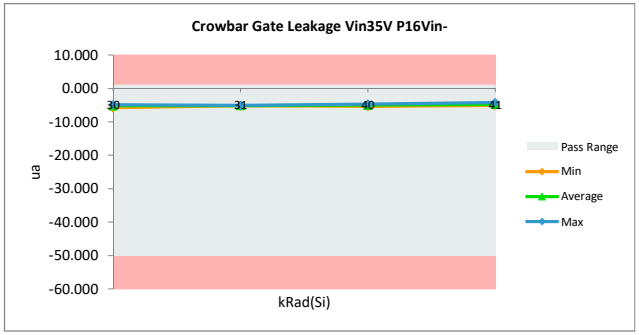


UC1834-SP TID Report

	Crowbar Gate Leakage Vin35V P16Vin-		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	1	1	
Min Limit	-50	-50	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-3.605	-5.022	-1.416
30	2	-3.608	-4.829	-1.221
30	3	-3.529	-5.742	-2.213
30	4	-3.744	-5.210	-1.466
30	5	-3.779	-5.098	-1.319
40	6	-3.572	-4.690	-1.118
40	7	-3.420	-4.852	-1.432
40	8	-3.551	-4.750	-1.199
40	9	-3.608	-5.061	-1.453
40	10	-3.646	-5.337	-1.691
31	17	-3.608	-5.134	-1.526
31	18	-3.682	-5.191	-1.509
31	19	-3.551	-5.155	-1.604
31	20	-3.494	-5.057	-1.564
31	21	-3.727	-5.057	-1.330
41	11	-3.763	-4.208	-0.445
41	12	-3.668	-4.831	-1.163
41	13	-3.677	-5.054	-1.377
41	14	-3.474	-4.881	-1.406
41	15	-3.575	-4.759	-1.185
	Max	-3.420	-4.208	-0.445
	Average	-3.614	-4.996	-1.382
	Min	-3.779	-5.742	-2.213
	Std Dev	0.098	0.303	0.326

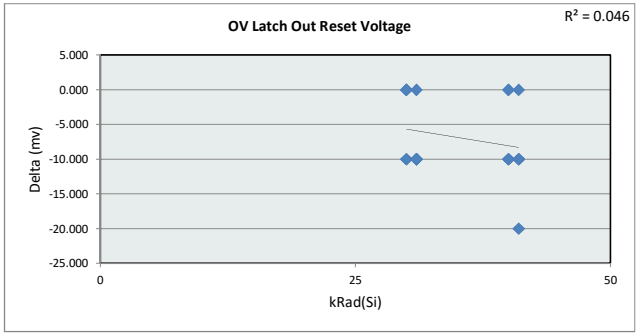


	Crowbar Gate Leakage Vin35V			
Test Site				
Tester				
Test Number				
Max Limit	1	ua		
Min Limit	-50	ua		
kRad(Si)	30	31	40	41
LL	-50.000	-50.000	-50.000	-50.000
Min	-5.742	-5.191	-5.337	-5.054
Average	-5.180	-5.119	-4.938	-4.746
Max	-4.829	-5.058	-4.690	-4.208
UL	1.000	1.000	1.000	1.000

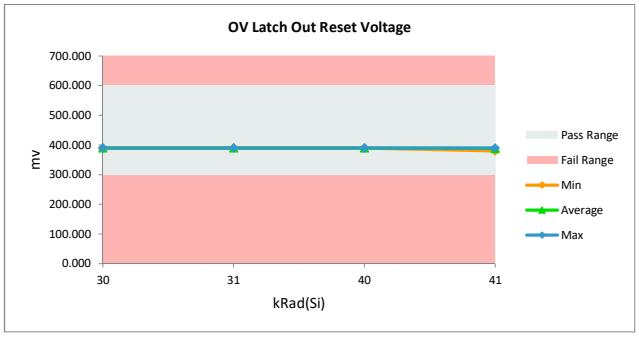


UC1834-SP TID Report

	OV Latch Out Reset Voltage		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	600	600	
Min Limit	300	300	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	399.999	390.000	-9.999
30	2	389.999	390.000	0.001
30	3	389.999	390.000	0.001
30	4	399.999	390.000	-9.999
30	5	389.999	390.000	0.001
40	6	389.999	390.000	0.001
40	7	399.999	390.000	-9.999
40	8	389.999	390.000	0.001
40	9	399.999	390.000	-9.999
40	10	399.999	390.000	-9.999
31	17	399.999	390.000	-9.999
31	18	399.999	390.000	-9.999
31	19	399.999	390.000	-9.999
31	20	389.999	390.000	0.001
31	21	399.999	390.000	-9.999
41	11	399.999	390.000	-9.999
41	12	399.999	390.000	-9.999
41	13	399.999	390.000	-9.999
41	14	399.999	380.000	-19.999
41	15	389.999	390.000	0.001
	Max	399.999	390.000	0.001
	Average	396.499	389.500	-6.999
	Min	389.999	380.000	-19.999
	Std Dev	4.894	2.236	5.712

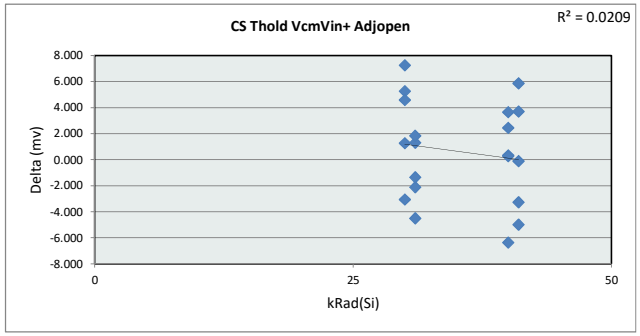


	OV Latch Out Reset Voltage			
Test Site				
Tester				
Test Number				
Max Limit	600	mv		
Min Limit	300	mv		
kRad(Si)	30	31	40	41
LL	300.000	300.000	300.000	300.000
Min	390.000	390.000	390.000	380.000
Average	390.000	390.000	390.000	388.000
Max	390.000	390.000	390.000	390.000
UL	600.000	600.000	600.000	600.000

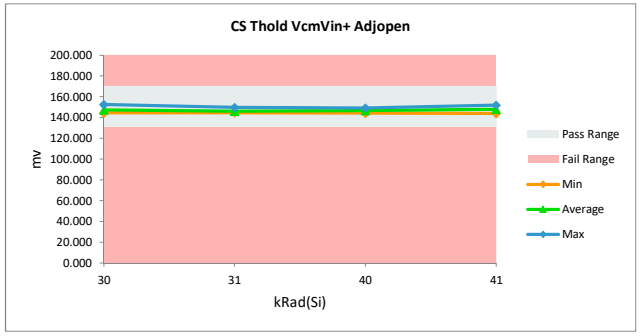


UC1834-SP TID Report

	CS Thold VcmVin+ Adjopen		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	170	170	
Min Limit	130	130	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	138.796	146.042	7.246
30	2	146.351	147.605	1.254
30	3	147.216	152.477	5.261
30	4	147.489	144.428	-3.061
30	5	141.419	145.988	4.569
40	6	145.853	148.286	2.433
40	7	146.691	147.025	0.334
40	8	151.059	144.691	-6.368
40	9	143.939	144.204	0.265
40	10	145.472	149.119	3.647
31	17	149.709	145.197	-4.512
31	18	151.867	149.750	-2.118
31	19	143.311	144.611	1.301
31	20	146.355	145.005	-1.350
31	21	143.725	145.557	1.832
41	11	145.126	145.005	-0.121
41	12	147.081	150.771	3.690
41	13	146.119	151.973	5.854
41	14	152.218	148.947	-3.272
41	15	148.787	143.797	-4.990
	Max	152.218	152.477	7.246
	Average	146.429	147.024	0.595
	Min	138.796	143.797	-6.368
	Std Dev	3.346	2.693	3.840

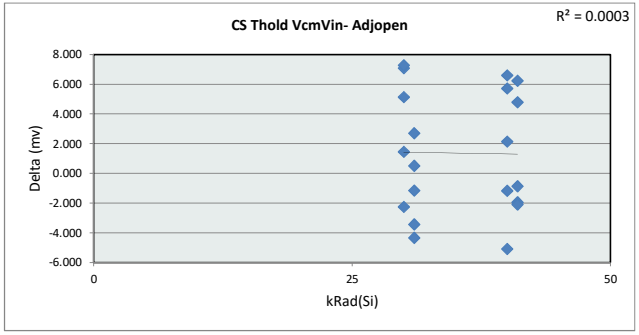


	CS Thold VcmVin+ Adjopen			
Test Site				
Tester				
Test Number				
Max Limit	170	mv		
Min Limit	130	mv		
kRad(Si)	30	31	40	41
LL	130.000	130.000	130.000	130.000
Min	144.428	144.611	144.204	143.797
Average	147.308	146.024	146.665	148.099
Max	152.477	149.750	149.119	151.973
UL	170.000	170.000	170.000	170.000

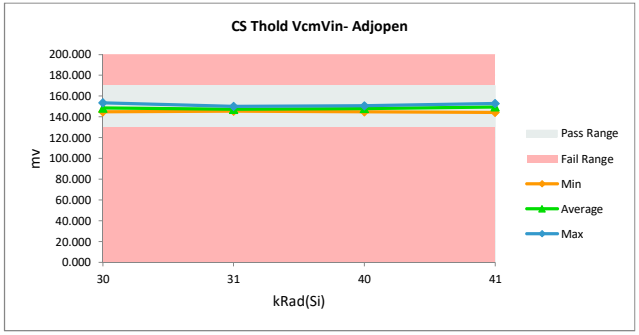


UC1834-SP TID Report

	CS Thold VcmVin- Adjopen		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	170	170	
Min Limit	130	130	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	139.559	146.645	7.087
30	2	147.983	149.433	1.450
30	3	148.522	153.648	5.125
30	4	147.273	145.002	-2.271
30	5	140.475	147.745	7.271
40	6	144.992	150.699	5.707
40	7	149.438	148.261	-1.178
40	8	150.008	144.906	-5.102
40	9	143.748	145.876	2.128
40	10	143.875	150.462	6.587
31	17	149.760	145.418	-4.341
31	18	153.465	150.028	-3.437
31	19	145.214	145.718	0.504
31	20	149.438	148.269	-1.170
31	21	144.609	147.305	2.697
41	11	146.359	144.411	-1.949
41	12	146.553	151.338	4.785
41	13	146.614	152.839	6.225
41	14	153.326	152.460	-0.867
41	15	149.397	147.303	-2.094
	Max	153.465	153.648	7.271
	Average	147.030	148.388	1.358
	Min	139.559	144.411	-5.102
	Std Dev	3.638	2.844	4.090

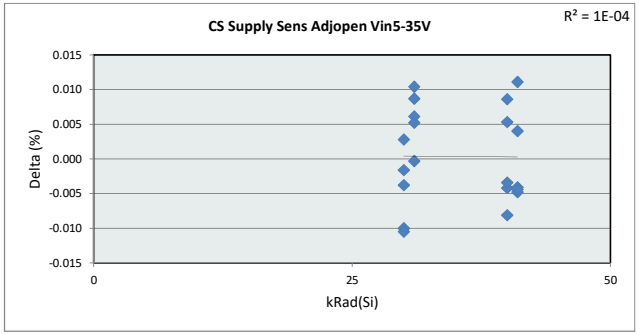


	CS Thold VcmVin- Adjopen			
Test Site				
Tester				
Test Number				
Max Limit	170	mv		
Min Limit	130	mv		
kRad(Si)	30	31	40	41
LL	130.000	130.000	130.000	130.000
Min	145.002	145.418	144.906	144.411
Average	148.495	147.348	148.041	149.670
Max	153.648	150.028	150.699	152.839
UL	170.000	170.000	170.000	170.000

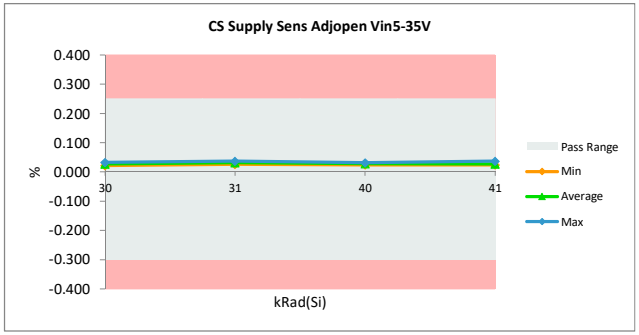


UC1834-SP TID Report

	CS Supply Sens Adjopen Vin5-35V		
Test Site			
Tester			
Test Number			
Unit	%	%	
Max Limit	0.25	0.25	
Min Limit	-0.3	-0.3	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	0.039	0.029	-0.010
30	2	0.028	0.027	-0.002
30	3	0.026	0.022	-0.004
30	4	0.030	0.032	0.003
30	5	0.037	0.026	-0.010
40	6	0.030	0.025	-0.004
40	7	0.023	0.031	0.009
40	8	0.025	0.031	0.005
40	9	0.034	0.030	-0.003
40	10	0.032	0.024	-0.008
31	17	0.025	0.035	0.010
31	18	0.020	0.026	0.006
31	19	0.028	0.037	0.009
31	20	0.027	0.027	0.000
31	21	0.030	0.035	0.005
41	11	0.026	0.037	0.011
41	12	0.030	0.025	-0.005
41	13	0.029	0.025	-0.004
41	14	0.022	0.026	0.004
41	15	0.029	0.024	-0.004
	Max	0.039	0.037	0.011
	Average	0.028	0.029	0.000
	Min	0.020	0.022	-0.010
	Std Dev	0.005	0.005	0.007

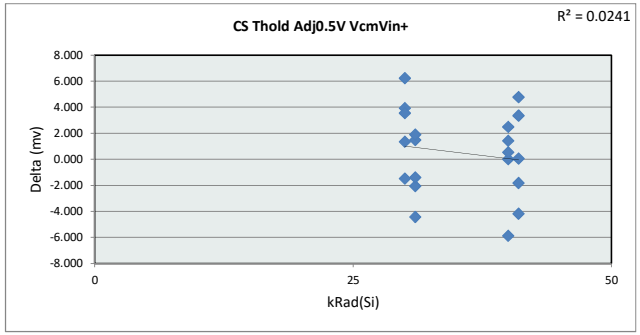


	CS Supply Sens Adjopen Vin5-3			
Test Site				
Tester				
Test Number				
Max Limit	0.25	%		
Min Limit	-0.3	%		
kRad(Si)	30	31	40	41
LL	-0.300	-0.300	-0.300	-0.300
Min	0.022	0.026	0.024	0.024
Average	0.027	0.032	0.028	0.027
Max	0.032	0.037	0.031	0.037
UL	0.250	0.250	0.250	0.250

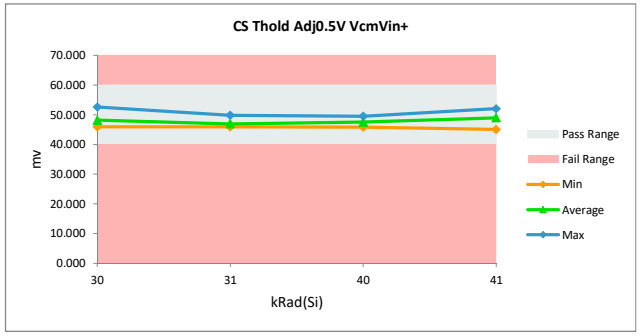


UC1834-SP TID Report

	CS Thold Adj0.5V VcmVin+		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	60	60	
Min Limit	40	40	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	41.032	47.263	6.231
30	2	47.028	48.367	1.339
30	3	48.657	52.580	3.923
30	4	47.432	45.941	-1.491
30	5	43.102	46.641	3.539
40	6	47.595	49.021	1.426
40	7	47.380	47.376	-0.003
40	8	51.677	45.789	-5.888
40	9	45.402	45.935	0.533
40	10	47.014	49.489	2.475
31	17	50.397	45.955	-4.442
31	18	51.877	49.809	-2.068
31	19	44.530	46.009	1.479
31	20	47.430	46.038	-1.392
31	21	45.036	46.925	1.889
41	11	45.905	45.956	0.050
41	12	48.319	51.678	3.359
41	13	47.276	52.040	4.764
41	14	52.012	50.182	-1.830
41	15	49.212	45.020	-4.192
	Max	52.012	52.580	6.231
	Average	47.416	47.901	0.485
	Min	41.032	45.020	-5.888
	Std Dev	2.844	2.344	3.210

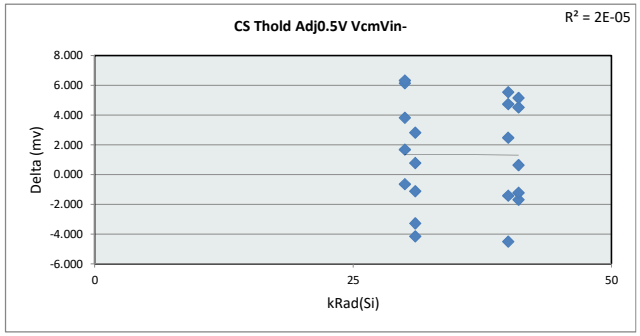


	CS Thold Adj0.5V VcmVin+			
Test Site				
Tester				
Test Number				
Max Limit	60	mv		
Min Limit	40	mv		
kRad(Si)	30	31	40	41
LL	40.000	40.000	40.000	40.000
Min	45.941	45.955	45.789	45.020
Average	48.158	46.947	47.522	48.975
Max	52.580	49.809	49.489	52.040
UL	60.000	60.000	60.000	60.000

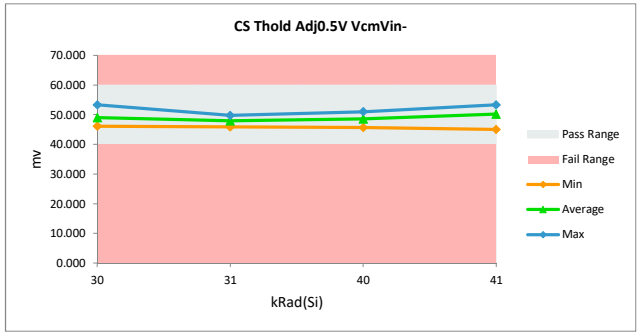


UC1834-SP TID Report

	CS Thold Adj0.5V VcmVin-		
Test Site			
Tester			
Test Number			
Unit	mV	mv	
Max Limit	60	60	
Min Limit	40	40	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	41.384	47.520	6.135
30	2	48.178	49.849	1.671
30	3	49.496	53.316	3.820
30	4	46.766	46.121	-0.645
30	5	41.738	48.064	6.326
40	6	46.277	51.014	4.737
40	7	49.679	48.255	-1.424
40	8	50.199	45.685	-4.514
40	9	44.793	47.271	2.477
40	10	44.958	50.487	5.529
31	17	50.008	45.849	-4.159
31	18	53.039	49.752	-3.288
31	19	45.985	46.757	0.772
31	20	50.052	48.922	-1.130
31	21	45.484	48.296	2.812
41	11	46.695	45.004	-1.690
41	12	47.373	51.889	4.516
41	13	47.331	52.483	5.152
41	14	52.650	53.282	0.632
41	15	49.375	48.144	-1.231
	Max	53.039	53.316	6.326
	Average	47.573	48.898	1.325
	Min	41.384	45.004	-4.514
	Std Dev	3.107	2.543	3.490

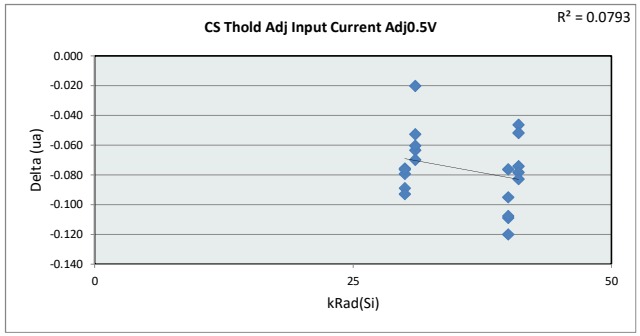


	CS Thold Adj0.5V VcmVin-			
Test Site				
Tester				
Test Number				
Max Limit	60	mv		
Min Limit	40	mv		
kRad(Si)	30	31	40	41
LL	40.000	40.000	40.000	40.000
Min	46.121	45.849	45.685	45.004
Average	48.974	47.915	48.542	50.161
Max	53.316	49.752	51.014	53.282
UL	60.000	60.000	60.000	60.000

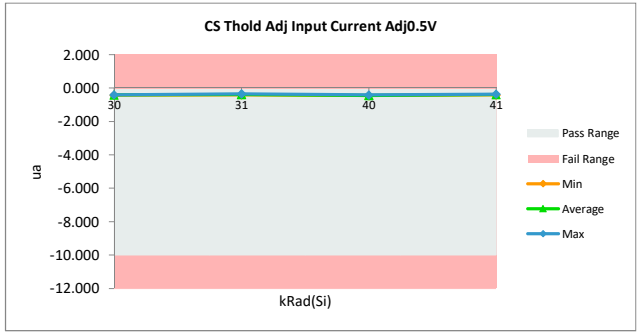


UC1834-SP TID Report

	CS Thold Adj Input Current Adj0.5V		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	0	-0.0001	
Min Limit	-10	-10	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-0.336	-0.424	-0.089
30	2	-0.325	-0.418	-0.093
30	3	-0.322	-0.401	-0.079
30	4	-0.336	-0.411	-0.076
30	5	-0.348	-0.424	-0.076
40	6	-0.325	-0.420	-0.095
40	7	-0.340	-0.417	-0.076
40	8	-0.340	-0.449	-0.109
40	9	-0.339	-0.447	-0.108
40	10	-0.330	-0.450	-0.120
31	17	-0.333	-0.397	-0.063
31	18	-0.342	-0.402	-0.060
31	19	-0.332	-0.352	-0.020
31	20	-0.327	-0.380	-0.053
31	21	-0.330	-0.400	-0.070
41	11	-0.317	-0.363	-0.046
41	12	-0.340	-0.414	-0.074
41	13	-0.332	-0.410	-0.078
41	14	-0.335	-0.387	-0.052
41	15	-0.330	-0.413	-0.083
	Max	-0.317	-0.352	-0.020
	Average	-0.333	-0.409	-0.076
	Min	-0.348	-0.450	-0.120
	Std Dev	0.008	0.026	0.023

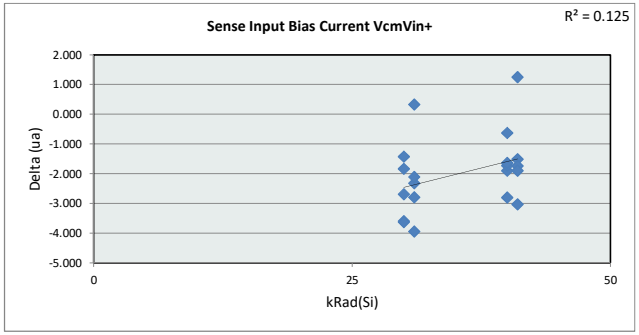


	CS Thold Adj Input Current Adj			
Test Site				
Tester				
Test Number				
Max Limit	-0.0001	ua		
Min Limit	-10	ua		
kRad(Si)	30	31	40	41
LL	-10.000	-10.000	-10.000	-10.000
Min	-0.425	-0.402	-0.450	-0.414
Average	-0.416	-0.386	-0.437	-0.397
Max	-0.401	-0.352	-0.417	-0.363
UL	0.000	0.000	0.000	0.000

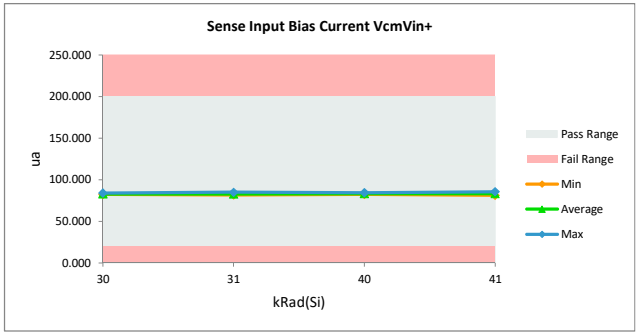


UC1834-SP TID Report

	Sense Input Bias Current VcmVin+		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	200	200	
Min Limit	20	20	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	86.201	83.515	-2.686
30	2	83.792	82.367	-1.425
30	3	84.561	82.727	-1.835
30	4	85.831	82.235	-3.596
30	5	87.536	83.912	-3.625
40	6	84.695	82.794	-1.901
40	7	85.003	84.377	-0.627
40	8	86.292	83.492	-2.800
40	9	84.778	83.050	-1.727
40	10	83.976	82.340	-1.636
31	17	84.636	84.965	0.329
31	18	84.771	82.447	-2.324
31	19	85.690	81.748	-3.942
31	20	84.093	81.984	-2.109
31	21	85.690	82.896	-2.794
41	11	84.309	85.559	1.250
41	12	84.987	83.473	-1.514
41	13	85.107	83.368	-1.739
41	14	84.150	81.119	-3.030
41	15	85.069	83.172	-1.897
	Max	87.536	85.559	1.250
	Average	85.058	83.077	-1.981
	Min	83.792	81.119	-3.942
	Std Dev	0.923	1.074	1.270

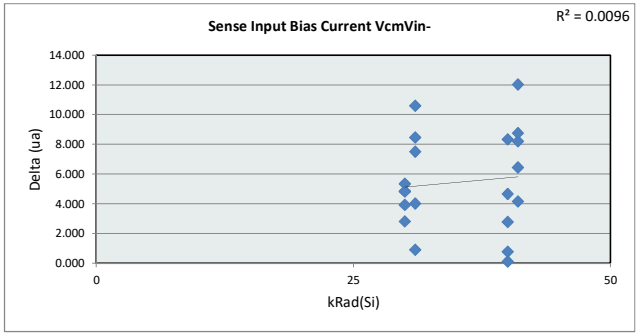


	Sense Input Bias Current VcmV			
Test Site				
Tester				
Test Number				
Max Limit	200	ua		
Min Limit	20	ua		
kRad(Si)	30	31	40	41
LL	20.000	20.000	20.000	20.000
Min	82.235	81.749	82.340	81.119
Average	82.951	82.808	83.211	83.338
Max	83.912	84.965	84.377	85.559
UL	200.000	200.000	200.000	200.000

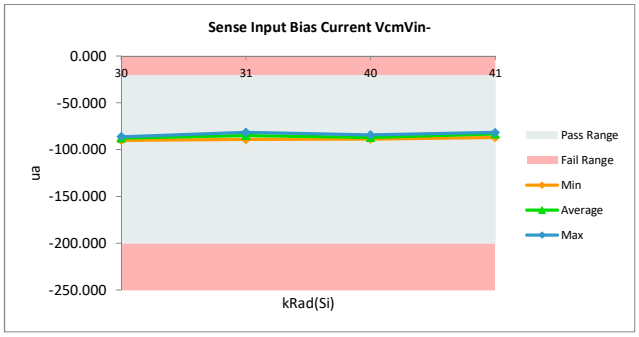


UC1834-SP TID Report

	Sense Input Bias Current VcmVin-		
Test Site			
Tester			
Test Number			
Unit	uA	ua	
Max Limit	-20	-20	
Min Limit	-200	-200	
kRad(Si)	Serial #	PRE_LDR	POST_LDR	Delta
30	1	-94.098	-90.169	3.929
30	2	-91.621	-86.275	5.347
30	3	-91.069	-88.253	2.816
30	4	-92.007	-87.157	4.851
30	5	-91.019	-86.190	4.829
40	6	-86.798	-86.676	0.121
40	7	-89.392	-88.605	0.787
40	8	-90.869	-88.085	2.783
40	9	-91.838	-87.175	4.663
40	10	-92.659	-84.332	8.326
31	17	-90.144	-89.233	0.911
31	18	-92.101	-81.516	10.585
31	19	-92.329	-83.867	8.462
31	20	-90.784	-83.277	7.507
31	21	-90.895	-86.877	4.018
41	11	-91.048	-86.881	4.166
41	12	-95.676	-83.655	12.021
41	13	-90.107	-81.903	8.204
41	14	-88.717	-82.265	6.452
41	15	-90.467	-81.715	8.752
	Max	-86.798	-81.516	12.021
	Average	-91.182	-85.705	5.477
	Min	-95.676	-90.169	0.121
	Std Dev	1.864	2.681	3.267



	Sense Input Bias Current VcmV			
Test Site				
Tester				
Test Number				
Max Limit	-20	ua		
Min Limit	-200	ua		
kRad(Si)	30	31	40	41
LL	-200.000	-200.000	-200.000	-200.000
Min	-90.169	-89.233	-88.605	-86.881
Average	-87.609	-84.954	-86.975	-83.284
Max	-86.190	-81.516	-84.332	-81.715
UL	-20.000	-20.000	-20.000	-20.000



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