

# ***TL7700-SEP Production Flow and Reliability Report***

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## **ABSTRACT**

The TL7700-SEP is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation, portable battery operation, and automotive applications. The TL7700- SEP device is designed for operation from –55°C to 125°C.

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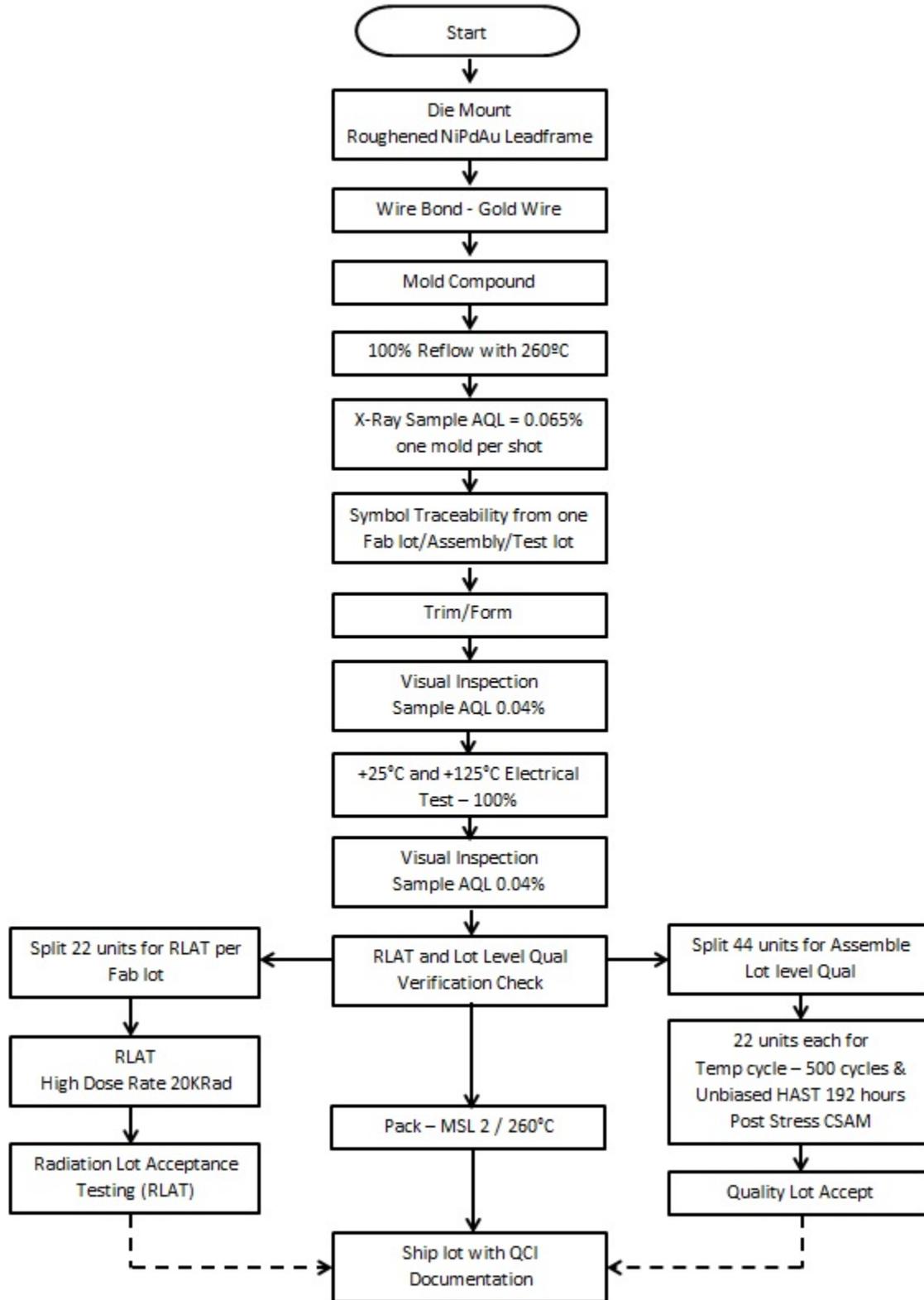
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## 1 Device Introduction

TL7700-SEP is a Radiation Hardened device in plastic package which allow this device to be use in a space application. The device was verified immune to 43 Mev·cm<sup>2</sup>/mg at 125°C for single event latchup. Each Fab lot was tested according to MIL-STD-883 for Radiation Lot Acceptance Tested (RLAT) up to 20 krad(Si) and each Assembly and Test lot will follow the process flow shown in [Section 2](#). To ensure the quality of TL7700-SEP, it is qualified with Space EP requirements. See [Section 3](#) for further details.

**2 TL7700-SEP Production Flow**



### 3 Device Qualification

The following is the device qualification summary:

#### Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing full scale quality and reliability tests on the actual device or using previously qualified device(s) through "Qualification by Similarity" (QBS) rules. By establishing similarity between the new device and those qualified previously, repetitive tests will be eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration.

The QBS rules for a technology, product, test parameters or package shall define which attributes are required to remain fixed in order for the QBS rules to apply. The attributes which are expected and allowed to vary will be reviewed and a QBS plan shall be developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device shall be reviewed for conformance to the QBS rule sets applicable to that device. See JEDEC JESD47 for more information.

Device Baseline				
TI Device:	TL7700CMPWTPSEP/ TL7700CMPWPSEP		Assembly Site:	TI-MLA (Malaysia)
DLA VID:	V62/19602 -01XE		Test Site:	TI-MLA (Malaysia)
Wafer Fab:	SFAB		Pin/Package Type:	TSSOP (PW)   8
Fab Process:	J11		Leadframe:	Cu
Fab Technology:	J11		Termination Finish:	NiPdAu
Die Revision:	C		Bond Wire:	24.3 μm Au
Die Name:	STLN7700CPS		Moisture Sensitivity:	MSL 2 / 260°C
ESD CDM:	±1000V			
ESD HBM:	±500V			

<sup>1</sup>Baseline information in effect as of the date of this report

Space Enhanced Products New Device Qualification Matrix				
Note that qualification by similarity ("qualification family") per JEDEC JESD47 is allowed				
Description	Condition	Sample Size Used/Rejects	Lots Required	Test Method
Electromigration	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
Wire Bond Life	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
Electrical Characterization	TI Data Sheet	10	3	N/A
Electrostatic Discharge Sensitivity	HBM	3 units/voltage	1	EIA/JESD22-A114
	CDM			EIA/JESD22-C101
Latch-up	Per Technology	6/0	1	EIA/JESD78
Physical Dimensions	TI Data Sheet	5/0	1	EIA/JESD22- B100
Thermal Impedance	Theta-JA on board	Per Pin-Package	N/A	EIA/JESD51
Bias Life Test	125°C / 1000 hours or equivalent	77/0	3	JESD22-A108*
Biased HAST	130°C / 85% / 96 hours	77/0	3	JESD22-A110*
Extended Biased HAST	130°C / 85% / 250 hours (for reference)	77/0	1	JESD22-A110*
Unbiased HAST	130°C / 85% / 96 hours	77/0	3	JESD22-A.118*
Temperature Cycle	-65°C to +150°C non-biased for 500 cycles	77/0	3	JESD22-A104*

<b>Space Enhanced Products New Device Qualification Matrix</b>				
<b>Note that qualification by similarity (“qualification family”) per JEDEC JESD47 is allowed</b>				
Solder Heat	260°C for 10 seconds	22/0	1	JESD22-B106
Resistance to Solvents	Ink symbol only	12/0	1	JESD22-B107
Solderability	Condition A (steam age for 8 hours)	22/0	1	ANSI/J-STD-002-92
Flammability	Method A / Method B	5/0	1	UL-1964
Bond Shear	Per wire size	5 units x 30/0 bonds	3	JESD22-B116
Bond Pull Strength	Per wire size	5 units x 30/0 bonds	3	ASTM F-459
Die Shear	Per die size	5/0	3	TM 2019
High Temp Storage	150 °C / 1,000 hours	15/0	3	JESD22-A103-A*
Moisture Sensitivity	Surface Mount Only	12	1	J-STD-020-A*
Radiation Response Characterization	Total Ionization Dose, and Single-Event Latchup	5 units/dose level	1	MIL-STD-883/Method 1019
Outgassing Characterization	TML (Total Mass Lost), CVCM (Collected Volatile Condensable material), WVR (Water vapor recorded)	5	1	ASTM E595
*Precondition performed per JEDEC Std. 22, Method A112/A113				

#### 4 Outgas Test Report

Outgassing test was performed on 5 units. A total mass loss (TML) of 1.00% and collected volatile condensable material (CVCM) of 0.10% were used as screening levels for rejection of spacecraft materials. The outgas test was performed in a vacuum environment of less than  $5 \times 10^{-5}$  torr according to ASTM E 595, for a duration of 24 hours, at 125°C. The TML, CVCM, and the amount of Water Vapor Recovered (WVR) were measured after the test.

**RESULTS** : The following tables list the results of the testing:

Table 1: Outgas test results.

Sample	TML (%)	CVCM (%)	WVR (%)
	0.05	<0.01	0.03

### Quality and Reliability Data Disclaimer

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