Application Note How TPSI3133 DESAT Can Protect Your Expensive SiC MOSFETs and IGBTs



Tilden Chen and Akshaya Ramachandran

ABSTRACT

Protecting power semiconductors like SiC MOSFETs and IGBTs from damage due to oversaturation is critical in power electronics design. When these devices perform beyond their intended operating region, excessive power dissipation can lead to thermal stress and failure.

Desaturation (DESAT) protection circuits offer cost-effective protection by monitoring the voltage across the semiconductor and shutting it down during an overcurrent event. This article explores how DESAT protection works, key circuit components, and how to design a DESAT circuit with the TPSI3133 isolated switch driver.

Table of Contents

1 Why DESAT Protection Is Needed	2
1.1 Key Considerations for DESAT Protection	3
2 Key DESAT Circuit Components	3
2.1 Circuit Startup Behavior	3
2.1 Circuit Startup Behavior	4
3.1 Design Requirements	4
3.2 Threshold Equations	4
3.3 Given Parameters	4
3.4 Inserting Given Parameters into Equations	5
3.5 Solving Equations for Unknowns	
3.6 Selecting Resistances to Satisfy Equations	
3.7 Determining Blanking Capacitance	
3.8 Final Component Values	6
3.8 Final Component Values 3.9 Lab Testing	6
4 Closing	6
•	

Trademarks

All trademarks are the property of their respective owners.



1 Why DESAT Protection Is Needed

Power semiconductors like MOSFETs and IGBTs ideally operate in a fully saturated state: ohmic region for MOSFETs and saturation region for IGBTs. The voltage across, V_{DS} for MOSFETs or V_{CE} for IGBTs, remains low to minimize power dissipation. However, when these devices enter an oversaturated state as shown in Figure 1-1, small increases in current cause large voltage increases, leading to excessive power dissipation and potential damage.

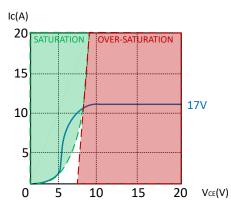


Figure 1-1. Example IGBT I-V Curve

Some isolated switch drivers include a desaturation (DESAT) protection feature that monitors V_{DS} or V_{CE} and quickly shuts down the semiconductor during an overcurrent event. The TPSI31xx is a family of fully integrated isolated switch drivers, which when combined with an external power switch, forms a complete isolated solid-state relay solution.

The TPSI3133, as shown in Figure 1-2, is a variant specifically intended for DESAT due to its internal pulldown MOSFET on the fault comparator input. This internal MOSFET prevents false positives while the IGBT/SiC MOSFET is off by pulling down the fault comparator input and keeping it pulled down for an additional 100ns after EN goes high, allowing the IGBT/SiC MOSFET to fully turn on.

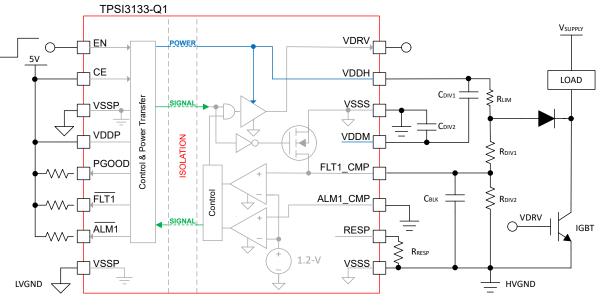


Figure 1-2. DESAT With TPSI3133



1.1 Key Considerations for DESAT Protection

DESAT protection circuits are typically configured with IGBTs because IGBTs show distinct voltages (V_{CE}) across current (I_C) in the saturation region which makes detection easier, have sharper transitions into the active region, and generally able to handle more power due to larger die size (many have a short circuit withstand rating).

DESAT can also work with SiC MOSFETs. The problem with low voltage MOSFETs is since the overcurrent threshold is typically set well above normal operation to avoid false positives, a low voltage MOSFET may be damaged by overheating well before the circuit even detects an overcurrent event.

By implementing DESAT protection, engineers can ensure power semiconductors stay within safe operating area.

2 Key DESAT Circuit Components

- 1. Blocking diode: Protects the circuit from high voltage while the IGBT/SiC MOSFET is off.
- 2. Current limiting resistor (R_{LIM}) to limit diode forward current.
- 3. DESAT threshold detection (R_{DIV1}, R_{DIV2}): Defines the voltage threshold for detecting oversaturation.
- 4. Blanking capacitance (C_{BLK}): Filters noise and prevents false triggering. While blanking capacitance helps avoid false positives, it may also extend stress time on the IGBT/SiC MOSFET during overcurrent events.

2.1 Circuit Startup Behavior

At power-up while EN is low, TPSI3133 receives power and begins to transfer power to its secondary rails (VDDM and VDDH). The internal MOSFET pulls down the comparator input to avoid a false trigger. Once EN goes high, the two current paths (paths 1 and 2) compete to set the comparator input voltage as shown in Figure 2-1. Since Path 1 normally would be faster than path 2 due to IGBT turn-on delay, once EN goes high, the TPSI3133 keeps the comparator input pulled down for an additional 100ns, allowing the IGBT to fully turn on before fault detection. Adding blanking capacitance (C_{BLK}) can provide additional delay but must be carefully selected in order to minimize stress time. During an overload condition, the IGBT V_{CE} rises, which brings up the voltage at the HV diode anode, trips the fault comparator threshold. Once the TPSI3133 detects the fault, it shuts off the driver which turns off the IGBT, protecting the system.

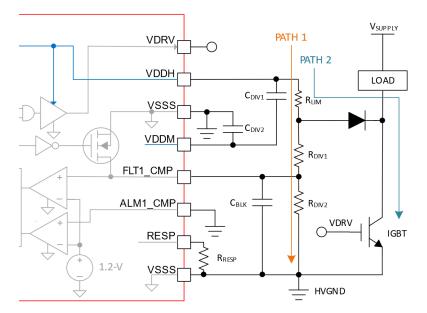


Figure 2-1. DESAT KVL Paths

3 Design Example

3.1 Design Requirements

Table 3-1 lists the requirements for an example DESAT design.

Table 3-1. Example Design Requirements
--

PARAMETER	VALUE
Overcurrent Threshold	10A
Maximum Response Time	10µs

3.2 Threshold Equations

Selecting appropriate resistance values ensures that the blocking diode becomes forward biased while the IGBT is on, allowing proper voltage sensing.

1. Condition for sensing voltage, allows the blocking diode to become forward biased when IGBT is on:

$$\left(V_{CE(DESAT)} + V_{F(DIODE)}\right) < \frac{R_{DIV1} + R_{DIV2}}{R_{DIV2} + R_{DIV1} + R_{LIM}} \times VDDH$$
(1)

 Overcurrent threshold equation, select the desired voltage threshold (V_{CE (DESAT)}) to trip the comparator (V_{REF+}):

$$V_{REF+} < \frac{R_{DIV2}}{R_{DIV2} + R_{DIV1}} \times \left(V_{CE(DESAT)} + V_{F(DIODE)} \right)$$
⁽²⁾

Using the example IGBT I-V curve from earlier, it looks like $I_C = 10$ A at $V_{CE} = 7.5$ V. With this overcurrent threshold value, solve for the resistances. Please keep in mind that I-V curves are typical and devices may individually have variation.

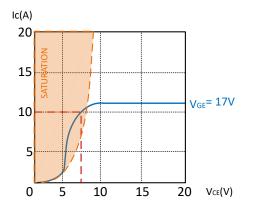


Figure 3-1. DESAT Selection V_{CE} Threshold

3.3 Given Parameters

4

Select R_{LIM} to limit diode forward current. Given the example HV diode I-V curve in Figure 3-2, selecting 54.9k Ω would limit V_F to 0.7V. Please keep in mind that the TPSI3100 family has 25mW available for powering auxiliary circuitry, R_{LIM} = 54.9k Ω consumes up to 5.26mW.

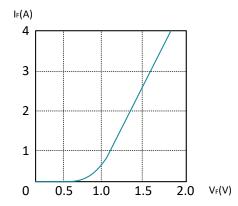


Figure 3-2. Example HV Diode I-V Curve

PARAMETER	VALUE	
V _{CE (DESAT)}	7.5V	
V _{F (DIODE)}	0.7V	
V _{REF+}	1.23V	
R _{LIM}	54.9kΩ	

Table 3-2. Given	Design	Parameter	Values
------------------	--------	-----------	--------

3.4 Inserting Given Parameters into Equations

- 1. $(7.5V + 0.7V) \times 1.2_{(20\% margin)} < \frac{R_{DIV1} + R_{DIV2}}{R_{DIV2} + R_{DIV1} + 54.9e3} \times 17V$
- 2. $\frac{R_{DIV2}}{R_{DIV2} + R_{DIV1}} \times (7.5V + 0.7V) > 1.23V^* 1.2_{(20\% margin)}$

3.5 Solving Equations for Unknowns

- 1. $R_{DIV1} > -\frac{41}{50}$
- 2. $R_{DIV2} > \frac{1}{73}(5325300 73 \times R_{DIV1})$

3.6 Selecting Resistances to Satisfy Equations

Table 3-3. Selected Design Resistances

PARAMETER	VALUE
R _{DIV1}	23.9kΩ
R _{DIV2}	11.5kΩ

3.7 Determining Blanking Capacitance

Select a C_{BLK} value based on the 10µs maximum delay requirement, starting with the general RC equation. If we use $R_{RESP} < 10k\Omega$, propagation delay time can be as long as 460ns and needs to be accounted for. Use Thevenin/Norton equivalent to determine the equivalent resistance seen by C_{BLK} .

$$V_C = V_S \times \left(1 - e^{-\frac{t}{RC}}\right) \tag{3}$$

$$V_{REF+} < VDDH \times \left(1 - e^{\frac{-(t_{MAXDELAY} - t_{RESP}) \times (R_{LIM} + R_{DIV1} + R_{DIV2})}{(R_{LIM} + R_{DIV1}) \times R_{DIV2} \times C_{BLK}}}\right)$$
(4)

$$1.23 < 17 \times \left(1 - e^{\frac{-(10\mu - 460n) \times (54.9e3 + 23.9e3 + 11.5e3)}{(54.9e3 + 23.9e3) \times 11.5e3 \times C_{BLK}}}\right)$$
(5)



(6)

 $0 < C_{BLK} < 12.66 nF$

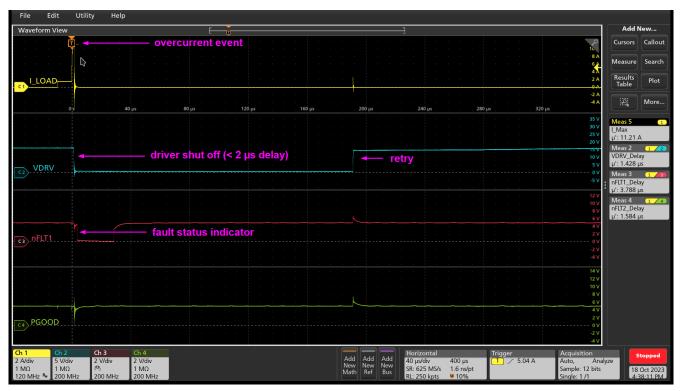
3.8 Final Component Values

With these selected values, the design prevents oversaturation and meets the desired delay time specified by the initial requirements.

Table 3-4. Final Design Component Values		
COMPONENT	VALUE	
R _{LIM}	54.9kΩ	
R _{DIV1}	23.9kΩ	
R _{DIV2}	11.5kΩ	
C _{BLK}	<12.66nF	

3.9 Lab Testing

The waveform below shows the DESAT circuit in action, confirming its ability to detect overcurrent conditions and shut down the IGBT before damage occurs.





4 Closing

6

Proper implementation of DESAT protection enhances the reliability and lifespan of SiC MOSFETs and IGBTs by preventing destructive oversaturation. By carefully selecting an isolated gate driver like TPSI3133 with DESAT protection and calculating component values, designers can optimize around speed while also preventing false positives. The article walks through an example of how to select components to meet specific DESAT design requirements. Engineers can use DESAT protection for their power semiconductors against overcurrent events, ensuring efficiency and long-term performance in high-power applications.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2025, Texas Instruments Incorporated