Application Brief

Using the TPS62830x to Power LPCAMM2

Andreas Mueller

Introduction

LPCAMM2 memory modules require several supply voltage rails, such as 1.8V (VDD1), 1.05V (VDD2H), 0.9V (VDD2L) and 0.5V / 0.3V (VDDQ), as standardized by JDEC in JESD318 (Compression Attached Memory Module (CAMM2) Common Standard). These voltage rails are covered by JESD301-3 (PMIC5200 Power Management IC Specification for LPDDR5). But the LPCAMM2 standard (JESD318A) is also describing an alternative architecture, using a PMIC5100 Power Management IC for DDR5 memory, to generate the VDD1 and VDD2 voltage rails and combine it with a separate discrete voltage regulator for generating VDDQ as illustrated in Figure 1.

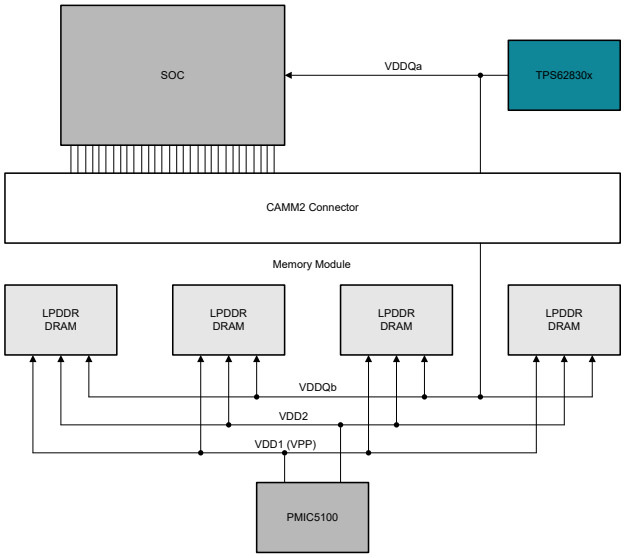

Figure 1. TPS62830x in LP5 CAMM2 VDDQ Common Power Delivery Method

This application brief is describing a way to overcome the discrete VDDQ design challenges with the help of the TPS62830x device family.

Discrete VDDQ Rail With TPS62830x

The TPS62830x family is natively supporting an output voltage of 0.5V as required for the VDDQ rail in LPCAMM2. Usually the required VDDQ current consumption is in the range of 1 A to 3 A, depending on the memory size and on VDDQ Split-Rail method or Common method implementation. The TPS62830x family consists of 1, 2, 3 and 4A device variants with comparable performance. In particular, high output voltage accuracy and optimized load transient performance are features, meeting the VDDQ requirements. The transient optimized BoM per the device-specific data sheet, with a 0.24µH inductor and 2 x 22µF output capacitor, can be recommended for this VDDQ supply application. The feedback voltage divider is not required for an output voltage of 0.5V. as this is the native FB reference voltage. The MODE pin can be set to high for enabling the Forced PWM operation. Figure 2 is illustrating an example application for VDDQ on LPCAMM2.

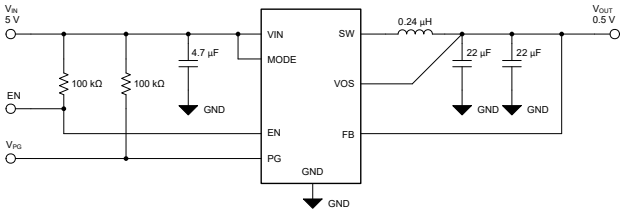

Figure 2. Example Application for LPCAMM2 VDDQ With TPS62830x

The load transient performance in this configuration is shown for a load step from 0.1A to 3A at 2.5A/µs in Figure 3.

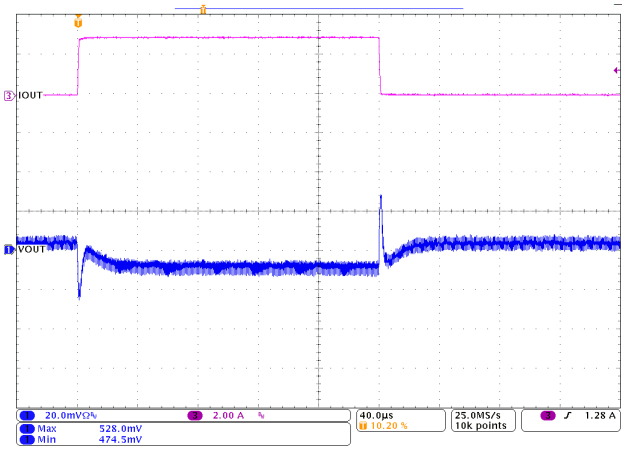

Figure 3. TPS628303 Load Transient Response 0.1A to 3A at 2.5A/µs

The shown load transient is including the static load regulation and the voltage ripple due to switching noise. The output voltage does not exceed the voltage range of 0.47V to 0.57 , which is specified in JESD209-5C (Low Power Double Data Rate LPDDR 5/5X).

The TPS62830x is ramping with a fixed soft-start time of typically 300µs. Together with the enable delay time of ca. 120µs the output voltage is fully powered within 420µs (max. 660µs) as shown in Figure 4.

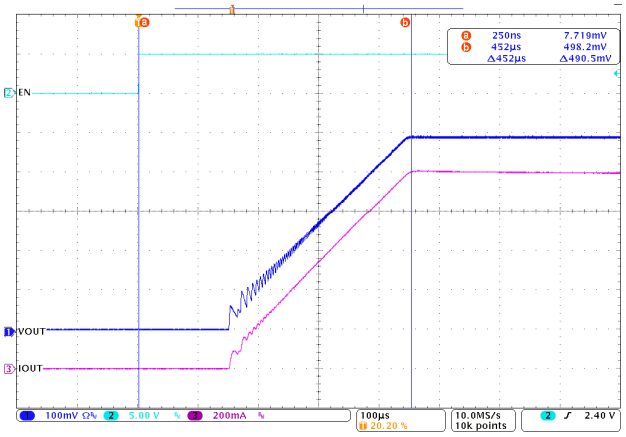

Figure 4. TPS628303 Soft Start at 1 A Load

The VDDQ rail is supposed to ramp as the last in the sequence of all supplies per JESD209-5C. The fast defined start-up time of the TPS62830x can help to meet the required maximum overall power ramp duration of 20ms.

The power-off sequence as defined in JESD209-5C is requiring VDDQ to ramp down as the fastest of all rails. In case of an uncontrolled power off, the maximum power-off ramp down time is specified with 2 s. The TPS62830x has a strong active discharge current of 400mA for fast ramp-down, even at 0 A load as shown in Figure 5.

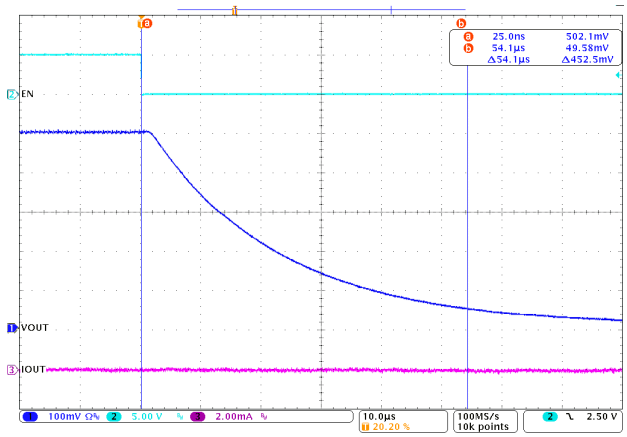

Figure 5. TPS628303 Disable at 0 A Load

Implementing DVFSQ Support With TPS62830x

Although JESD318 (Compression Attached Memory Module (CAMM2) Common Standard) is clearly excluding the 0.3V support for DVFSQ in the discrete VDDQ implementation, it can be possible to emulate DVFSQ control with the circuit in Figure 6.

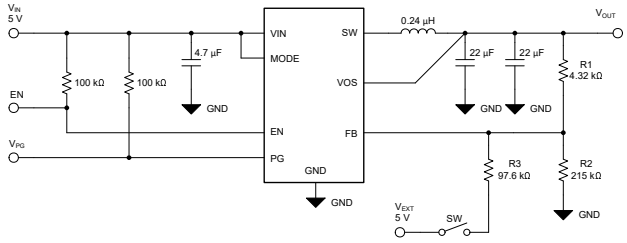

Figure 6. TPS62830x DVFSQ Implementation Example

The output voltage when the switch is open can be calculated with Equation 1.

$$V_{OUT} = V_{FB} \times \left(\frac{R_1}{R_2} + 1\right) \quad (1)$$

The output voltage when the switch is closed can be calculated with Equation 2.

$$V_{OUT} = V_{FB} \times \left(\frac{R_1}{R_2} + 1\right) - \frac{R_1}{R_3} \times (V_{EXT} - V_{FB}) \quad (2)$$

The resistor values in Figure 6 are setting up V_{OUT} = 0.51V for an open switch and V_{OUT} = 0.31V for a closed switch. These values are considering 10mV voltage drop across the CAMM2 connector and the

PCB, as recommended in JESD318A for a VDDQ Common power delivery method.

The voltage level transition is shown in Figure 7.

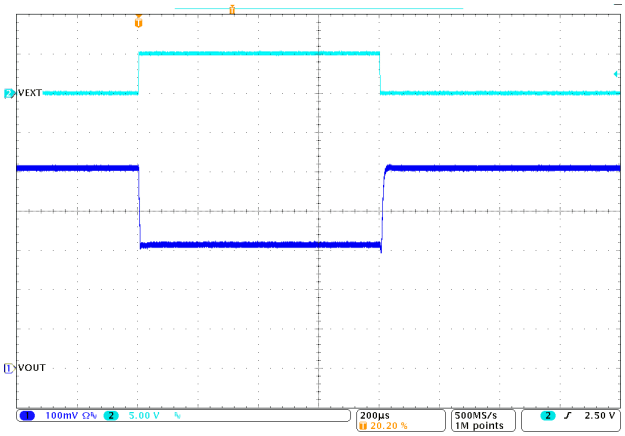

Figure 7. TPS628303 DVFSQ

The VIN_BULK supply of the PMIC5100 can be used as an external reference voltage as an example, but the TPS62830x output voltage accuracy now also depends on this external voltage.

TPS62830x – Dual Source Package

The TPS62830x device family is available in two package types (QFN and SOT583), which are layout compatible. When considered in the design phase, the board designers can overlap both package footprints like in Figure 8. This overlap provides flexibility to switch between packages and mitigate any potential supply issues.

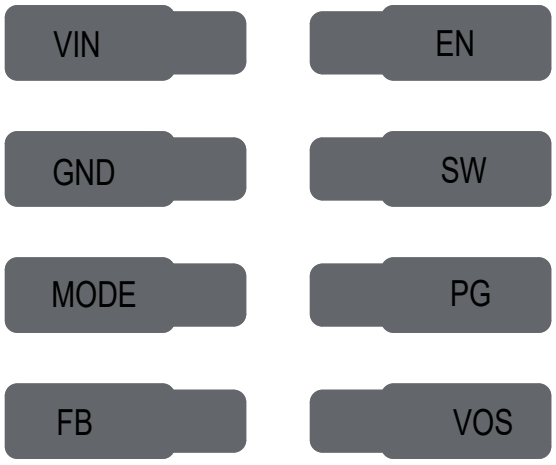

Figure 8. Overlapped QFN and SOT583 Footprints

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