Application Note
Using the TPS6284x in an Inverting Buck-Boost Topology

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ABSTRACT

The TPS6284x family is a high-efficiency step-down converter with ultra-low operating quiescent current of typically 60nA. The device contains special circuitry to achieve just 120nA IQ in 100% mode to further extend battery life near the end of discharge. With an input voltage of 1.8V to 6.5V, the device supports multiple power sources such as 2S to 4S Alkaline, 1S to 2S Li-MnO2, or 1S Li-Ion/Li-SOCl2. These devices are well-designed for many battery powered applications, such as smart meters, medical sensor patches, industrial IoT (smart sensors) and other test and measurement equipment. The analog signal chain in such applications often requires symmetrical supply voltage or negative voltage biasing. The TPS6284x can be configured in an inverting buck-boost topology, where the output voltage is inverted or negative with respect to ground. This application report describes the inverting buck-boost topology in detail for the TPS6284x family.

> **Note**
>
> Precautions need to be taken when using these devices in an inverting buck-boost topology. Please review section Section 2 to understand and robustly eliminate known risk.

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1 Inverting Buck-Boost Topology

1.1 Concept

The inverting buck-boost topology is very similar to the buck topology. In a standard buck configuration, shown in Figure 1-1, the positive connection (V_{OUT}) is connected to the inductor and the return connection is connected to the device ground.
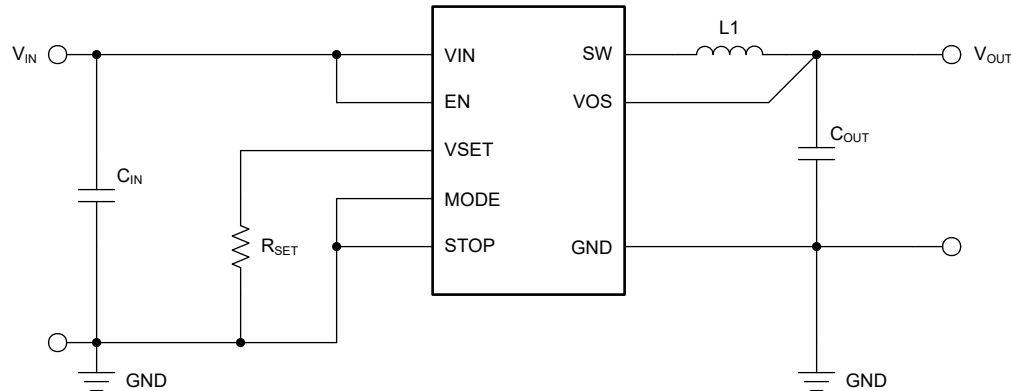

Figure 1-1. Buck Topology

However, in the inverting buck-boost configuration illustrated in Figure 1-2, the device ground is used as the negative output voltage pin (labeled as V_{OUT}). What was previously the positive output in the buck configuration is now used as the ground (GND). This shift in topology allows the output voltage to be inverted and always remain lower than the ground.
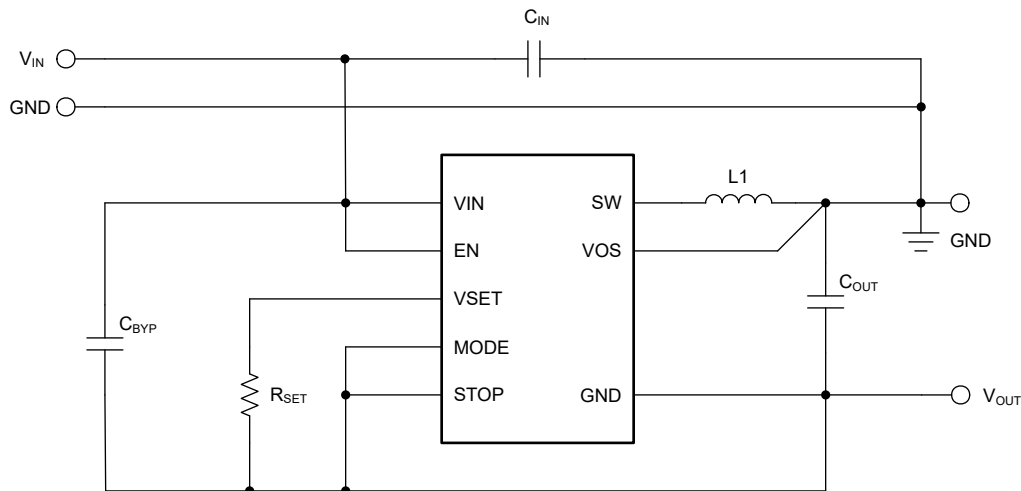

Figure 1-2. Inverting Buck-Boost Topology

The circuit operation in the inverting buck-boost topology differs from that in the buck topology. Though the components are connected the same as with a buck converter, the output voltage terminals are reversed, as Figure 1-3 shows. During the *on* time of the control MOSFET, shown in Figure 1-4, the inductor is charged with current, while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the *off* time of the control MOSFET and the *on* time of the synchronous MOSFET, shown in Figure 1-5, the inductor provides current to the load and the output capacitor. These changes affect many parameters, as discussed in the Design Considerations section.
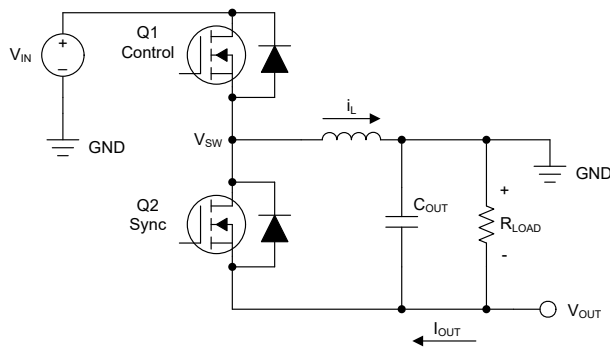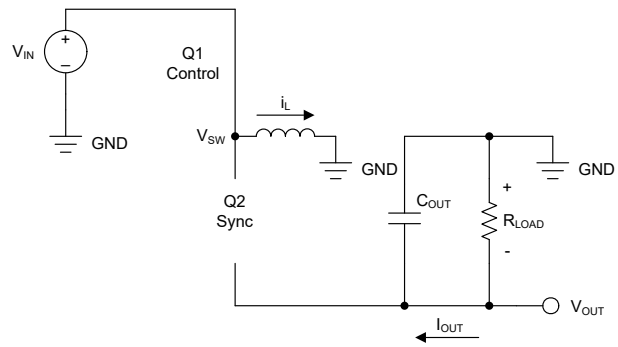
Figure 1-3. Buck-Boost Configuration

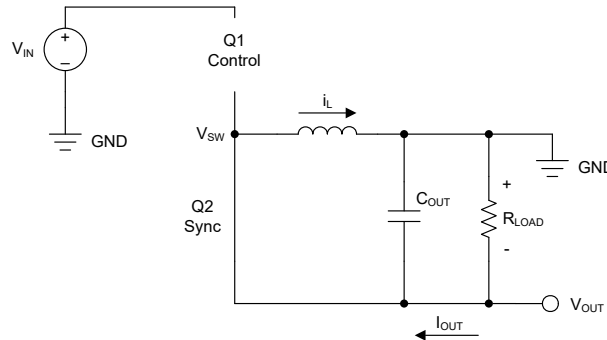**Figure 1-4. Buck-Boost On Time**

Figure 1-5. Buck-Boost Off Time

1.2 Output Current Calculations

The average inductor current is also affected in this topology. In the buck configuration, the average inductor current is equal to the average output current because the inductor always supplies current to the load during both the *on* and *off* times of the control MOSFET. However, in the inverting buck-boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the *on* time of the control MOSFET. During the *off* time, the inductor connects to both the output capacitor and the load (see Figure 1-5). Knowing that the *off* time is (1 – D) of the switching period, Equation 1 can be used to calculate the average inductor current:

$$I_{L(Avg)} = \frac{I_{OUT}}{(1 - D)} \tag{1}$$

The operating duty cycle for an inverting buck-boost converter can be found with Equation 2:

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN}) \times \eta} \tag{2}$$

Rather than V_{OUT}/V_{IN} for a buck converter. The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. The peak-to-peak inductor ripple current is given by Equation 3:

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} \tag{3}$$

where:

- ΔI_L (A): the peak-to-peak inductor ripple current
- D: duty cycle
- η: efficiency
- f_S (MHz): switching frequency
- L (µH): inductor value

- V_{IN} (V): the input voltage with respect to ground, not with respect to the device ground or V_{OUT}

Equation 4 calculates the maximum inductor current:

$$I_L = I_{L(avg)} + \frac{\Delta I_L}{2} \tag{4}$$

For example, for an output voltage of –1.8V, 2.2µH inductor, and input voltage of 3.3V, the following calculations produce the maximum allowable output current that can be achieved based on the TPS62840 minimum current limit value of 1A. The efficiency term is estimated at 80 %.

$$D = \frac{V_{OUT}}{(V_{OUT} - V_{IN}) \times \eta} = \frac{-1.8\ V}{(-1.8\ V - 3.3\ V) \times 0.8} = 0.441 \tag{5}$$

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} = \frac{3.3\ V \times 0.441}{1.8\ MHz \times 2.2\ \mu H} = 368\ mA \tag{6}$$

Rearranging Equation 4 and setting $I_{L(max)}$ equal to the minimum value of I_{LIMF}, as specified in the data sheet, gives:

$$I_{L(avg)} = I_{L(max)} - \frac{\Delta I_L}{2} = 1000\ mA - \frac{368\ mA}{2} = 816\ mA \tag{7}$$

This result is then used in Equation 1 to calculate the maximum achievable output current:

$$I_{OUT} = I_{L(avg)} \times (1 - D) = 816\ mA \times (1 - 0.441) = 456\ mA \tag{8}$$

Table 1-1 provides several examples of the calculated maximum output currents for different output voltages (–1.8V, –1.5V and –1.2V) based on an inductor value and switching frequency of 2.2µH and 1.8MHz, respectively. Increasing the inductance and/or input voltage allows higher output currents in the inverting buck-boost configuration. The maximum output currents for the TPS62840 in the inverting buck-boost topology are frequently lower than 750mA due to the fact that the average inductor current is higher than that of a typical buck. The output current for the same three output voltages and different input voltages is displayed in Figure 1-6.

Table 1-1. Maximum Output Current Calculation for Different Values of V_{OUT}

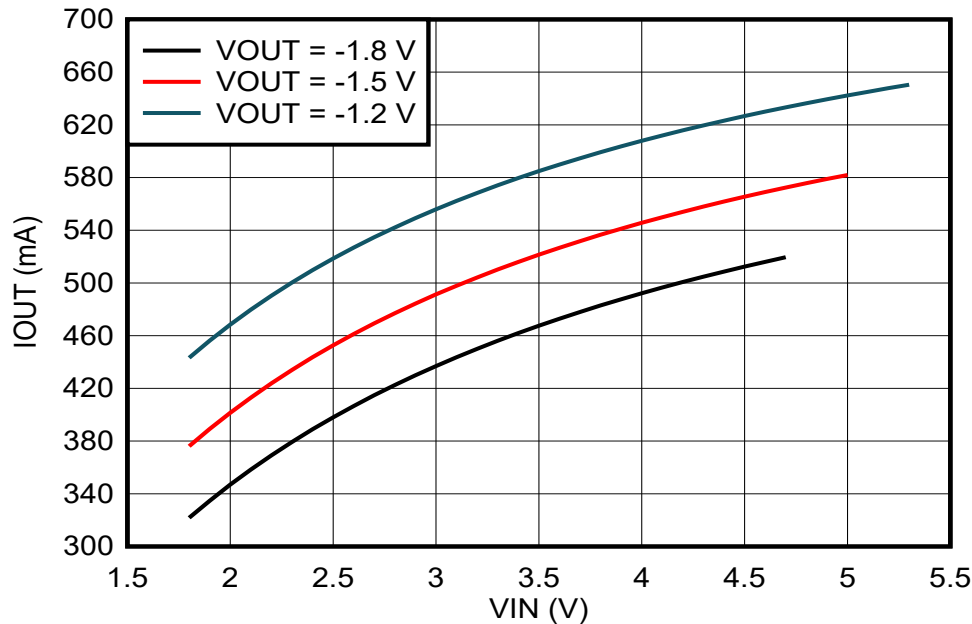| Parameter	VOUT = -1.8V	VOUT = -1.5V	VOUT = -1.2V
V_{IN} (V)	3.3	3.3	3.3
η	0.8	0.8	0.8
f_s (MHz)	1.8	1.8	1.8
L (µH)	2.2	2.2	2.2
$I_{L(max)}$ (mA)	1000	1000	1000
D	0.441	0.391	0.333
ΔI_L (mA)	368	326	278
$I_{L(avg)}$ (mA)	816	837	861
I_{OUT} (mA)	456	510	574

Figure 1-6. Maximum Output Current versus V$_{IN}$

1.3 V$_{IN}$ and V$_{OUT}$ Range

The input voltage that can be applied to an inverting buck-boost converter IC is less than the input voltage that can be applied to the same buck converter IC. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V$_{IN}$ to V$_{OUT}$, not V$_{IN}$ to ground. Thus, the input voltage range of the TPS6284x is 1.8V to 6.5V + V$_{OUT}$, where V$_{OUT}$ is a negative value. The output voltage range is the same as when configured as a buck converter, but negative. The output voltage for the inverting buck-boost topology can be set the same way as in the buck configuration, with the R$_{SET}$ resistor connected to the device GND pin.

2 Design Considerations

2.1 Additional Input Capacitor

An additional input capacitor, C$_{BYP}$, is required for stability as a bypass capacitor for the device. This capacitor is in addition to the input capacitor, C$_{IN}$, from V$_{IN}$ to ground (refer to Figure 1-2). The recommended minimum value for the bypass capacitor and the input capacitor is 4.7µF. As a side effect, the C$_{BYP}$ capacitor provides an AC path from V$_{IN}$ to V$_{OUT}$ and together with C$_{OUT}$ a capacitive voltage divider is build against GND. In the moment when V$_{IN}$ is applied to the circuit, the capacitive voltage divider is pulling up V$_{OUT}$ above GND, which is causing a positive prebias of the negative rail. This also means the IC GND pin (connected to V$_{OUT}$) is also prebiased positive, which is pulling SW pin and VOS pin more than 0.3V below IC ground, violating the absolute maximum rating. Such a condition can damage the device and is not recommended. Therefore, a Schottky diode (D1) has to be installed on the output, per Figure 2-1. Startup testing needs to be conducted to verify that the VOS pin is not driven more than 0.3V below IC ground when V$_{IN}$ is applied.
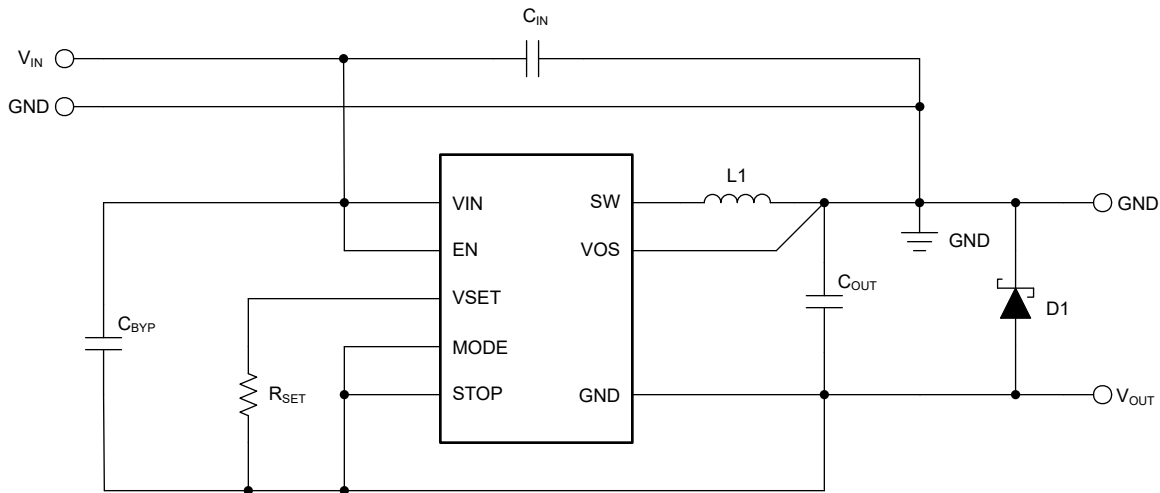
Figure 2-1. Inverting Buck-Boost Topology With Schottky Diode

The AC path through C_{BYP} can also worsen the line transient response. If strong line transients are expected, the output capacitance can be increased to keep the output voltage within acceptable levels during the line transient.

The TPS6284x can operate without the bypass capacitor and without Schottky diode, but care must be taken to verify stability in the individual application and to check that the SW and VOS pin signals do not violate the recommended operating conditions during startup.

2.2 Digital Input Pin Configurations

Because V_{OUT} is the IC ground in this configuration, the EN pin must be referenced to V_{OUT} instead of the ground. In a buck configuration, the specified threshold voltage for the enable pin in the product data sheet is 1.1V to be considered high and 0.4V to be considered low (see the TPS62840 product data sheet). In the inverting buck-boost configuration, however, the V_{OUT} voltage is the reference; therefore, the high threshold is 1.1V + V_{OUT} and the low threshold is 0.4V + V_{OUT}. For example, if V_{OUT} = -1.8V, the V_{EN} is considered a high level for voltages above –0.7V and a low level for voltages below –1.4V. The same effect is true with the MODE and STOP pins. This behavior can cause difficulties enabling or disabling the part, since in some applications, the IC providing the EN signal cannot produce negative voltages. The level shifter shown in Figure 2-2 alleviates any problems associated with the offset EN threshold voltages by eliminating the need for negative EN signals.
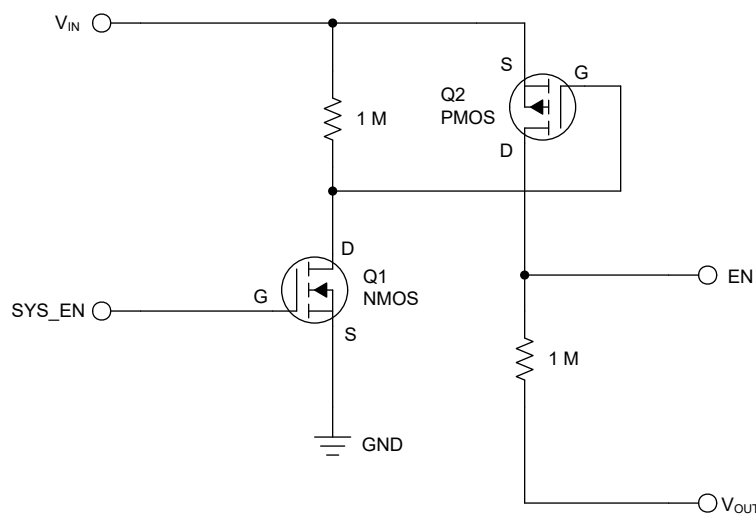

Figure 2-2. EN Pin Level Shifter

The positive signal that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN grounded), Q2 sees 0V across the VGS, and also remains off. In this state, the EN pin sees VOUT which is

below the low level threshold and disables the device. When SYS_EN provides enough positive voltage to turn Q1 on (minimum VGS as specified in the MOSFET's data sheet), the gate of Q2 is pulled low through Q1. This drives the VGS of Q2 negative and turns Q2 on. As a consequence, VIN ties to EN through Q2 and the pin is above the high level threshold, causing the device to turn on. Make sure that the VGD of Q2 remains within the MOSFET's ratings during both enabled and disabled states. Failing to adhere to this constraint can result in damaged MOSFETs. The enable and disable sequence is illustrated in Figure 2-3 and Figure 2-4. The SYS_EN signal activates the enable circuit, and the G/D NODE signal represents the shared node between Q1 and Q2. The EN signal is the output of the circuit and goes from VIN to –VOUT properly enabling and disabling the device.
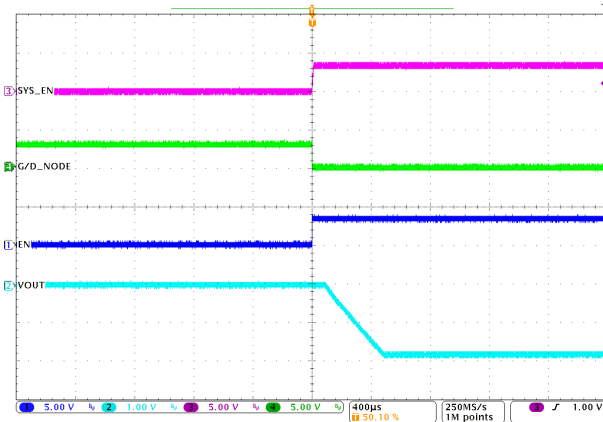
Figure 2-3. EN Pin Level Shifter on Startup
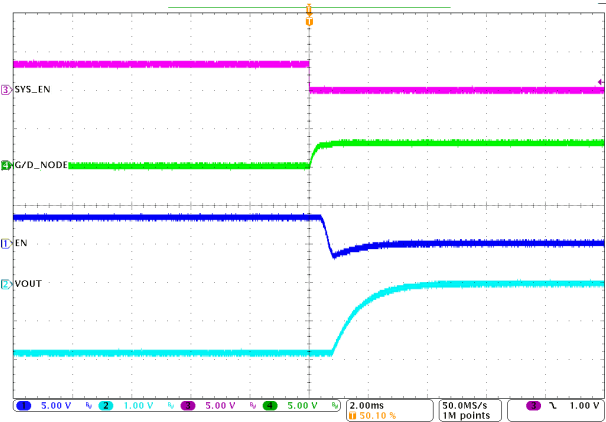
Figure 2-4. EN Pin Level Shifter on Shutdown

2.3 Startup Behavior and Switching Node Consideration

In the inverting buck-boost topology, the voltage on the SW pin switches from VIN to VOUT, instead of from VIN to GND. As the high-side MOSFET turns on, the SW node sees the input voltage; as the low-side MOSFET turns on, the SW node sees the device ground, which is the output voltage. During startup, VIN rises to achieve the desired input voltage. VOUT starts ramping down after the EN pin voltage exceeds the threshold level and VIN exceeds the UVLO threshold. As VOUT continues to ramp down, the SW node low level follows VOUT down. Figure 2-5 shows the resulting normal and smooth startup of the output voltage.
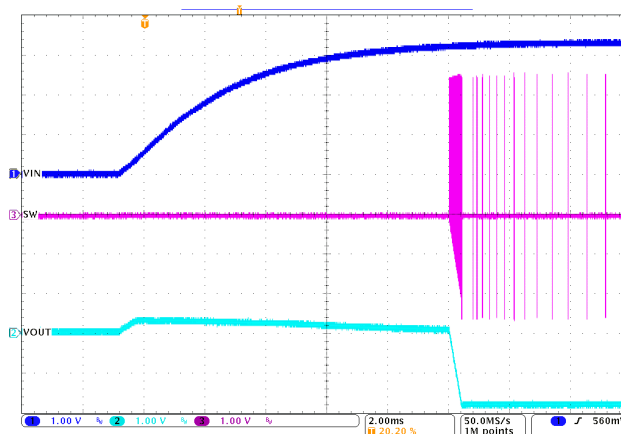
Figure 2-5. SW Node Voltage During Startup

3 External Component Selection

The inductor and output capacitor must both be selected based on the requirements of the application and the stability criteria of the device, which are different from the traditional buck converter approach. A load transient test needs to be performed to evaluate stability. Figure 4-7 shows the results of such a test performed on the example circuit. The lack of ringing indicates stability.

3.1 Inductor Selection

To select the inductor value for the inverting buck-boost topology, use Equation 1 through Equation 4 instead of the equations provided in the TPS62840 data sheet. These formulas help to select the proper inductance by designing for a maximum inductor current ($I_{L(Max)}$) or finding the peak inductor current for a given inductance. $I_{L(Max)}$ needs to be kept below the device minimum current limit value for a reliable design. The worst-case $I_{L(Max)}$ occurs at the minimum V_{IN} for a given design. Once $I_{L(Max)}$ is determined, the recommendation is to choose an inductor with a saturation rating 20 % to 30 % higher than $I_{L(Max)}$ to allow for peak currents that can occur during startup or load transients. For the inverting buckboost topology, the recommended inductance is 2.2µH.

3.2 Capacitor Selection

Tiny ceramic capacitors with low equivalent series resistance (ESR) are desired to have low output voltage ripple. X5R- or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics. A minimum 10µF capacitor is recommended for both C_{BYP} and C_{IN}. These capacitance values can be increased without limit. For the output capacitor, a minimum of 22µF is recommended. Making this capacitor value too great can cause instability. This situation can be evaluated through a Bode plot or load transient response. The voltage rating of C_{BYP} must be greater than (V_{IN} + V_{OUT}).

4 Typical Performance

The reference design with V_{OUT} = -1.8V, as shown in Figure 4-1 was used to generate the typical characteristic graphs presented in this section and shown in Figure 4-2 through Figure 4-9.
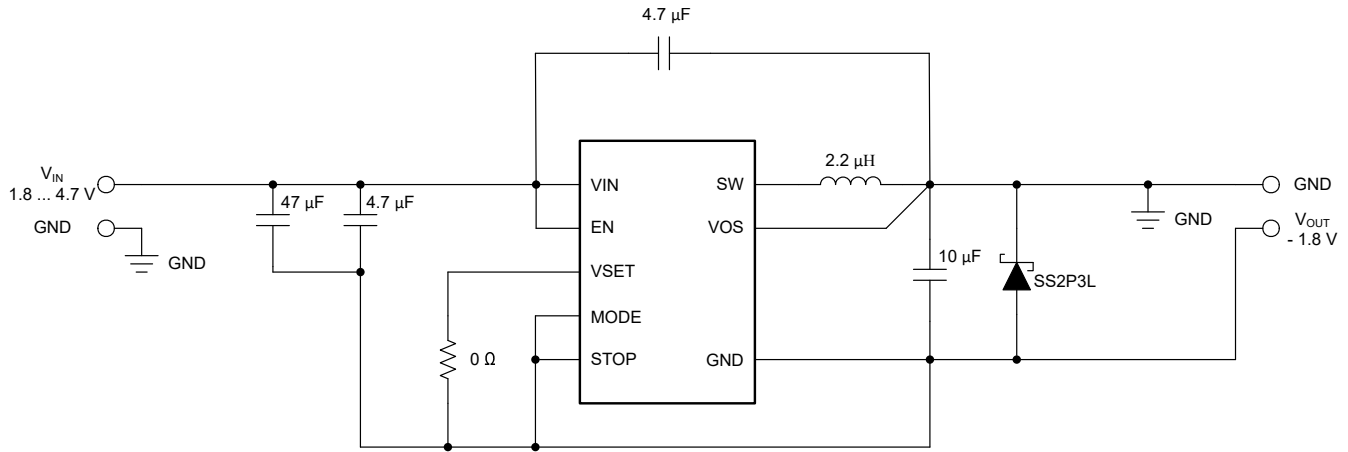

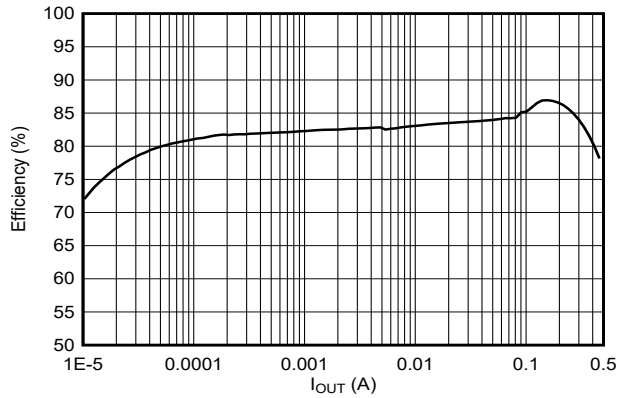**Figure 4-1. Schematic of the Tested Circuit**

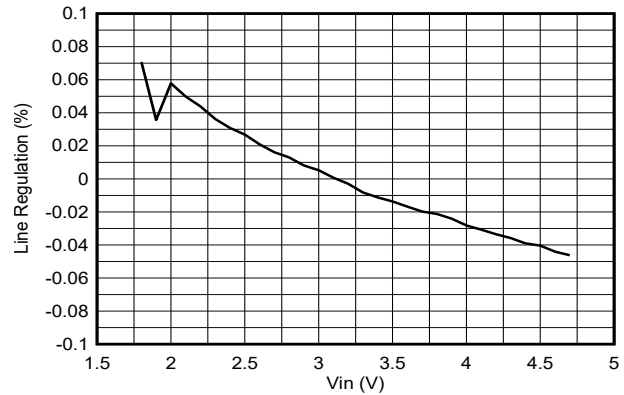**Figure 4-2. Efficiency vs Load Current with V_{IN} = 3.3V, V_{OUT} = 1.8V**
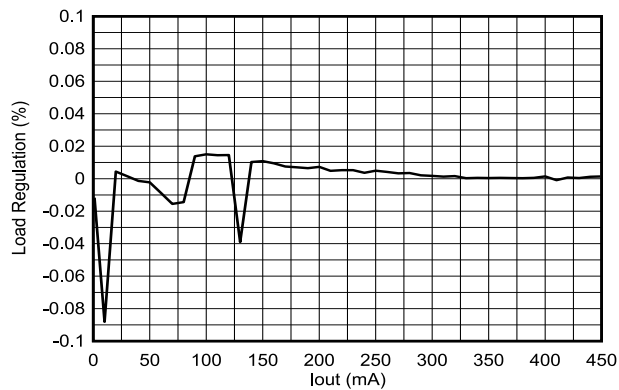

Figure 4-3. Line Regulation at 320mA Load

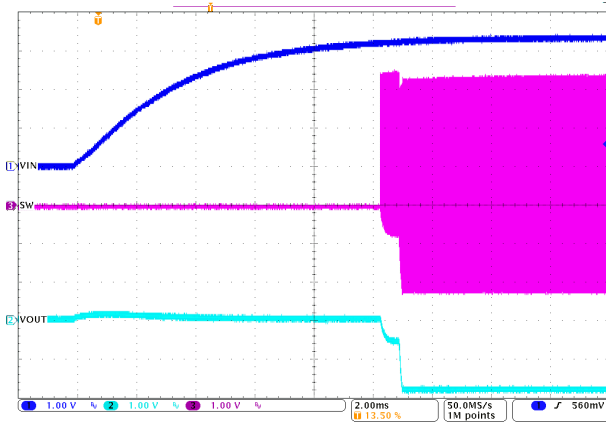**Figure 4-4. Load Regulation at V_{IN} = 3.3V, V_{OUT} = -1.8V**

Figure 4-5. Startup on V$_{IN}$ at 450mA Load, V$_{IN}$ = 3.3V, V$_{OUT}$ = -1.8V
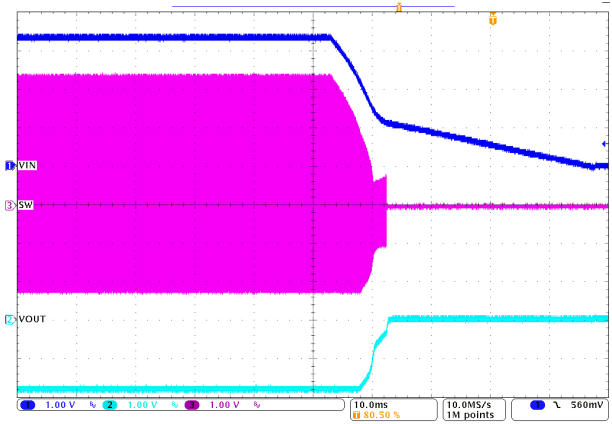
Figure 4-6. Shutdown on V$_{IN}$ at 450mA Load, V$_{IN}$ = 3.3V, V$_{OUT}$ = -1.8V
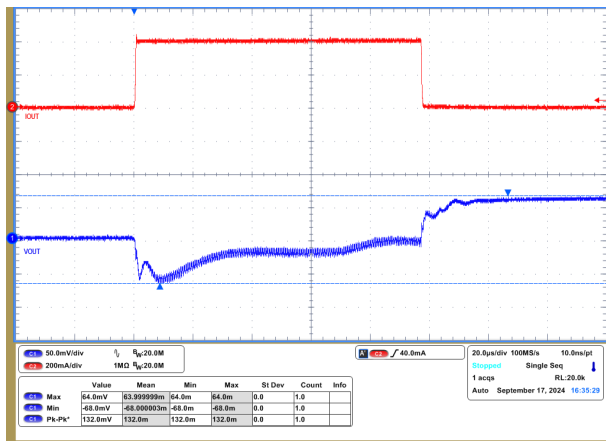
Figure 4-7. Load Transient Response, 0mA to 400mA at 1A/µs With V$_{IN}$ = 3.3V, V$_{OUT}$ = -1.8V
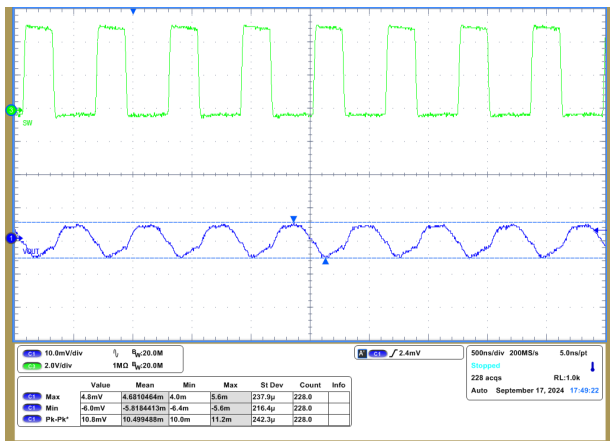
Figure 4-8. Output Voltage Ripple, V$_{IN}$ = 3.3V, V$_{OUT}$ = -1.8V and I$_{OUT}$ = 450mA
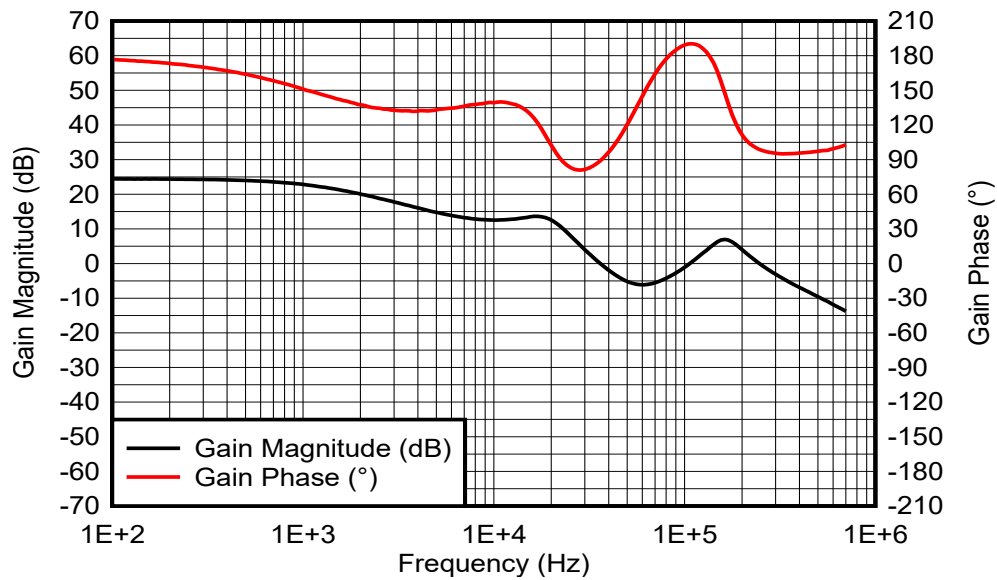
Figure 4-9. Bode Plot at V$_{IN}$ = 3.3V, V$_{OUT}$ = -1.8V and 450mA Load

5 Summary

The TPS62840 buck dc-to-dc converter can be configured as an inverting buck-boost converter to generate a negative output voltage. The inverting buck-boost topology changes some system characteristics, such as input voltage range and maximum output current. This application report explains the inverting buck-boost topology and how to select the proper values of external components with the changed system characteristics. TPS62840 also gives design guidelines and precautions to make sure the robust operation of the converter. Measured data from the example design are provided. This application report also applies to any of the devices in the TPS6284x family.

6 References

1. Texas Instruments, *Using the TPS6215x in an Inverting Buck-Boost Topology*, application note.
2. Texas Instruments, *TPS62840 1.8-V to 6.5-V, 750-mA, 60-nA IQ Step-Down Converter*, data sheet.

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