Application Note

Enhancing Server Power Design Using Advanced Features of TI's Smart eFuses

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ABSTRACT

This application note explains and demonstrates two different over-current protection mechanisms that the different eFuse devices provide. One is called current-limit, and another is circuit-breaker. Using experimental results, this article also discusses the limitations of the current-limit-based over-current protection in enterprise server applications, where the power delivery system is exposed to high slew-rate, high frequency, and high amplitude load transients. The limitations of the approach as mentioned above are solved through the circuit-breaker mechanism along with a programmable over-current blanking timer in TI's high-current eFuse family of devices. This design is discussed in this application note through experimental results. The system-level benefits of using TI's high-current eFuse design over the conventional eFuse devices available in the market are also discussed.

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1 Introduction

A typical power tree of an enterprise server motherboard is shown in Figure 1-1. With the advancement of artificial intelligence and machine learning, graphics processing units (GPUs) are becoming more and more power-hungry over time and demand high slew-rate and amplitude current pulses to improve the processor computation speed. Figure 1-2 depicts a typical load transient profile seen at the 12V bus (50A to 110A load transient) while applying a load transient of 300A for 8ms to 675A for 2ms and then 300A for 8ms (as per Intel® Birch Stream server platform) at the output of VRM with 1.8V. To support these load transients at the output of the voltage regulator modules (VRMs), the power stages of the VRMs have to draw the pulse currents from the input power supply unit (PSU) as the input and output filters of the VRMs are unable to support these high-frequency load transients. As shown in Figure 1-1, the input power path protection devices, eFuses are placed in between the PSU and the power stages of VRMs for inrush current management and protecting the PSUs and the VRMs against different faults, such as input under-voltage, input over-voltage, power up into output short, over-current, output hot-short, etc. The over-current protection mechanism needs to be implemented inside the eFuses so that these devices can protect the system against a persistent over-current fault whereas the transient peak current pulses of a certain amplitude and duration must be allowed to pass through.

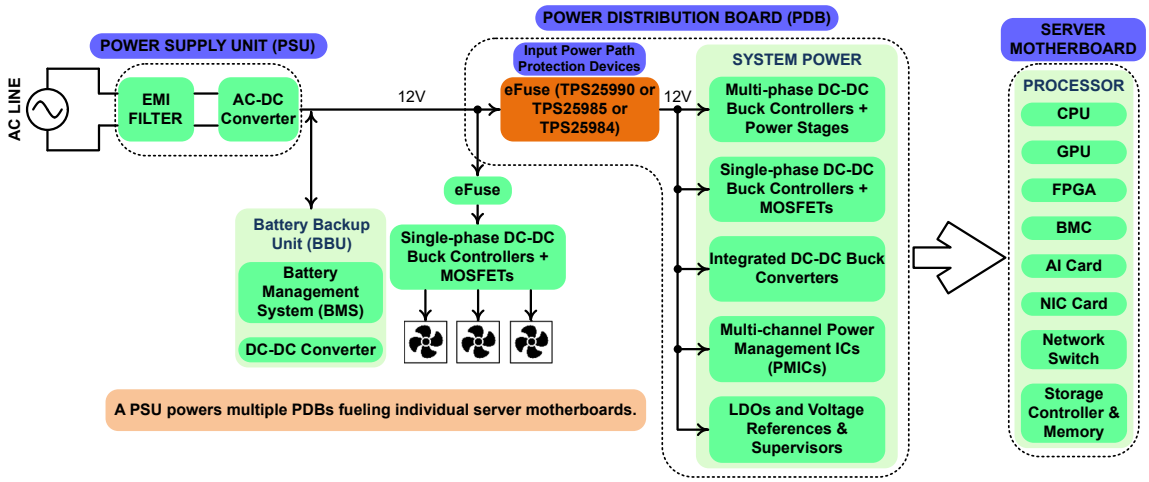

Figure 1-1. Enterprise Server Power Block Diagram

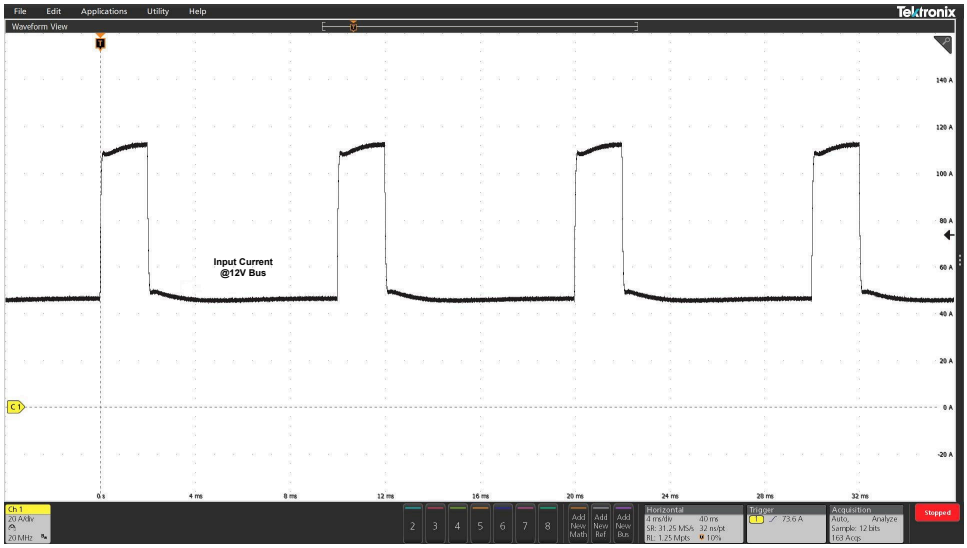

Figure 1-2. A Typical Load Transient Profile Seen at the 12V Bus Powering a VRM with 1.8V Output

2 Over-Current Response of Conventional eFuse Devices

The conventional eFuse devices continuously monitor the current flowing through it and provide a current output to a particular pin. Connecting an appropriate resistance to this pin generates a voltage, which is linearly proportional to the current flowing through the device. This voltage is compared with a reference voltage to detect an output over-current event. The reference voltage is user-configurable. Once the current sense voltage (configured via an external resistor) exceeds the current limit reference voltage threshold, the internal circuitry regulates its gate to maintain a constant current on the MOSFET and an internal fault timer (not user-configurable) starts. The device resumes normal operation if the load current drops below the current limit set point within the fixed fault timer period. Otherwise, the device is turned off in the event of a persistent over-current event. The over-current responses of two conventional eFuses are shown in Figure 2-1 and Figure 2-2.

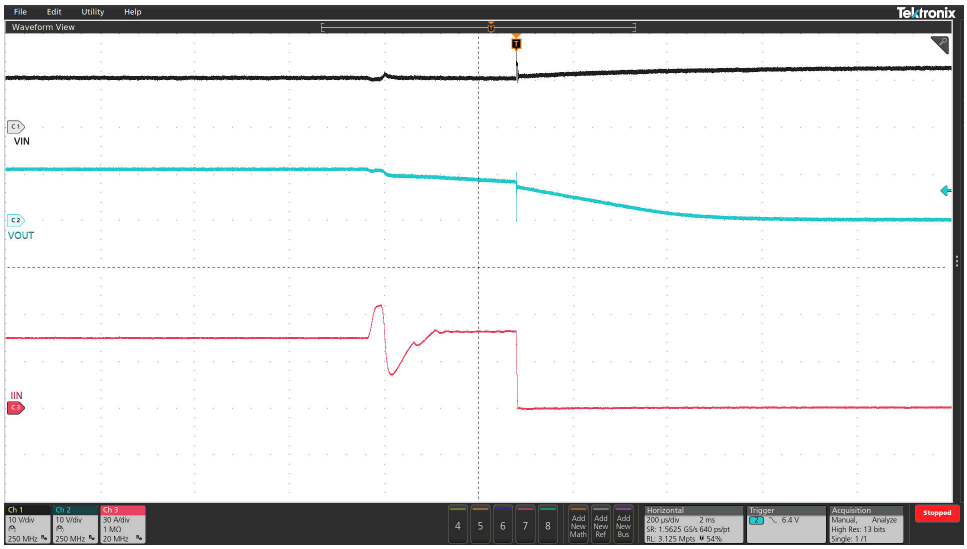

Figure 2-1. Over-Current Response of the Conventional eFuse-1

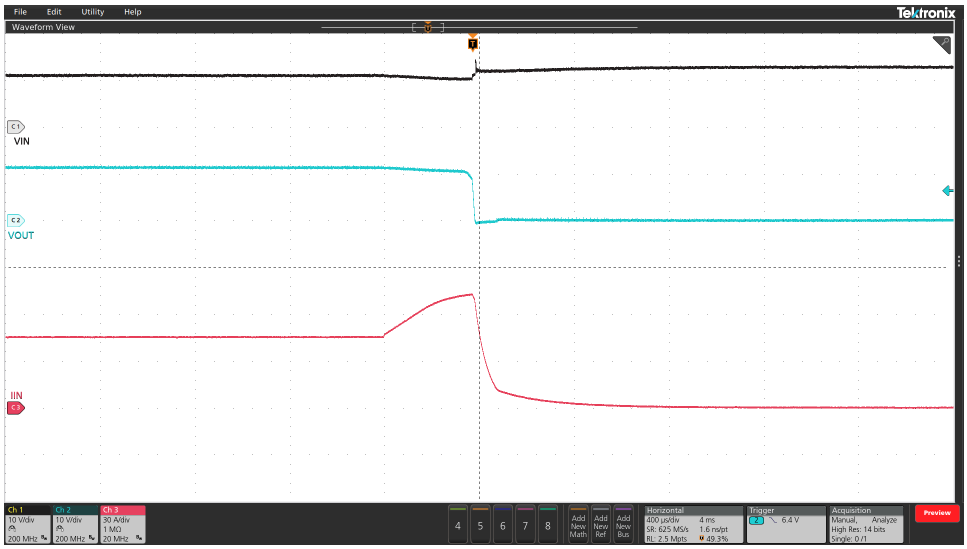

Figure 2-2. Over-Current Response of the Conventional eFuse-2

3 Challenges with Current Limit Functionality

The over-current response of the conventional eFuses is the current-limit, which means the device current is limited to the current-limit threshold for a user-defined or a fixed fault timer interval. Generally, the over-current protection (OCP) threshold is set at around 1.1-1.2 times the thermal design current (TDC) to protect the complete server power delivery systems and the PSU from the thermal runway due to excessive overheating. If the current amplitudes of the load transients are more than the OCP threshold, the devices mentioned above do not allow the flow of that transient current into the load from the supply as it gets limited. The solution is to set the OCP threshold beyond the maximum amplitude of the transient pulse current to avoid the device's false turn-off in the presence of the load transients. This behavior in one of the conventional eFuses is demonstrated in Figure 3-1 and Figure 3-2. In both cases, a load transient of 100A for 12ms to 160A for 12ms and then back to 100A is applied. However, the OCP threshold is set at 120A in Figure 3-1, 1.2 times the steady-state current of 100A. As the amplitude of the load transient (160A) is more than the OCP threshold of 120A, the devices are turned off. Also, the OCP threshold is set at 170A in Figure 3-2, which is more than the load transient magnitude of 160A. Therefore, the load transients of 100A for 12ms to 160A for 12ms and then back to 100A pass through.

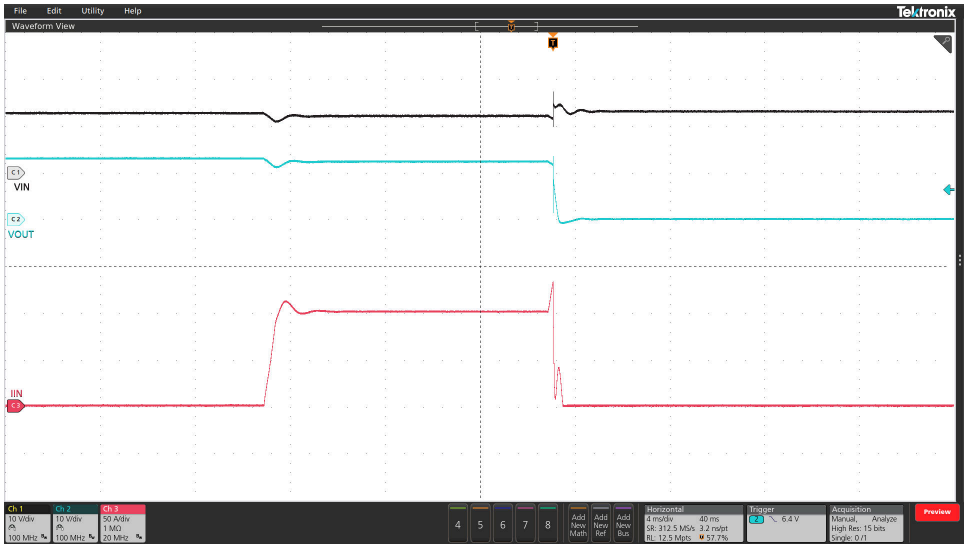

Figure 3-1. Conventional eFuse-1: Load Transient of 100A for 12ms to 160A for 12ms and Then Back to 100A With OCP Threshold of 120A

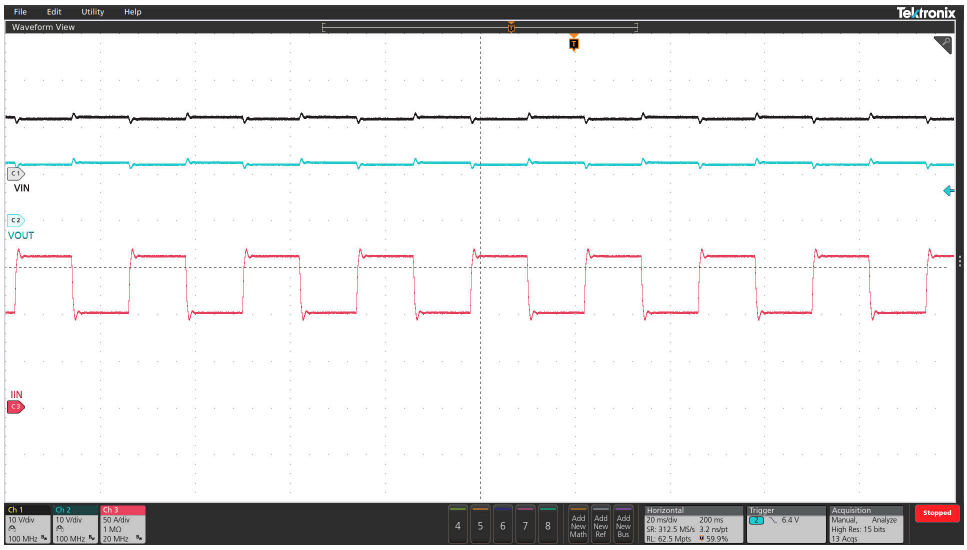

Figure 3-2. Conventional eFuse-1: Load Transient of 100A for 12ms to 160A for 12ms and Then Back to 100A With OCP Threshold of 170A

However, there is a challenge in increasing the OCP threshold more than the peak pulse current level as outlined in the following. Increasing the OCP threshold beyond the transient peak pulse current level instead of setting it at 1.1-1.2 times the TDC level makes the input power path not have any over-current protection till the peak pulse current level although it is a transient load. Therefore, the input PSU and the power distribution systems of the server motherboard have to be designed for a continuous current rating of transient peak pulse current instead of TDC. This increases the overall system cost and solution size as each power component must be rated for a much higher current rating or more power components need to be in parallel. This is required to handle the system's increased current rating. The system utilization also becomes poor as the system is designed for a current rating of transient peak pulse current but is used at the level of TDC for a duty cycle of more than 90%. The steady-state power rating of the input PSU has to correspond to the transient peak pulse current instead of TDC as there is no over-current protection till the current level of the transient peak pulse current.

4 Proposed Design Using TI's High-Current eFuses

4.1 Steady-State Over-Current Protection in TPS25984, TPS25985, TPS25990, and TPS1685 eFuses

The TPS25984, TPS25985, TPS25990, and TPS1685 eFuses respond to output over-current conditions during steady-state by performing a circuit-breaker action after a user-adjustable transient fault blanking interval. This action allows the device to support a higher peak current for a short user-defined interval but also makes sure of robust protection in case of persistent output faults.

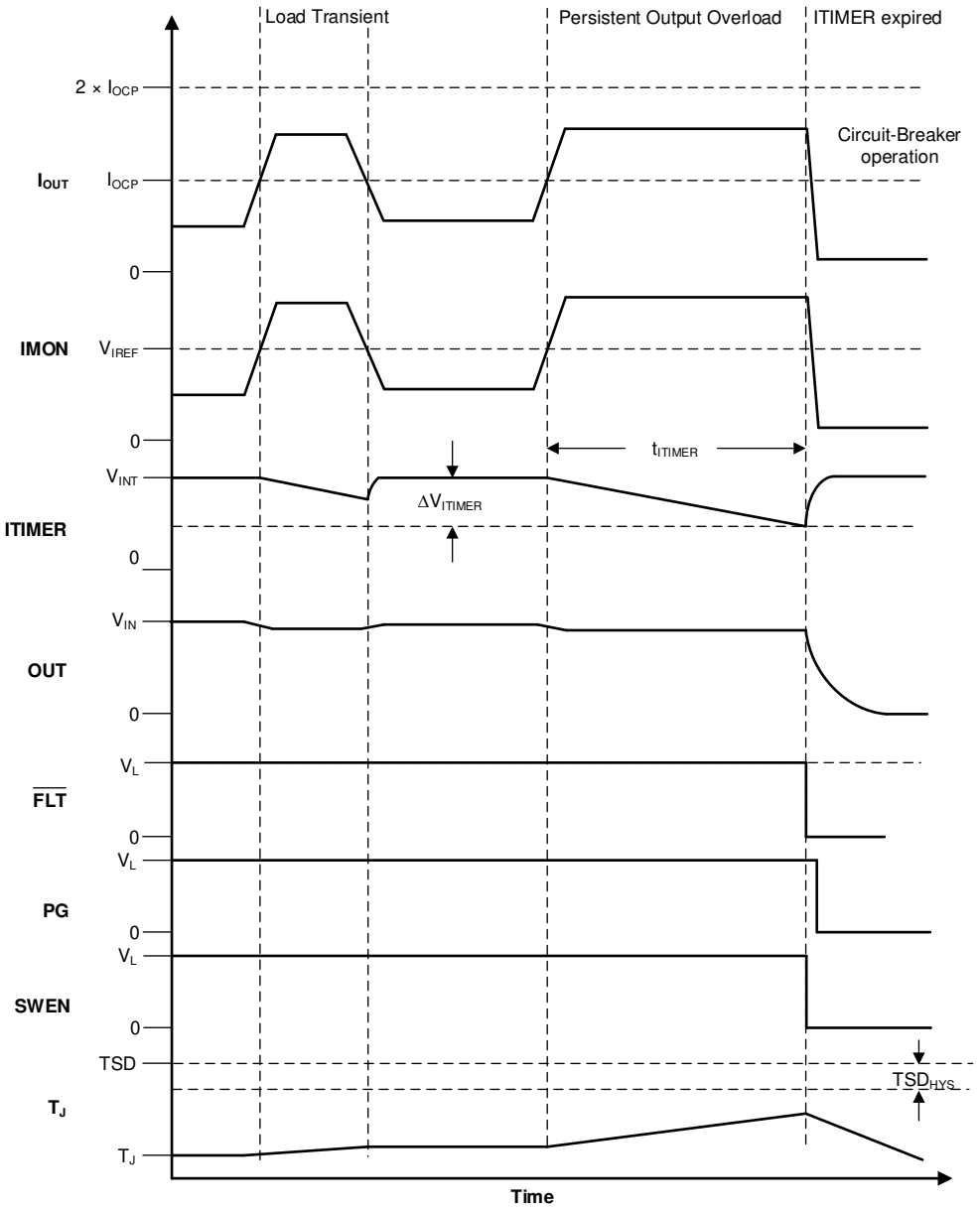

Figure 4-1. Steady-State Over-current (Circuit-Breaker) Response

The device constantly senses the output load current and provides an analog current output (I_{IMON}) on the IMON pin, which is proportional to the load current. This in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) as per Equation 1.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \quad (1)$$

Where G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT})

The over-current condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) sets the over-current protection threshold (I_{OCP}) accordingly.

- In the standalone or primary mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage. It is also possible to drive the IREF pin from an external low impedance reference voltage source as shown in Equation 2.

$$V_{IREF} = I_{IREF} \times R_{IREF} \quad (2)$$

- In a primary and secondary parallel configuration, the primary eFuse or controller drives the voltage on the IREF pin to provide an external reference (V_{IREF}) for all the secondary devices in the chain.

The over-current protection threshold during steady-state (I_{OCP}) can be calculated using Equation 3.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \quad (3)$$

After an over-current condition is detected, that is the load current exceeds the programmed current limit threshold (I_{OCP}), but stays lower than the scalable short-circuit threshold (I_{SFT}) of 2 × I_{OCP}, the device starts discharging the ITIMER pin capacitor using an internal pull-down current (I_{TIMER}) of ~ 2.0µA. If the load current drops below the circuit-breaker threshold before the ITIMER capacitor discharges by ΔV_{ITIMER} of 1.5V (typical), the ITIMER is reset by pulling it up to V_{INT} of 3.65V (typical) internally and the circuit-breaker action is not engaged. This action allows short overload transient pulses to pass through the device without tripping the circuit. If the over-current condition persists, the ITIMER capacitor continues to discharge and after it falls by ΔV_{ITIMER}, the circuit-breaker action turns off the device immediately. At the same time, the ITIMER cap is charged up to V_{INT} again immediately so that it is at its default state before the next over-current event. This action makes sure the full blanking timer interval is provided for every over-current event. Equation 4 can be used to calculate the R_{IMON} value for the desired over-current threshold.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP}} \quad (4)$$

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient over-current blanking interval can be calculated using Equation 5.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \quad (5)$$

Figure 4-1 illustrates the over-current response for TPS25984, TPS25985, TPS25990, and TPS1685 eFuses. After the part shuts down due to a circuit-breaker fault, the part either stays latched off (latch-off variant) or restarts automatically after a fixed delay (auto-retry variant).

Figure 4-2 and Figure 4-3 represent the responses of TPS25990 eFuse to a transient overload event and a persistent overload event.

Figure 4-2: Device in steady-state, Load current ramped up from 50A to 70A for 10ms and then ramped down to 50A. OCP threshold set to 55A, Over-current blanking delay set to 15ms (OC_TIMER = 0x89)

Figure 4-3: Device in steady-state, Load current ramped up from 50A to 70A for > 15ms. OCP threshold set to 55A, Over-current blanking delay set to 15ms (OC_TIMER = 0x89)

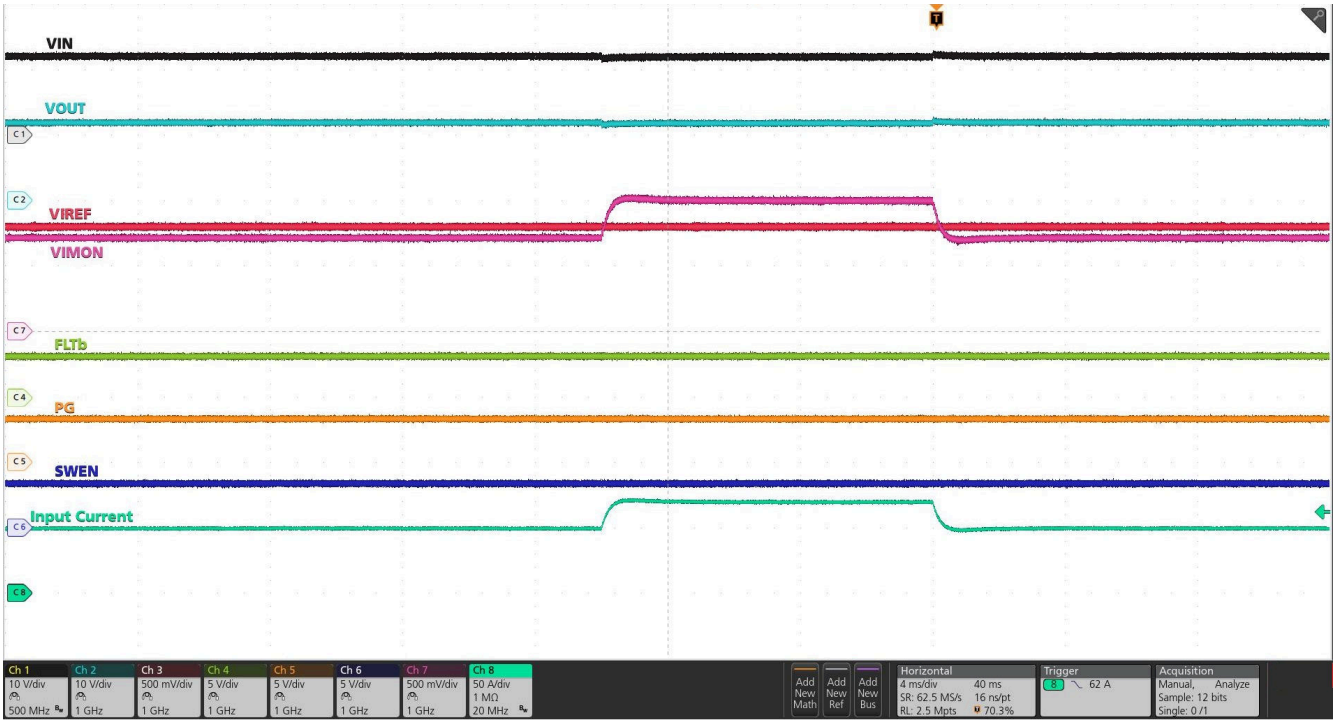

Figure 4-2. Transient Over-Current Blanking in TPS25990 eFuse

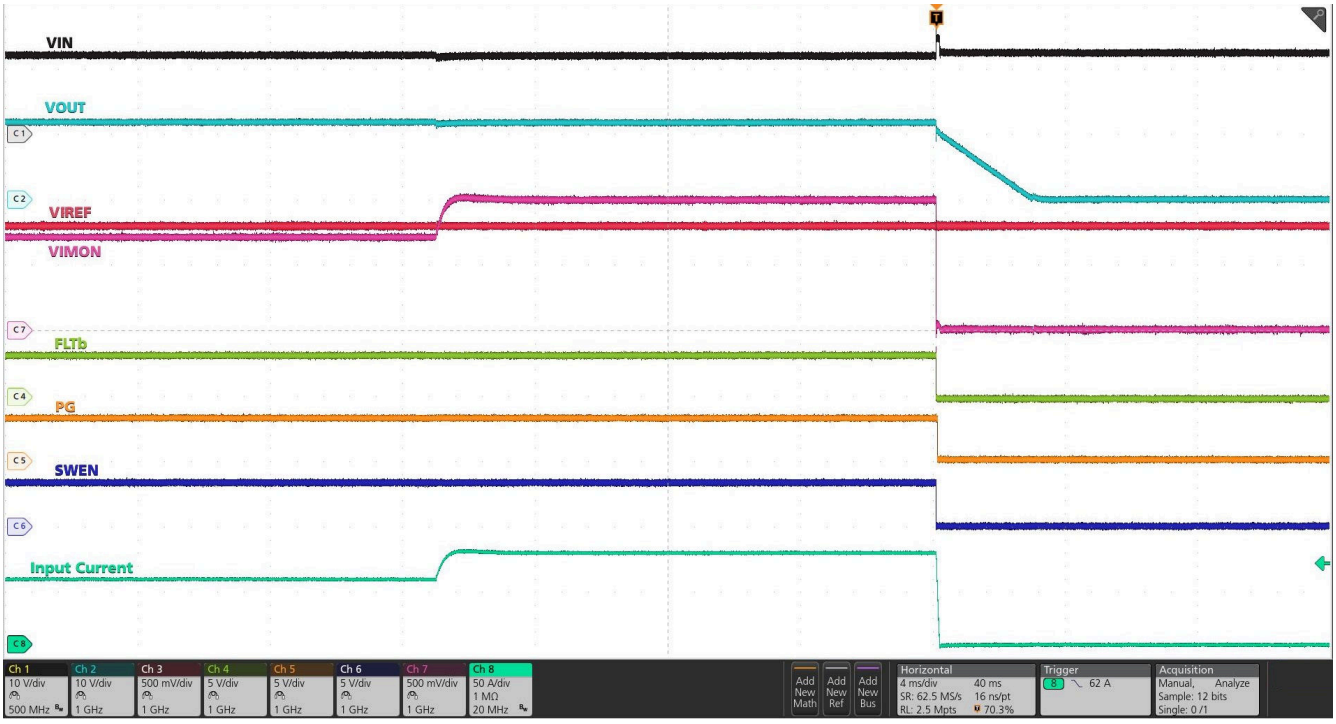

Figure 4-3. Over-current Protection in TPS25990 eFuse

4.2 Design Guideline

1. Decide the following parameters,
   a. Thermal design current (TDC) or continuous maximum steady-state current,
   b. Maximum amplitude (IMAX) of the transient peak pulse current,
   c. Maximum duration of the transient peak pulse current,
2. Set the scalable fast-trip threshold (I_{SFT}) at around 1.2 times IMAX to allow the transient load current to flow,

3. The over-current threshold (I_{OCP}) is a fraction of I_{SFT} as depicted in Equation 6.

$$I_{OCP} = k \times I_{SFT} \quad (6)$$

   By default, the value of k is 0.5 in TPS25984, TPS25985, TPS25990, and TPS1685 eFuses. However, it is user-programmable in TPS25990 and TPS1685 eFuses through PMBus and pin strapping respectively. Afterword, the value of R_{IMON} resistance is obtained using Equation 4 and considering the actual value of k.
4. The fault timer duration needs to be set at more than the maximum duration of the transient load current pulse whose amplitude is greater than I_{OCP}. The maximum possible fault timer duration is around 30ms. The fault timer duration is PMBus programmable in TPS25990 and hardware programmable in the other three eFuses by placing a ceramic capacitor on the ITIMER pin. The value of the capacitor is obtained using Equation 5.
5. The number of eFuses in parallel needs to be calculated based on the RMS current rating of the device and the RMS value of the total system current or the TDC rating.

5 Thermal Performance with Continual Transient Load Current

In the presence of transient load current, the device junction temperature rise is proportional to the square of the root mean square (RMS) current flowing through it instead of the average DC current. The junction temperature is obtained using Equation 7.

$$T_J = T_A + \left(I_{RMS}^2 \times R_{DSon} \times R_{\theta JA}\right) \quad (7)$$

T_J: Device junction temperature,

T_A: Device ambient temperature,

I_{RMS}: RMS value of the current flowing through a single device,

R_{DSon}: ON resistance of each eFuse,

$R_{\theta JA}$: Junction-to-ambient thermal resistance of the eFuse.

Under the presence of transient load scenarios, the device junction temperature must be limited to the maximum recommended operating temperature of 125°C at the elevated system ambient temperature. To make sure of this, either the value of $R_{\theta JA}$ must be lowered by improving the thermal management and PCB layout or the number of devices in parallel must be increased to the next integer. To avoid the effect of electromigration over the lifetime of the device to maintain long-term reliability, the transient peak current flowing through each device needs to be close to the peak current rating (for example, TPS25985 is for 60A RMS current and 80A peak current). The thermal performance of TPS25985 eFuse with the transient load of 50A for (100-X) ms and 80A for X ms is shown in Figure 5-1, where X is the PEAK Current Applied Duration in ms.

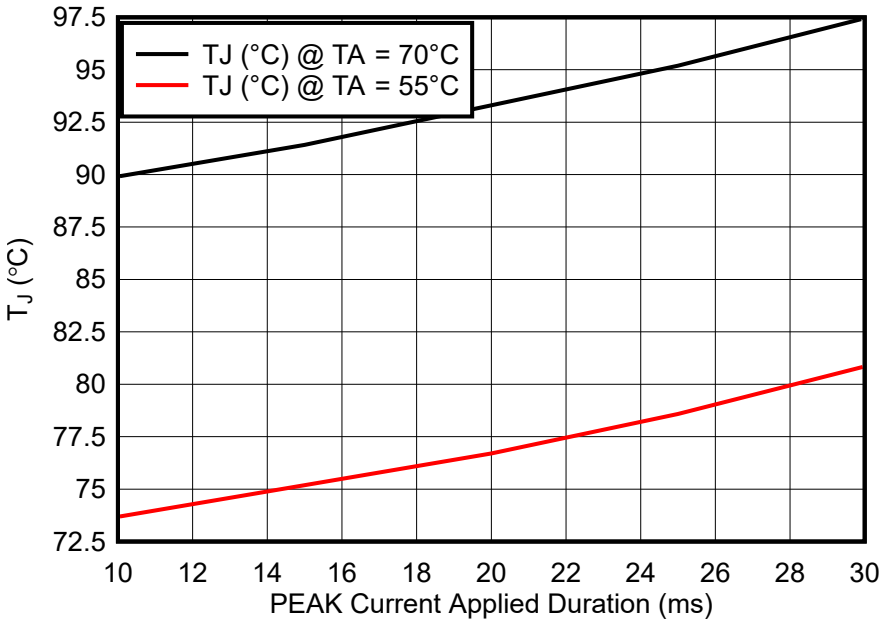

Figure 5-1. Thermal Performance of TPS25985 eFuse under Transient Load

6 System Level Advantages with TI's eFuse Design

6.1 Lower Number of eFuses to be Connected in Parallel

Customer Use Case:

- VIN = 12V,
- TDC = 220A, and
- IMAX = 370A for 12ms (max).

Using conventional eFuses, the minimum over-current protection set point needs to be around 400A, considering a 10% margin on top of the IMAX. To support this requirement, eight (8) conventional eFuses with a continuous output current rating of 50A (without air flow) are required to be in parallel, as there is no over-current protection until the system current reaches 400A.

Using TI's eFuse design, the I_{OCP} threshold is set at 1.1 times TDC, which becomes approximately 240A (220A x 1.1). Considering k as 0.5, I_{SFT} is at approximately 480A. One (1) TPS25990 (with a continuous RMS current rating of 50A) and a maximum of three (3) TPS25985 (with a continuous RMS current rating of 60A) eFuses need to be in parallel to support this customer use case.

The number required eFuses becomes half while using TI eFuse. This reduces the bill-of-material (BOM) cost of the system and improves the power density to a great extent.

6.2 Reduced PSU Size

In the customer use case mentioned in Section 6.1, the input PSU's minimum steady-state current rating needs to be around 240A using TI's eFuse design. A 3.2kW M-CRPS is selected. Dimensions of this PSU are 185mm (L) x 73.5mm (W) x 39mm (H).

The input PSU's minimum steady-state current rating needs to be around 440A using conventional eFuses. A 3.2kW M-CRPS is not enough to support this current. Another 2.2kW CRPS (DPS-2200AB-2) needs to be in parallel with a 3.2kW M-CRPS. Dimensions of the DPS-2200AB-2 PSU are 265mm (L) x 73.5mm (W) x 40mm (H). The total PSU size can be 265mm (L) x 147mm (73.5 x 2) (W) x 40mm (H) using the conventional eFuse design, **which is approximately 2.9 times larger than the design using TI's eFuse devices**.

7 Summary

This application note discusses the system-level benefits of using TI's high current eFuses over the other existing eFuses or hot-swap controller designs in the context of over-current protection and transient overload conditions for an enterprise server motherboard. The circuit breaker mechanism and a programmable over-current blanking timer feature greatly reduce the total system cost. It improves the power density by reducing the number of high-current-carrying power components in parallel or their size and the PCB copper trace thickness. This is because of the reduction of the overall RMS current rating of the system. Using TI's high-current eFuse designs, the input PSU rating is optimized to the TDC rating of the system, instead of making it rated for the peak pulse current rating of the system. Therefore, the system power utilization is greatly enhanced.

8 References

- Texas Instruments, *TPS25984: 4.5-V to 16-V, 0.8-mΩ, 70-A stackable eFuse with accurate and fast current monitor* data sheet.
- Texas Instruments, *TPS25985: 4.5-V to 16-V, 0.59-mΩ, 80-A Stackable Compact eFuse with Accurate and Fast Current Monitor* data sheet.
- Texas Instruments, *TPS25984Bx: 4.5V–16V, 0.8mΩ, 70A Stackable Integrated Hotswap (eFuse) With Accurate and Fast Current Monitor* data sheet.
- Texas Instruments, *TPS25990: 2.9-V to 16-V, 0.79-mΩ, 60-A eFuse With Digital Telemetry Controller* data sheet.
- Texas Instruments, *TPS1685x 9V–80V, 3.65mΩ, 20A Stackable Integrated Hotswap (eFuse) With Accurate and Fast Current Monitor* data sheet.

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