Application Note

TPS257xx-Q1 Pass Compliance and QuadraMAX Best Practice

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ABSTRACT

Passing USB Power Delivery Compliance Test Specification (CTS) issued by USB-IF is required for all USB Power Delivery (PD) end-products. Programmable Power Supply (PPS) function can be validated based on Power Delivery Source Power Requirements Test document if required by customer. This application note shows some compliance test cases and QuandraMAX test practice based on TPS257xx-Q1 products. VIF configurations are also introduced.

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Trademarks

1 Introduction

The TPS257xx-Q1 is a highly integrated USB TypeC® Power Delivery controller for use in single and dual USB port applications including: charging only; charging with USB 2.0 or USB3.0 data; and charging with USB data and DisplayPort™ alternate mode. The power communication talking message is transferring on CC line referring to USB-PD protocol. As USB-PD negotiation completed, appropriate power path enabled and corresponding power mode set.

2 Vendor Information File (VIF) Setting

To expedite the compliance testing process for qualifying products that support USB, product vendors are required to provide one or more Vendor Info Files (VIF's) that describe, in detail, the product to be tested. Tool is shared by USB-IF for VIF generation.

VIF defines the capabilities of the Device Under Test (DUT). The compliance testers uses this information to devise some tests or results. But there are many parameters to be entered manually. Mismatches between VIF and Configuration settings are common compliance failures. There are two methods to generate VIF.

2.1 Automatic VIF Generation

The first method is to generate VIF automatically by using customized GUI tool for TPS257xx-Q1.

The tool can generate .XML format VIF file based on current project settings. Fill in all the configurations and click save vendor information file. Opening the generated VIF file by USB vendor generation tool to double check the configuration correctness is a good practice.

2.2 Generate VIF Manually

Below is the general view of VIF editor shared by USB-IF. Customers or engineers can download the tool on USB-IF official website. The tool allows engineers to configure needed parameters matching with product waiting for test. The editor generates .xml VIF for Type-C compliance, PD compliance, USB3.2 compliance and USB4 compliance. The following sections depict these fields and features briefly based on products TPS2772-Q1. Single port PD devices have a similar principle. Open VifEditor which can be downloaded from USBIF official website. Firstly, choose Port Product and then create new VIF. Below tab emerges.

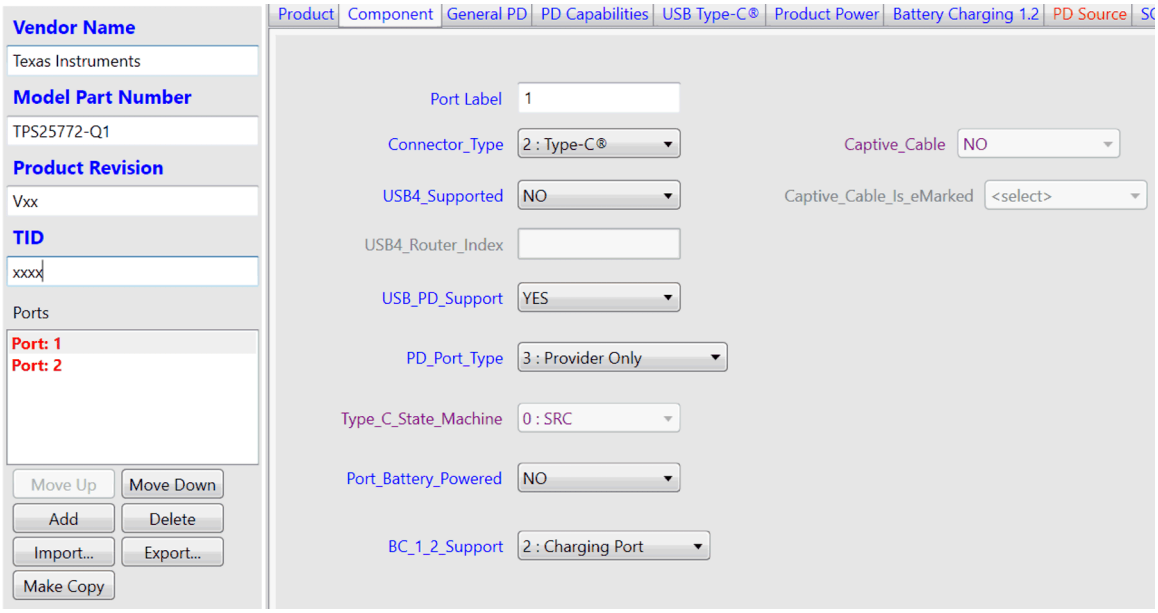

Figure 2-1. Generate VIF Manually

Captive_Cable:

Indicates whether this Component has a captive cable. Any Component that presents a Type-A or USB Type-C plug is considered to have a captive cable, even if there is nothing visible that looks like a cable (for example, a USB thumb-drive).

PD_Port_Type:

3 - Provider Only (asserts Rp)

TPS257xx-Q1 only serves as a power source. So item 3 'Provider Only' must be chosen.

As the above information is filled in, other tabs pop up.

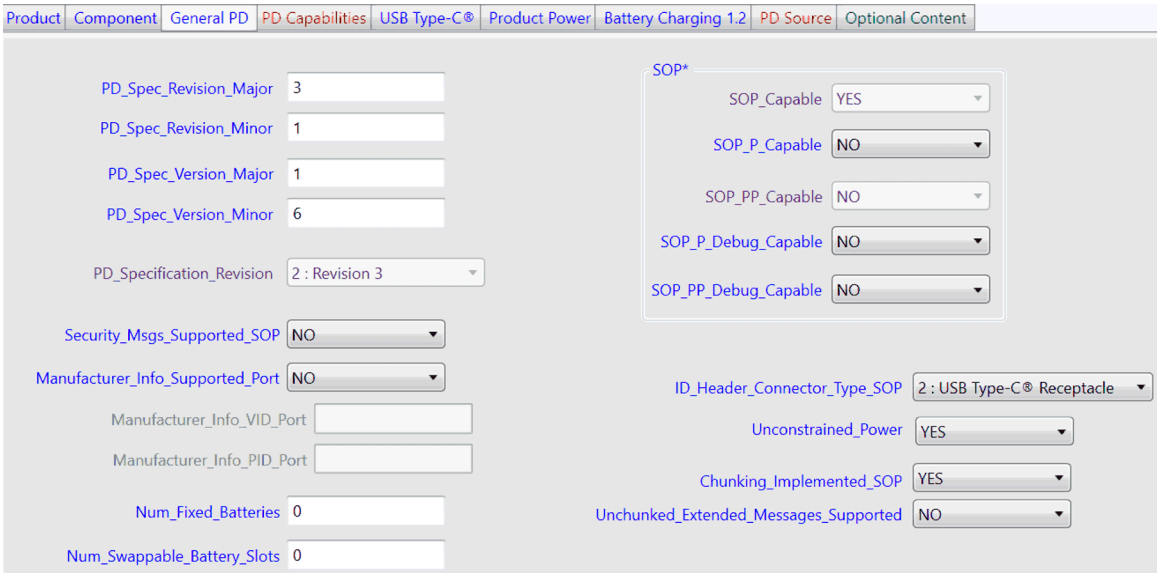

Figure 2-2. General PD Configuration

For PD_Spec_Version_Minor, please check USBIF official website for the latest version number.

Note that PD CTS revision 1.2 is the initial merged specification. This document specifies USB-IF compliance tests for a USB PD3.1 device. This document includes both PD2.0 and PD3.0 test items into one specification. Products must pass both PD2.0 and PD3.0 items test. Customers need to pay attention to the latest specification versions no matter for PD CTS or PD specification. USBIf can modify, add, remove, relax or strict some items. The updates matters a lot of the test results. Please check USB IF official website timely for the latest specifications.

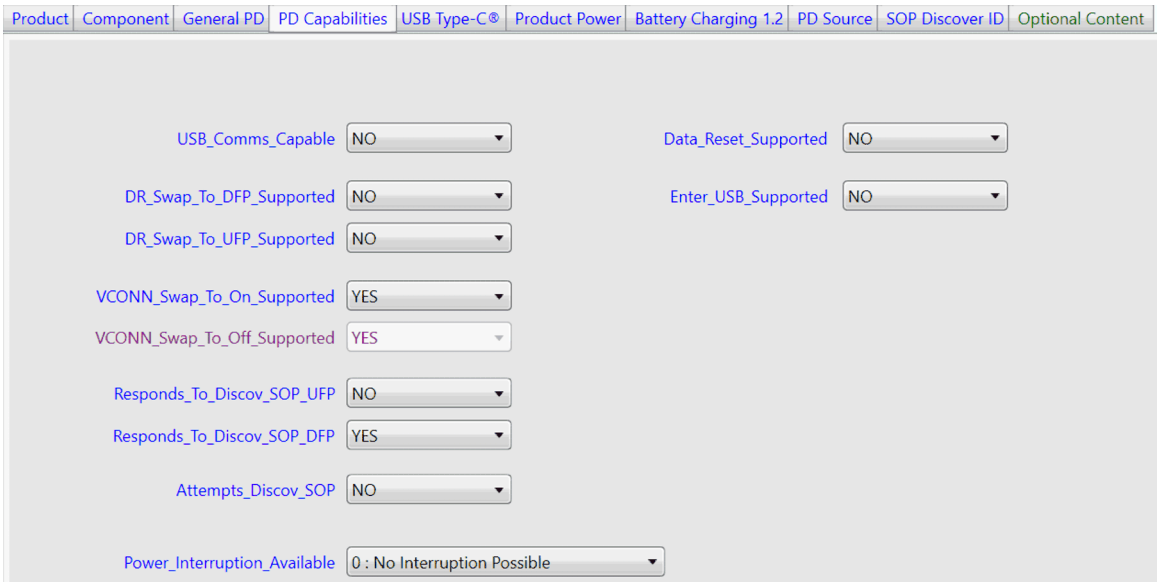

Figure 2-3. PD Capabilities

USB_Comms_Capable:

This item signifies whether Qualifying Product is capable of enumerating as a USB host or device?

Generally, this is no meaning the product does not support data communication and only acts as power source. But some customers, can bypass IC data line and connect USB2.0 or USB3.2 signals directly to HUB or SOC to support data communication. For this scenario, check Yes for this item. The reason is that tester checks data line signals to confirm whether any signal passes or not.

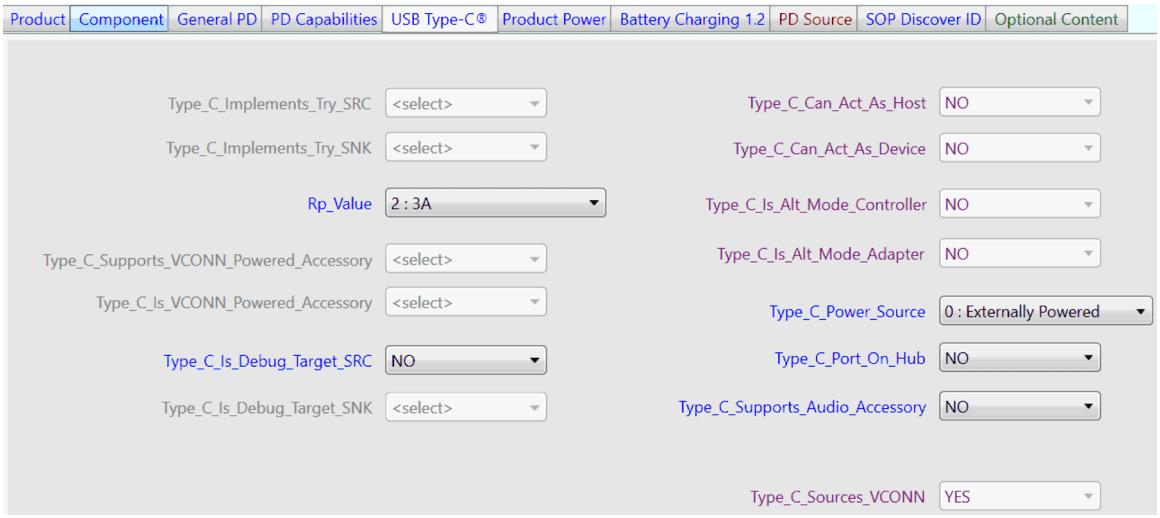

Figure 2-4. USB Type-C Configuration

Additionally, based on Vendor Info File Definition, if USB_Comms_Capable is No, then Type_C_Can_Act_As_Host and Type_C_Can_Act_As_Device is No. If USB_Comms_Capable is set to YES and Type_C_Can_Act_As_Device is set to NO, then Type_C_Can_Act_As_Host field shall be set to YES.

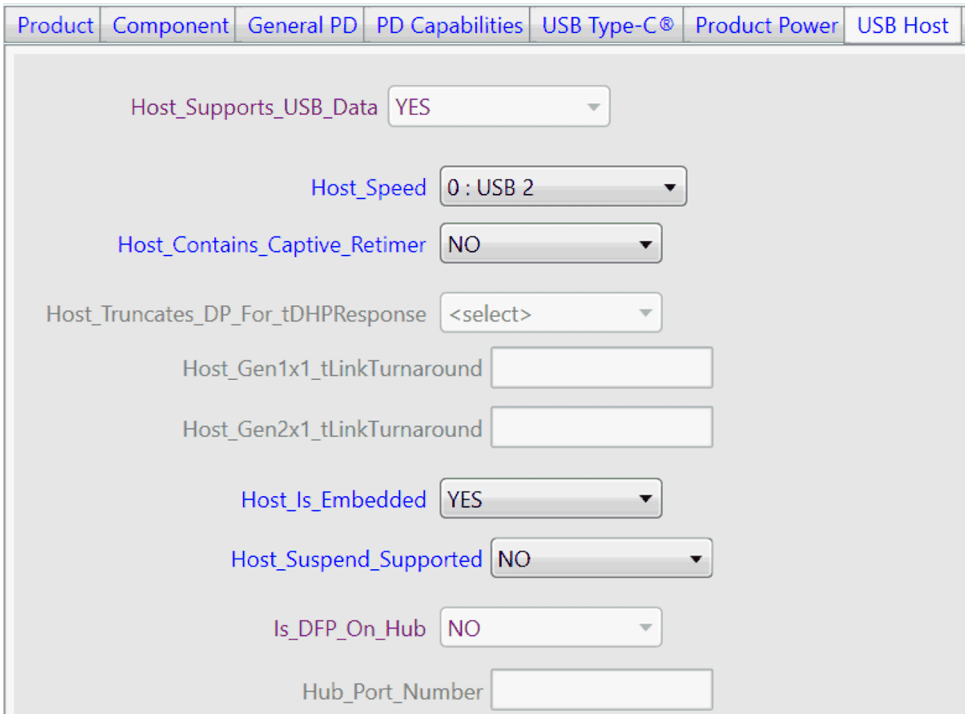

Figure 2-5. USB Host Configuration

If USB_Comms_Capable is set YES, then another panel USB HOST pops up. Please configure the page according to Figure 2-5.

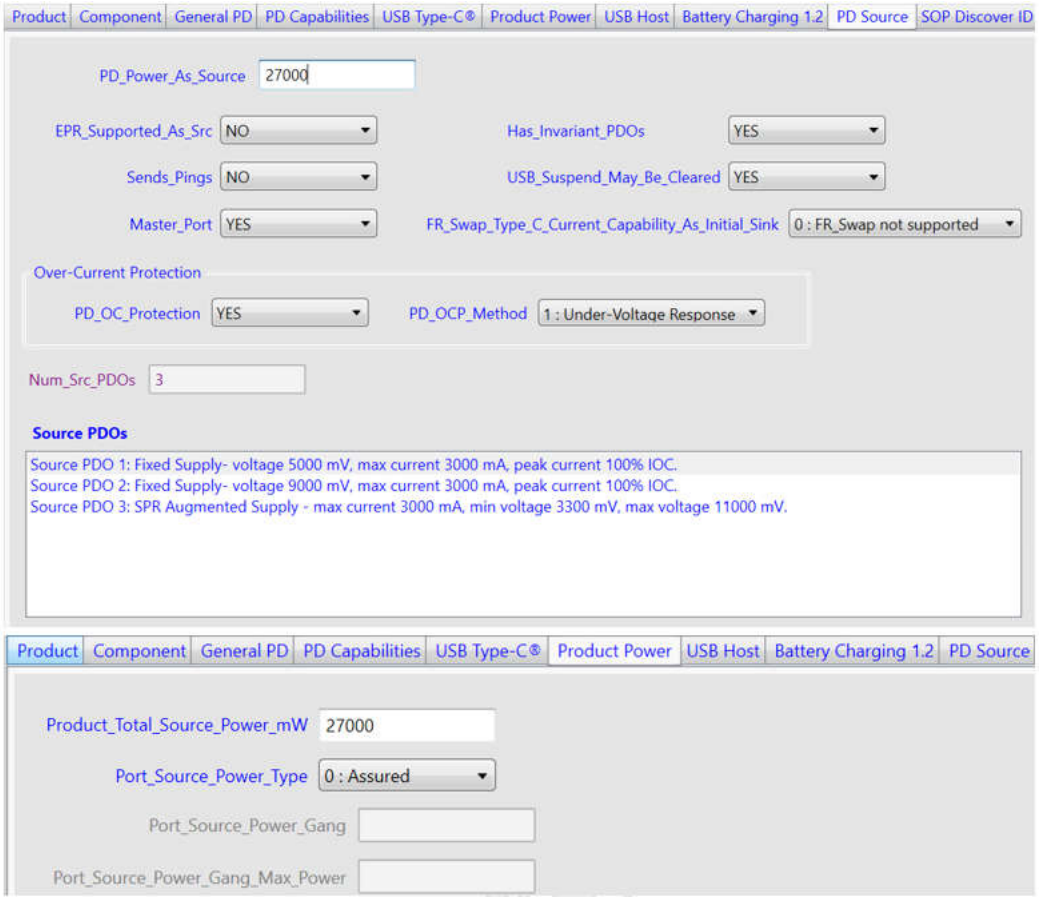

Figure 2-6. PD Source Configuration

Figure 2-6 sets parameters of PD source. Note that PD_Power_As_Source is fixed Power Delivery Objects (PDO) maximum power instead of Augmented Power Delivery Objects (APDO). Otherwise, some failures can occur as doing PD compliance test. So for above case, fill in 27W source power other than 33W. Also Product_Total_Source_Power_mW also corresponds to 27W. Port_Source_Power_Type is determined by customer's specific requirements.

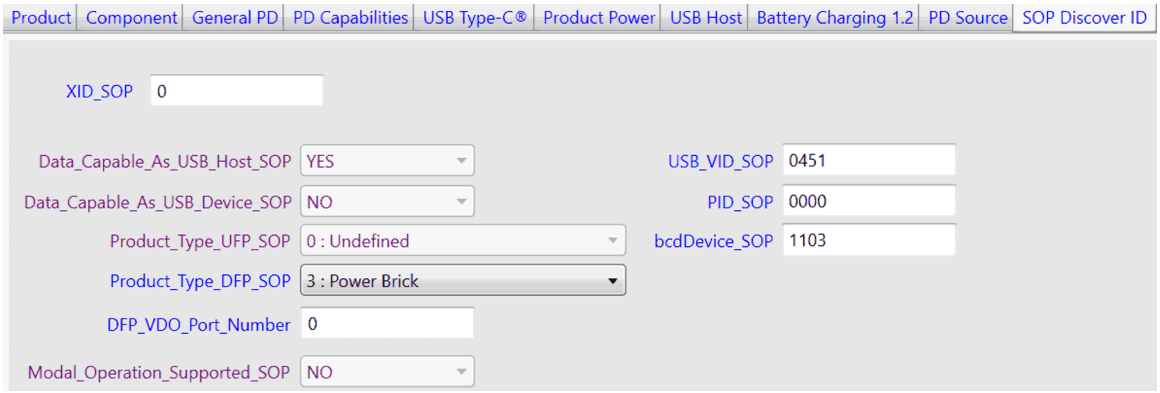

Figure 2-7. BC1.2 Protocol and SOP Discover ID

For XID_SOP, A decimal number assigned by USB-IF prior to certification. For USB_VID_SOP, this field is a 4-digit hexadecimal number, with valid values in the range of 0h - FFFFh (0 - 65535). This field is assigned to the Vendor by USB-IF. The vendor must ask USBIF and apply for both XID and VID before informal compliance certification or test.

For BC_1_2_Charging_Port_Type, the application generally is charge only. Item 0, DCP mode can be chosen. Some customers can require to support data communication. So for BC1.2 charging protocol, item 1, CDP mode is the choice.

Above is the general configuration of VIF parameters. Some parameters or panels can change in future based on specification revision updates or modification by USB IF. Please check and download the latest spec or configuration tools on USB IF official website.

3 Power Delivery Compliance Test

The Universal Serial Bus (USB) specification defines the product design targets at the level of interfaces and mechanisms. Compliance program is to complement the specifications and enable measurement of compliance in real products. Compliance Program provides reasonable measures of acceptability. The Compliance Program uses multiple test specifications along with a Test ID (TID) to track and define the test criteria used to evaluate a product. Products that pass this level of acceptability are considered USB-IF certified and are added to the Integrator's List and have the right to license the USB-IF Logos. USB-IF WG defines and updates the Base Spec, Tests Spec, conduct compliance workshops or conference etc. Currently USBC/PD End Product Certification requires a complete Pass from below Tests :

- Type-C Functional Tests
- USB PD Compliance – PD Merged CTS Rev 1.4
- Source Power Tests (Quadramax Tests)
- Inter-Operability tests with known good devices.

This section specifies USB-IF compliance tests for USB PD3.1 device. The section includes both PD2.0 and PD3.0 test items into one specification, namely merged specification. Products must pass both PD2.0 and PD3.0 items test. Currently the USB Power Delivery Specification is revision 3.1 version 1.8. All USB PD products can be tested by one approved design listed below. The pre-condition is to scan through all test items (physical, protocol and power) by one institution. If not, all USB PD products must be tested against 2 of the 4 approved designs listed below. There is a grace period of all new tests on CTS. For silicon the period is 1 Year and for end product the period is 1.5 Years from Introduction data.

- Granite River Labs- USB Power Delivery and USB Type-C Tester and Analyzer (GRL-USB-PD-C2)
- MQP PDT
- Teledyne LeCroy - Voyager M310e/M310p Protocol Analyzer / Exerciser / Compliance Test Platform
- Ellisys USB Explorer® 350 Protocol Analyzer, Generator, and Compliance Test System

Deterministic and communication engine are integrated and include Common Bring-Up procedures, Common Procedures and Common Checks.

- There are up to 13 Common checks. These checks are performed throughout all the tests. The correctness of basic rules of physical and protocol layers are checked. Common check failures are treated as Common check failure, not test failure. But there is not any common check failure for certification. Please refer to section 3.1 of PD spec for more information.
- Common bring-up procedures are used to bring up the Device Under Test (DUT) in specific way for the tests. There are up to 12 Bring up procedures. Each test uses one or more bring-ups for a test execution. Please refer to section 3.2 of PD spec for more information.
- Common Procedures determine how the testers responds to the messages from the DUT. Unless otherwise specified on specific test, the tester runs this procedure. Please refer to section 3.3 of PD spec for more information.

3.1 Basic Software for Compliance Test and Results Analysis

Figure 3-1. GRL C2 PD Compliance Test Tool

GRL-USB-PD-C2-EPR (C2-EPR) provides and automates USB Power Delivery compliance testing at up to 240W at the push of a button. A comprehensive API portfolio enables users to run sample scripts, or program

them in C# and Python. And the Power Suite Pro Application takes users beyond traditional compliance. For PD3.1, the basic test items include Physical layer, Protocol layer and Power Supply tests.

Please download GRL-C2 USB Power Delivery and USB Type-C Test software on GRL official website. One basic function of this software is used for PD compliance test results analysis.

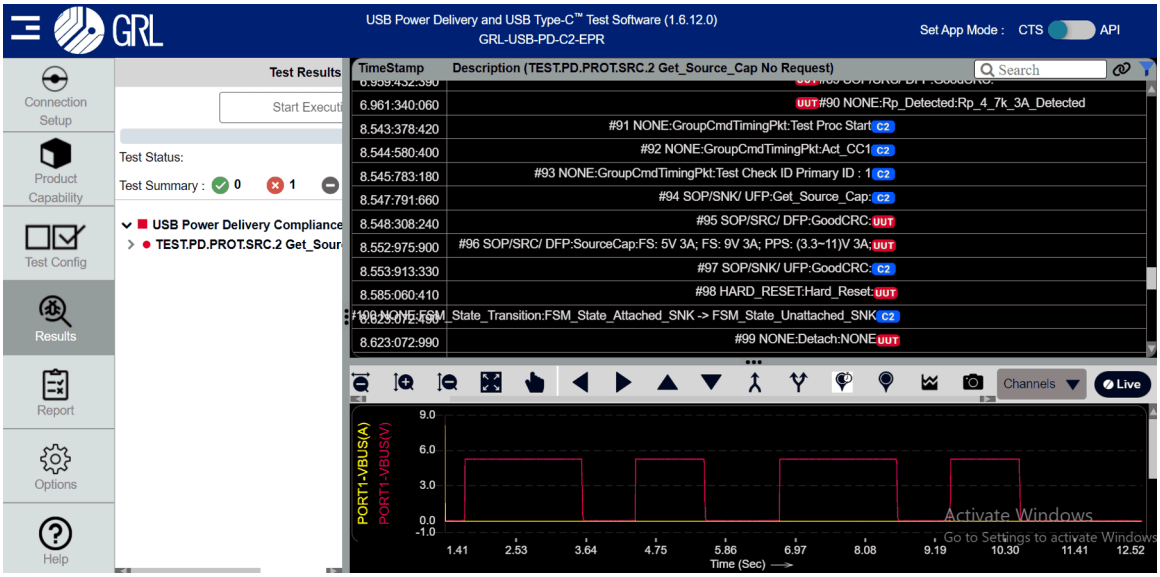

Figure 3-2. GRL-C2 Results Analyzer

Click Results panel and choose .grltrace file that you want to check or failure analysis. The file includes PD message data communication log and areas for waveforms display which is very convenient for results check. It also imbeds toolbars useful to view results. Please find help files for more details.

Figure 3-3. LeCroy: M310

The Voyager M310e is used for validating USB designs with the USB-IF compliance test specifications. the Voyager M310e fully supports USB PD 3.1 functionality. The exerciser port of the Voyager M310e is also enhanced to capture side band use (SBU) and auxiliary (AUX) messages for USB Type-C devices that support USB4 or DisplayPort Alternate modes. The instrument can fully validate PD3.1 compliance spec includes Physical layer, Protocol layer and Power Supply and so on.

Please download Teledyne LeCroy USB Protocol Suite on LeCroy official website. The suite is able to analyze USB4, USB3.2, USB2.0 and PD results. Open data log file with the extension of .usb. Similar with GRL-C2, the log also mainly includes two sections. Data log trace view is for protocol data analysis. Power tracker section consists of VBUS power tracker, CC power tracker and VCONN power tracker. waveform details are shown as below.

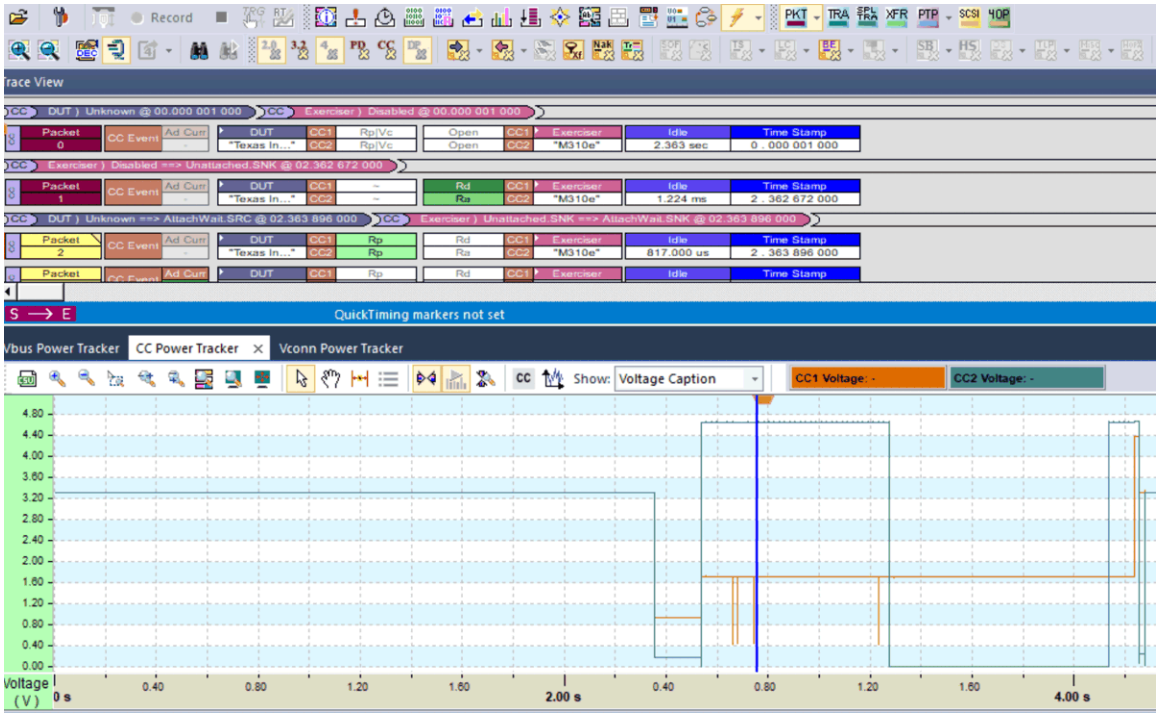

Figure 3-4. M310 Data Log Analyzer

Also there are other two solutions for PD compliance test, MQP and Ellisys. Please search their official website for more information.

4 Power Delivery Source Power Requirements Test

Universal Serial Bus Type-C and Power Delivery Source Power Requirements Test Specification (SPT) applies to Vbus source-capable USB Type-C connector ports. The test definitions cover droop/drop, connect, disconnect, and USB PD voltage transitions, current transitions and over current protection. Compliance criteria are provided as a list of assertions that describe specific characteristics or behaviors that must be met. Each assertion provides a reference to the USB Power Delivery specification or other documents from which the assertion was derived. In addition, each assertion provides a reference to the specific test descriptions where the assertion is tested.

For single port PD products, SPT1, SPT3, SPT5, SPT6 and SPT7 are required to be tested. For multi-ports PD products, SPT1, SPT2, SPT5, SPT6 and SPT7 are necessary test items. Noted that SPT6 and SPT7 shall be tested only for products with PPS function supported. If customers don't require PPS function, only SPT1, SPT3, SPT5 shall be tested for single port production and SPT1, SPT2, SPT3, SPT5 shall be tested for dual ports.

4.1 SPT.1 Load Test and SPT.2 Capabilities Test

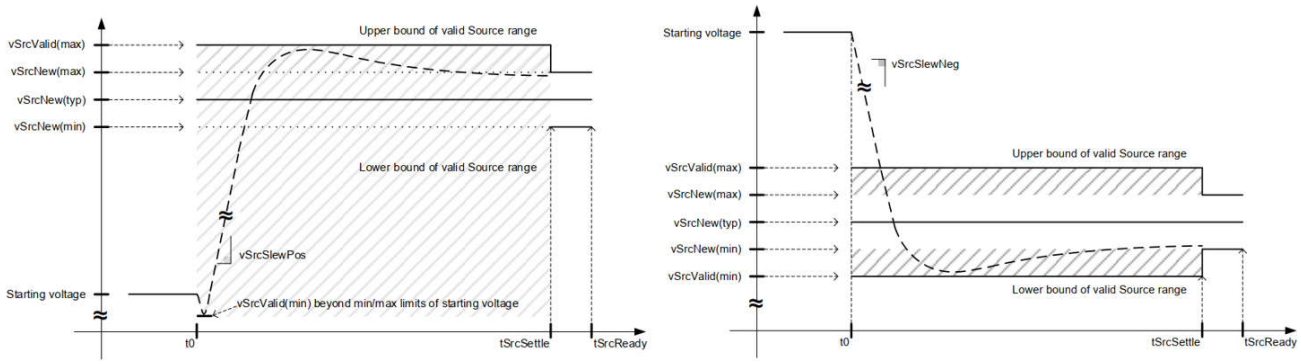

Figure 4-1. Fixed Supply Voltage Transition

Figure 4-1 shows fixed supply voltage transition tests which asserts in PD CTS Power Supply section 7.1.4.1. The Source Shall transition VBUS from the starting Voltage to the higher new Voltage in a controlled manner. The negotiated new Voltage (For example, 5V, 9V, 15V…) defines the nominal value for vSrcNew. During the transitions, voltage thresholds and time specs shall be in demanded range.

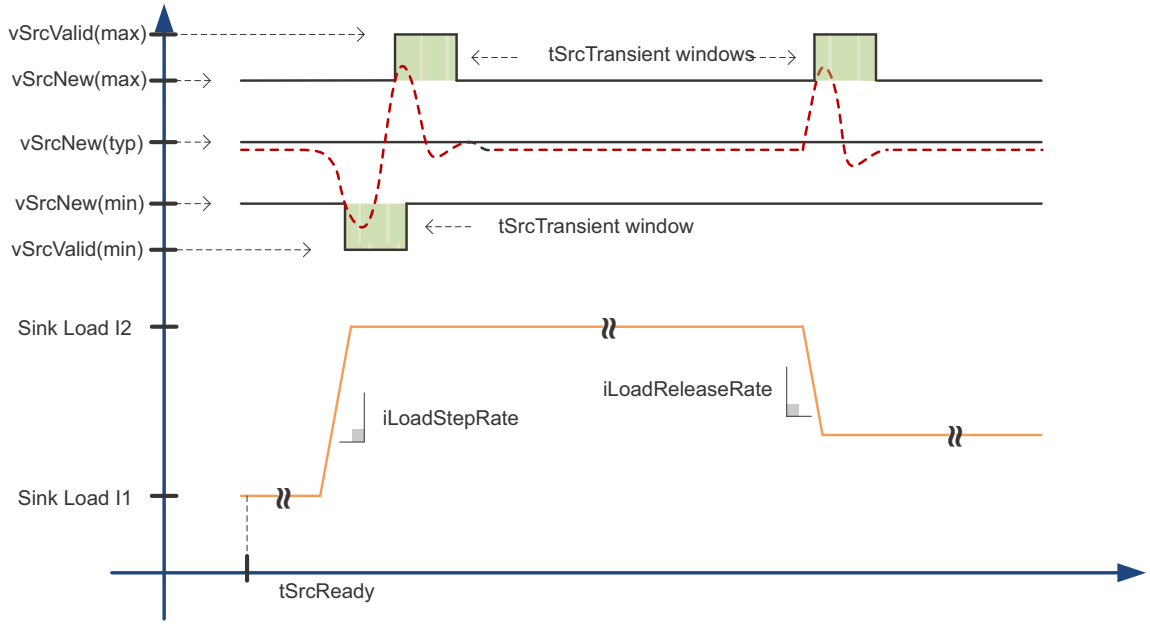

Figure 4-2. Application of vSrcNew and vSrcValid Limits After tSrcReady

Figure 4-2 illustrates PD CTS Power Supply section 7.1.8. This test item defines output voltage tolerance and range after voltage transition is complete and during static load conditions or transient load conditions. Please refer to PD spec for more information.

SPT.2 Capabilities Test verifies that each port can simultaneously provide a different advertised voltage. This test is required for Multi-Port products with at least one PD port that supports more than one Source Capability. The test also asserts PD3.0 7.1.4.1 and 7.1.8.

4.2 SPT.3 Hard Reset Test

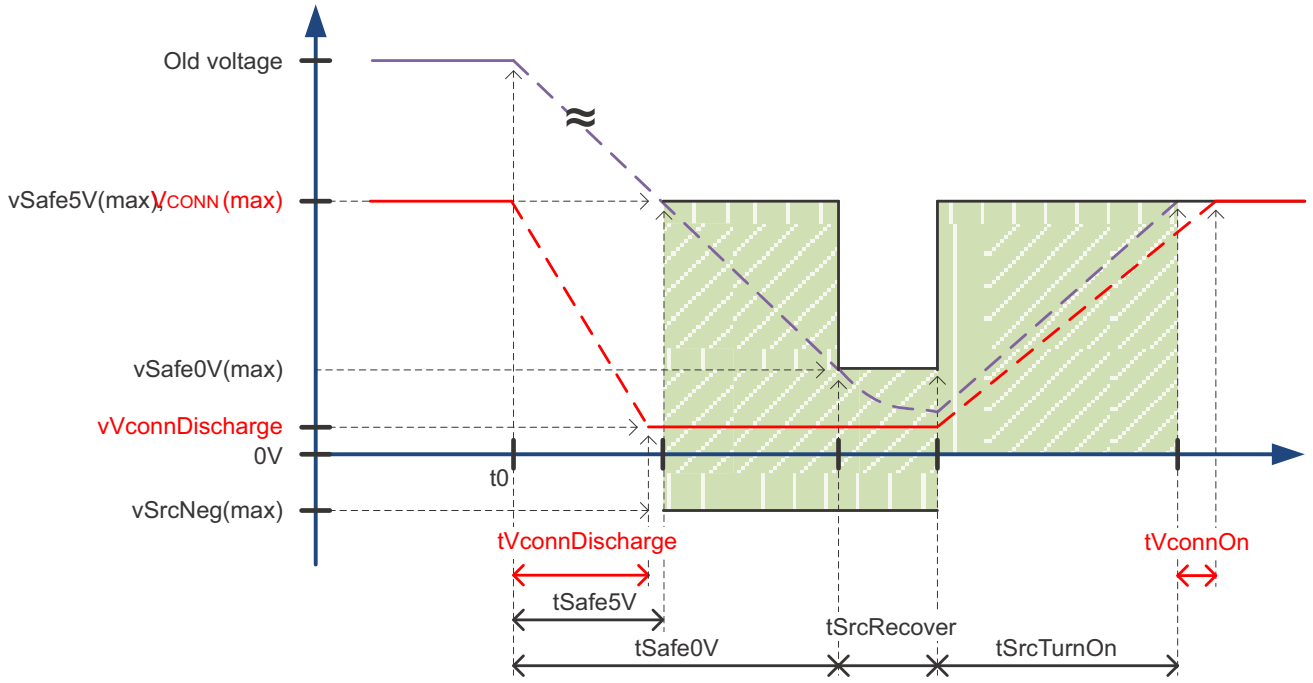

Figure 4-3. Source VBUS and VCONN Response to Hard Reset

Hard reset signaling indicates a communication failure has occurred and the source stops driving VCONN, removes Rp from the VCONN pin and drives VBUS to vSafe0V. The USB connection resets during a hard reset since the VBUS voltage is less than vSafe5V for an extended period of time. After establishing the vSafe0V voltage condition on VBUS, the source shall wait tSrcRecover before re-applying VCONN and restoring VBUS to vSafe5V. The test also belongs to Power Supply section covering PD CTS 7.1.5.

4.3 SPT.5 Over Current Test

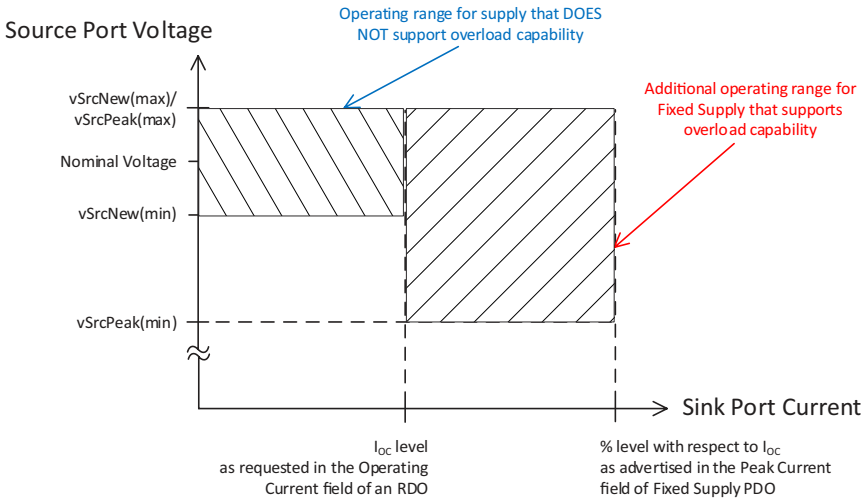

Figure 4-4. Source Peak Current Overload

This test item covers PD3.0 CTS 7.1.7.1 and CTS 7.1.11. Sources operating in SPR mode Shall implement over current protection to prevent damage from output current that exceeds the current handling capability of the Source. Sources attempt to send a Hard Reset message when over current protection engages followed by an Alert Message indicating an OCP event once an Explicit Contract has been established.

A Source that has the Fixed Supply PDO or EPR AVS APDO Peak Current bits set to 01b, 10b and 11b Shall be designed to support one of the overload capabilities. Sources are not required to support continuous overload operation. When overload conditions occur, the Source is allowed the range of vSrcPeak (instead of vSrcNew) relative to the nominal value. When the overload capability is exceeded, the Source is expected take whatever action is necessary to prevent electrical or thermal damage to the Source.

4.4 SPT.6 PPS Voltage Step Test

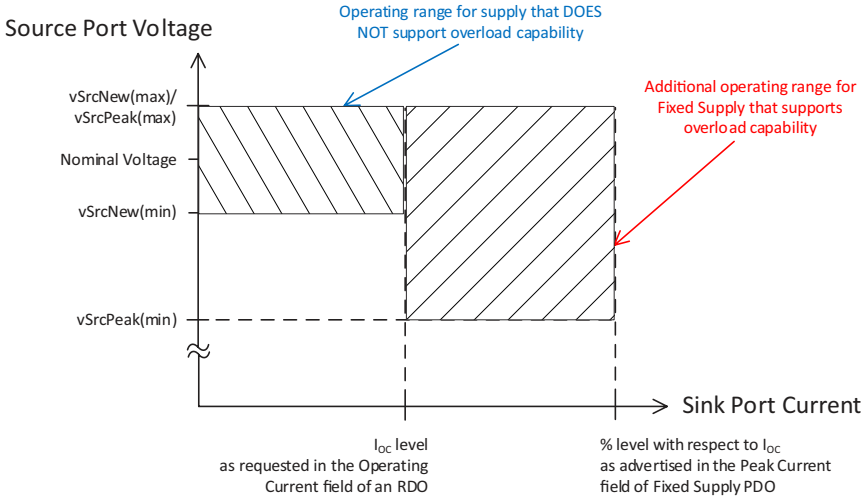

Figure 4-5. PPS Positive Voltage Transitions

For PD products supporting PPS function or advertising APDO capabilities, SPT.6 shall be tested. The PPS Step Test verifies that when a source port makes a contract using an APDO, the output follows the monotonicity and tolerance requirements from USB PD spec section 7.1.4.3. The test is required to pass no matter for single port or multi-ports and is verified by Quadramax instrument. For multi-ports tests, two or more Quadramax instruments are needed. For bench set-up details, please refer to ‘QuadraMAX PPS Test Guide.

During tests, SPT verifies several tolerance requirements based on PD spec. In practice, error 'The source voltage remains within vPpsValid for the duration of the transition' usually occurs. Just open the log folder and search 'testLog.csv' file. The file logs all test data information of each step. Step 2.k.1.b.ii shows failure. Check 'Universal Serial Bus Type-C and Power Delivery Source Power Requirements Test Specification' and the spec also describes the failure step details.

To show the log more intuitively, checking both total-phase data log and QuadView data log is a good practice. Download both tools from total-phase official website and USBIF official website individually. Both methods depict logs by waveforms. Acquiring total-phase data log is strongly recommended. Customers can require test institutions to extract data by total-phase tools. The data log is beneficial for data analysis further. Institutions opt to not use these tools.

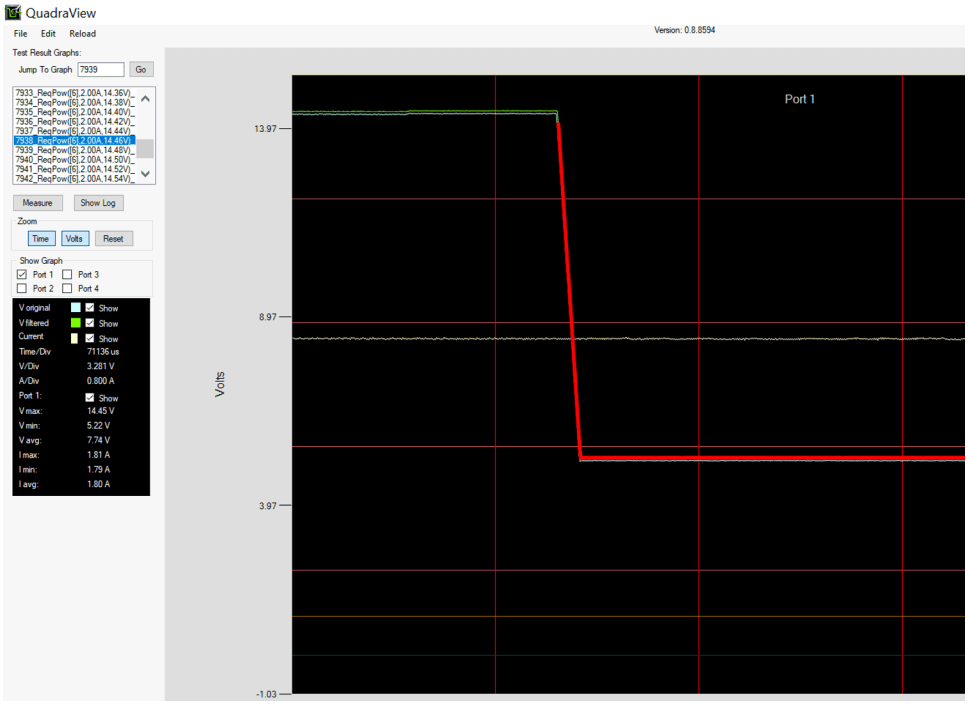

Figure 4-6. QuadView Data Log Check

Check picture #7939 by QuadView, red line indicates the error. The data log shows as voltage increases from 14.46V to 14.48V by 20mV step, VBUS voltage drops to 5V.

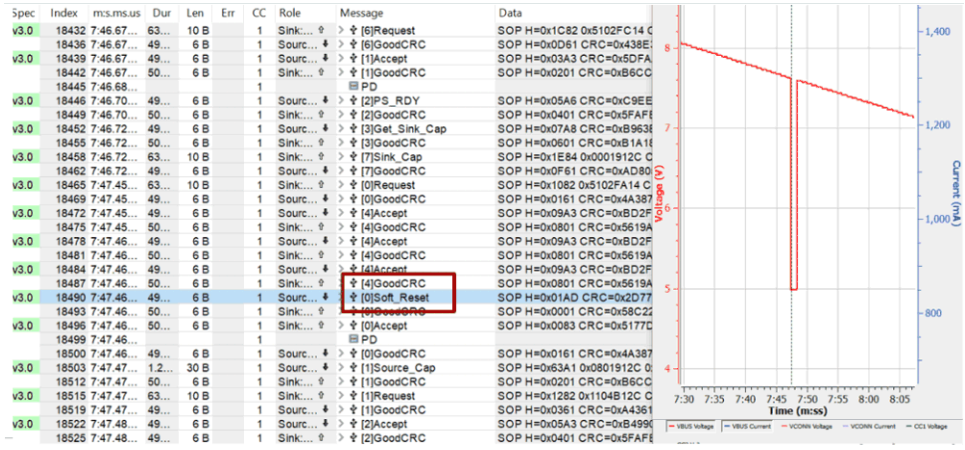

Figure 4-7. Total-Phase Data Log Check

To spot the root cause further, check total-phase data log. The log shows Soft_Reset occurs. By comparison test in lab, the error is introduced by tester issue. Update latest tester software version, issue solved.

4.5 SPT.7 PPS Current Limit Test

The PPS Current Foldback Test verifies that when a source port makes a contract using an APDO and current reaches Operating Current level, the output follows the tolerance requirements from USB PD spec 7.1.4.2. Please timely check latest PD spec and PD CTS upon USBIF official website. USBIF updates specs occasionally which are crucial for certification test reference. USBIF relaxes the current limit test range recently. The key parameters is iPpsCLNew (-150mA, 150mA) and slew rate of current step (iPpsCLLoadReleaseRate, iPpsCLLoadStepRate). In practice, output capacitors influence heavily on this test item. TI suggests customer to strictly follow capacitance values IC provider rules. The test procedures refer to 'Universal Serial Bus Type-C and Power Delivery Source Power Requirements Test Specification'. Look up the test manual, Total-phase data log and QuadView data log as debug failures.

Figure 4-8 is SPT.7 test log extracted by total-phase analyzer. The tester runs 3 APDOs, 3.3V~11V, 3.3V~16V, 3.3V~21V. Customer's requirements determine how many APDOs need to be tested. Test procedures C, D, E rules RDO currents, voltages and steps resolution to test.

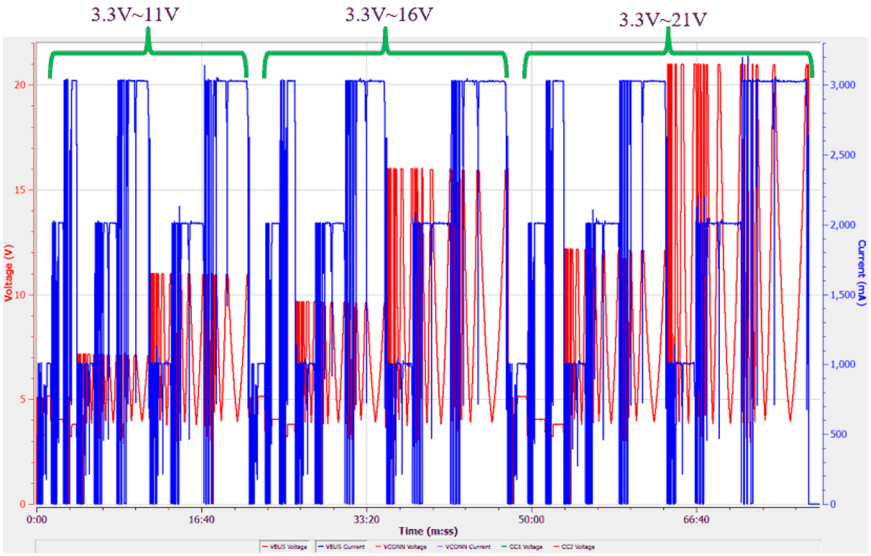

Figure 4-8. SPT.7 Total-Phase Analyzer Data Log

6.b.6.b	23:19.2	1	1294	Current exceeded iPpsCLTransient.
6.b.6.b	23:19.2	1	1294	Current did not settle to iPpsCLNew within tPpsCLSettle.
	23:20.0			Result Graph # 1295:
6.b.6.b	23:20.0	1	1295	Current exceeded iPpsCLTransient.
6.b.6.b	23:20.0	1	1295	Current did not settle to iPpsCLNew within tPpsCLSettle.
6.b.6.e	23:20.0	1	1295	Average Current has decreased in CL Mode when resistance has decreased.
	23:28.1			Result Graph # 1303:

Figure 4-9. SPT.7 Failure Data Log

Based on .cvs log, search image #1294 by QuadView shown in Figure 4-10 and clearly displays oscillation as increase current by 500mA step. Also check Total-phase data log depicted in Figure 4-11 for more information. Similar oscillation occurs. But the protocol negotiation is normal. So try to figure out some methods to stabilize current, such as increasing capacitance around BUS pin, or check filtering circuit of current limit loop. For most current limit test, simply increase BUS capacitance being able to solve several failures.

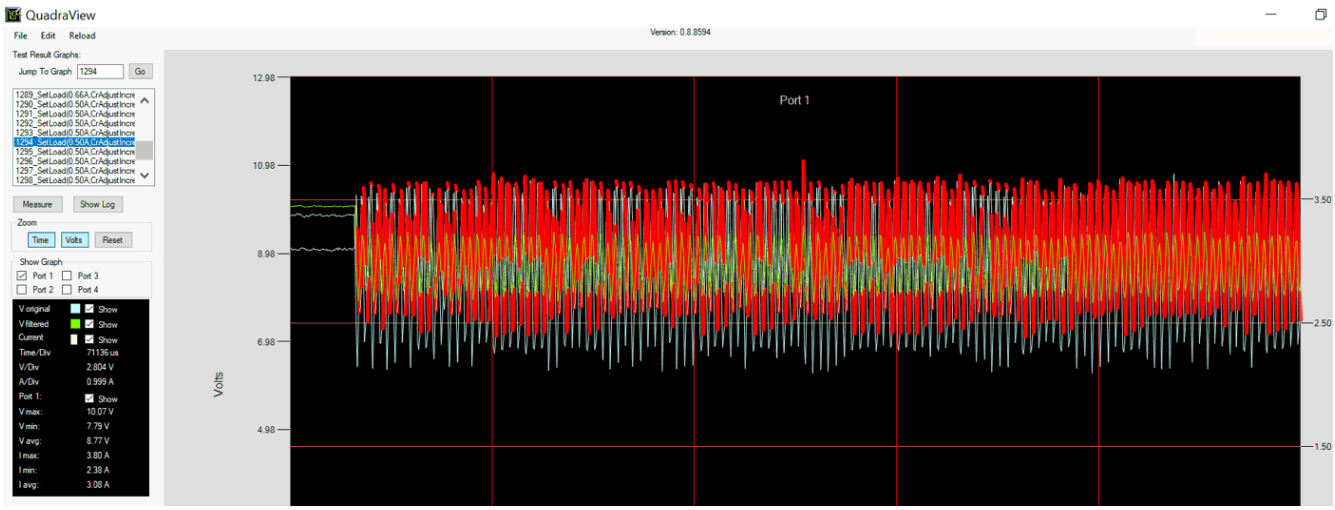

Figure 4-10. QuadView Data Log of SPT.7

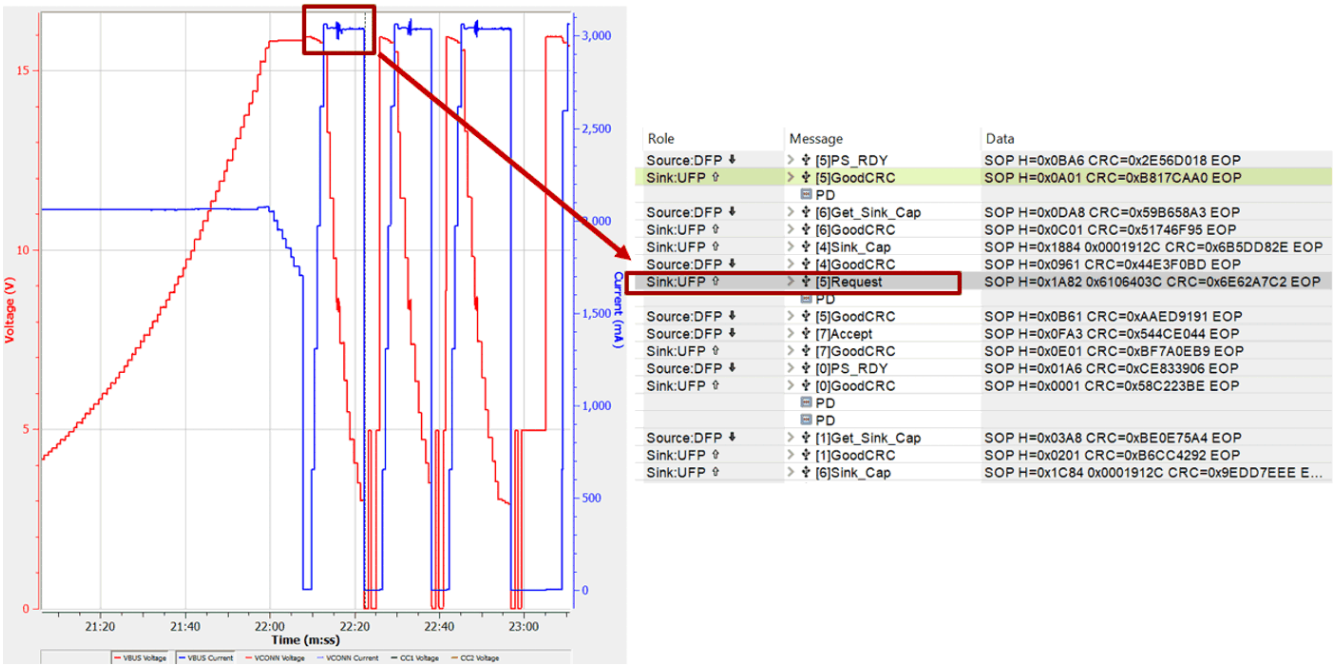

Figure 4-11. Total-Phase Data Log of SPT.7

5 Analysis of Some Failure Examples

Common check failure

Open .XML format log file and spot the failure item. The log shows Common.Check.PD.7#7 failure and occurs as testing TEST.PD.PS.SRC.1.

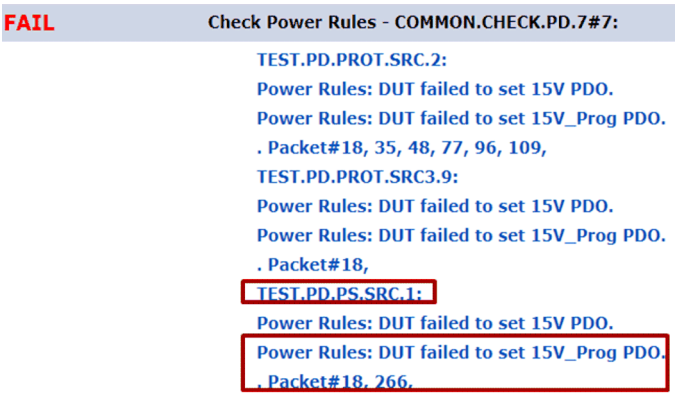

Figure 5-1. Common Check Data Log

Search CTS file and locate Common.Check.PD.7#7. 'The Tester compares all PDOs to VIF field PD_Power_as_Source and checks that they meet the requirements of the Power Rules.' The line indicates PDOs settings contradict with PD_Power_as_Source in VIF.

Open the failure .grltrace file and based on Figure 5-2, spot packet #18 in the data log. VIF settings contains 5V 3A, 9V 3A and (3.3V~11V) 3A. Also check field PD_Power_as_Source = 33W. The failure prompts DUT failed to set 15V_Prog PDO. So the failure is caused due to incorrect PD_Power_as_Source setting. Fill in 27W which is determined by Fixed PDO power instead of APO power. What's more, Product_Total_Source_Power is 27W as well.

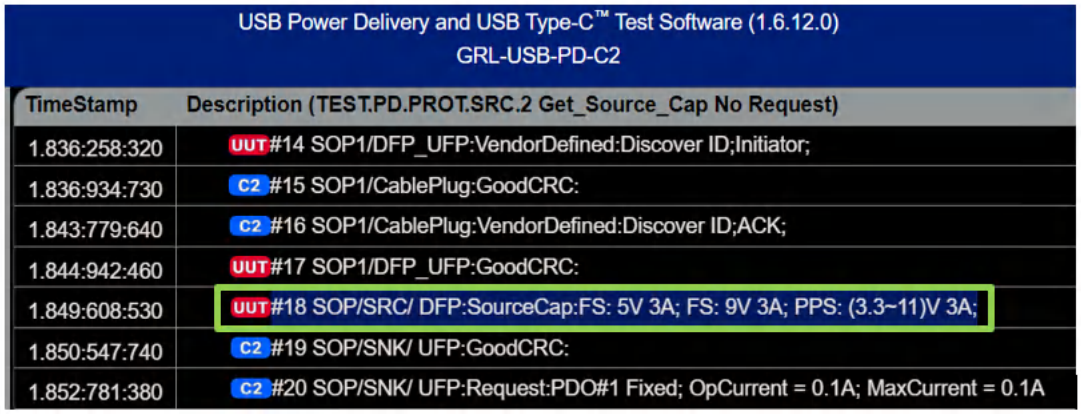

Figure 5-2. TEST.PD.PRO.SRC.2 Data Log by GRL-C2

TEST.PD.PROT.SRC.2#2 Get_Source_Cap No Request

Open .XML format log file and spot the failure item. The item belongs to protocol layer failure and occurs as testing DUT source capability.

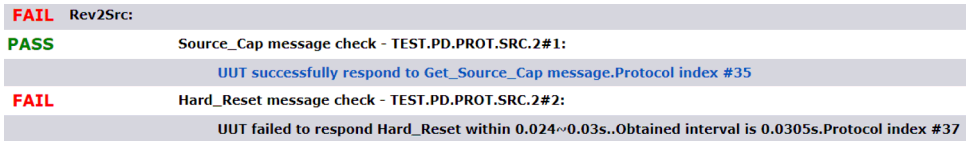

Figure 5-3. XML Data Log

Look up CTS file and search Get_Source_Cap No Request test item. The Tester sends a Get_Source_Cap Message to the UUT. After receiving a Source_Capabilities Message, the Tester intentionally does not send the Request Message to force a SenderResponse Timer timeout on the Source UUT. The Tester verifies correct implementation of this timer.

Open the failure item .grltrace or Lecroy .usb log file and find index 37 based on Figure 5-4. Before further analysis, get noted that the Code 'Rev3ChkdSrc' means that the Port is being tested for PD Revision 3, with the Tester set not to support Unchunked Extended Messages, and as a Source. 'Rev2Src' suggests the Port is being tested for PD Revision 2 and as a source. So both check PD2.0 specification and PD3.1 specification. Listed as below. The log shows very clear that PD3 mode passed but PD2 mode fail. Because it's a firmware failure, so ask firmware team for one new patch and solve this issue.

Figure 5-4. GRL-C2 data log of TEST.PD.PRO.SRC.2

TEST.PD.PS.SRC.1 Multiple Request Messages

Open .XML format log file and spot the failure item. The failure belongs to Power Source layer and occurs as testing DUT source capability.

The purpose of this test is to check whether DUT Source responds correctly to various Sink load Request Message. VBUS voltage shall be limited in provided range during Request transition. Open the failure log file .XML. The failure occurs as current increases from 2.25A to 3A. Measured VBUS voltage is out of range. Protocol log shows the failure happens at the place of index 81.

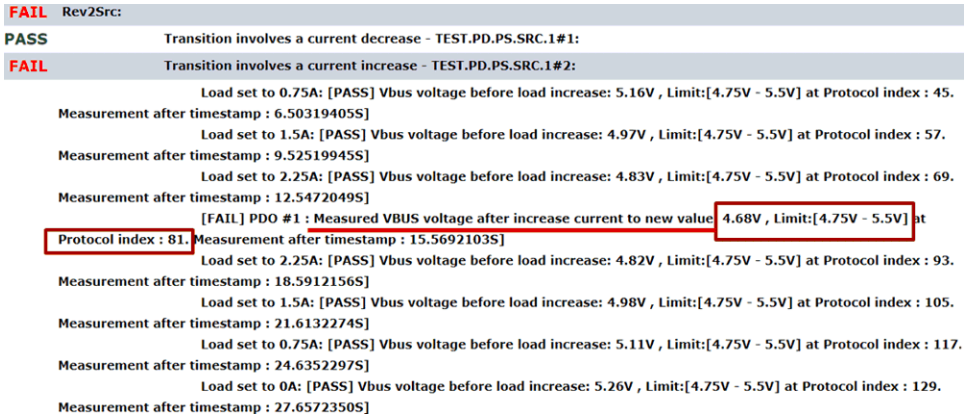

Figure 5-5. XML data log of TEST.PD.PS.SRC.1

Further, check the data log .grltrace or LeCroy .usb file. Spot packet 81. The packet indicates requested operating current is 3A. Waveforms log shows more clearly of the process. By initial analysis, the issue is related to cable compensation deficiency. After improving cable compensation level, test passes.

Figure 5-6. GRL-C2 Log of TEST.PD.PS.SRC.1

During compliance test procedures, various issues or concern shall encounter. Above 3 cases are some general analysis process. Additionally, some failures are tester issues instead of being introduced by products or silicon. Furthermore, due to continuous updates of PD specification or PD compliance test specification, some tests can be waived. Please ask USB-IF for waiver if necessary. Refer to references for more details.

6 Summary

This app note describes certification tests of PD products TPS257xx-Q1 by three elements, VIF configuration, compliance test, QuadraMAX test. This document introduces several related tools needed for data log analysis and some tips for VIF configuration. Check the latest PD compliance spec and test instruments versions or software versions. Download the latest GUI and claim the latest patch for testing or certification to influence test results heavily.

7 References

1. Texas Instruments, *USB Power Delivery - Compliance Tests* application report.
2. Texas Instruments, *TPS257XX-Q1-GUI* tool.
3. USB Compliance, *USB-IF Compliance Updates* article.
4. Granite River Labs, *Download Center* web page.
5. Teledyne Lecroy, *Protocol Test Solutions Software* web page.
6. USB, *USB Type-C and Power Delivery Source Power Requirements Test Specification* web page.
7. USB, *QuadraMAX PPS Test Manual* web page.
8. USB, *USB Vendor Info File Generator* web page.

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