Application Note

Powering Xilinx® Zynq® UltraScale+® MPSoCs With the TPS65219 PMIC

Power Management IC

ABSTRACT

This application note can be used as a guide for integrating the TPS65219 power management integrated circuit (PMIC) into a system powering the Xilinx® Zynq® UltraScale+® line of MPSoCs. The document outlines the benefits of the PMIC and provides example power maps for each supply consolidation designs to assist with the design process. For any questions or technical support, use the Power Management E2E design support forum.

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Trademarks

1 Introduction

Xilinx's Zynq UltraScale+ MPSoC line offers a high level of flexibility, with a range of devices that scale in complexity to work with a wide variety of applications. As such, the designs that power the Zynq UltraScale+ must be equally adaptable to meet the power needs of a complex line. This application note describes how TI's user programmable TPS6521*905* Power Management IC (PMIC) can be configured to meet the power requirements of the Xilinx® Zynq® UltraScale+®. The MPSoC integrates independent power domains that can be isolated for low power mode implementation, reducing the overall power consumption. When applications do not require the use of low power modes, the power domains can also be combined, reducing the amount of rails that are needed and allowing to reduce the BOM size/cost of the power design.

PMIC and SoC data sheets provide recommended operating conditions, electrical characteristics, recommended external components, package details, register maps, and overall component functionality. In the event of any inconsistency between any user's guide, application report, or other referenced material, the data sheet specification is the definitive source.

2 TPS65219 Overview

The TPS65219 is a cost and space optimized PMIC. TPS65219 integrates 3 Buck regulators, 4 Low Drop-out Regulators (LDO), GPIO, multi-function pins and I2C communication. The power and digital resources can be configured to meet the requirements of a variety of applications. The GPIO can be configured to enable or disable external discrete ICs when needed. This device has two package options: 4mm × 4mm 0.4m pitch VQFN package or 5mm × 5mm 0.5m pitch VQFN package. Table 2-1 shows a summary of the power resources.

The TPS6521905 is the user programmable version that comes with all Bucks and LDOs disabled by default to provide freedom to customize the desired output voltages, sequencing and more from start up to fit the system needs. For applications that require 7+ rails, this PMIC also offers a multi-PMIC configuration which allows to synchronize the sequence of 2x TPS65219 devices. The small package options, the highly integrated resources and configuration flexibility makes the TPS65219 PMIC a full power package to supply the Zynq UltraScale+ for the largest range of ZU+ devices, from ZU2CG all the way through ZU19EG. For more information on the different ZU+ devices, please refer to the Xilinx Zynq UltraScale+ site. Table 2-2 shows a summary of the main available resources to assist with the design process and the PMIC NVM programming. For any questions or technical support, use the Power Management E2E design support forum.

Table 2-1. TPS65219 Power Resources

	Input Voltage	Output Voltage	Current Capability	Comments
BUCK1	2.5V - 5.5V	0.6V - 3.4V	3.5A	• 2.3MHz switching frequency (auto-PFM or forced-PWM) • Dynamic voltage scaling • Configurable bandwidth. Low bandwidth for a smaller output capacitance (lower cost) or high bandwidth to support higher transient (higher performance). • Programmable power sequencing and default voltages. • Integrated voltage supervisor for undervoltage and current limit.
BUCK2	2.5V - 5.5V	0.6V - 3.4V	2A	
BUCK3	2.5V - 5.5V	0.6V - 3.4V	2A	
LDO1	1.5V - 5.5V (LDO, Load-Switch) 1.5V - 3.4V (Bypass)	0.6V - 3.4V (LDO) 1.5V - 3.4V (Bypass)	400mA	• Programmable power sequencing and default voltages. • Configurable as LDO, load switch or bypass-mode. • Integrated voltage supervisor for undervoltage and current limit
LDO2	1.5V - 5.5V (LDO, Load-Switch) 1.5V - 3.4V (Bypass)	0.6V - 3.4V (LDO) 1.5V - 3.4V (Bypass)	400mA	
LDO3	2.2V - 5.5V	1.2V - 3.3V	300mA	• Programmable power sequencing and default voltages. • Configurable as LDO or load switch • Integrated voltage supervisor for undervoltage and current limit.
LDO4	2.2V - 5.5V	1.2V - 3.3V	300mA	

Table 2-2. TPS6521905 Programming Resources

Resources	Links
Programming Guide	TPS65219 Non-Volatile Memory (NVM) Programming Guide
Graphical User Interface (GUI)	TPS65219 graphical user interface
Socketed EVM	TPS65219 non-volatile memory (NVM) programming board
Programming Tutorial Video	Programming the TPS6521905
TPS6521905 data sheet	User-programmable power management IC (PMIC) with three step-down DC/DC converters and four LDOs

3 Power Delivery Networks

The Xilinx UltraScale MPSoCs require multiple power rails to support a variety of features. Some of the power domains can be consolidated to optimize the power design in terms of cost, efficiency or performance. This section describes the Power Delivery Network (PDN) for each of the power supply consolidations. All PDN use TPS65219 (user-programmable) which can be configured and optimized to meet different application needs. In addition to this applications note, TI also provides the PMIC NVM configuration files to assist with the design process. These NVM files have the default register settings that are used on each power delivery network (PDN) and can be easily uploaded into the TPS65219-GUI for re-programming.

Table 3-1 shows the options for power supply consolidation based on the speed grade. The power design on each PDN follows the recommended PL power supply sequencing to help achieve minimum current draw and to make sure the I/Os are 3-stated at power-on.

Table 3-1. Power Supply Consolidation

Power Supply Consolidation	Speed Grade	Power Delivery Network (PDN)
Always On: Optimized for Cost	-1 and -2 Devices	Section 3.1
Always On: Optimized for Power/Efficiency	-1L and -2L Devices	Section 3.2
Always On: Optimized for PL Performance	-3 Devices	Section 3.3
Full Power Management Flexibility	All Speed Grades/Devices	Section 3.3

3.1 Always ON: Designed for Cost (-1 and -2 Devices)

The always ON/cost designed power supply consolidation uses the -1/-2 speed grade devices. This power scheme allows to consolidate the 0.85V domains. When VCCINT and VCCINT_IO/VCCBRAM operate at the same voltage levels, they can be powered by the same supply and ramped simultaneously. If the maximum total current of all the power domains supported by *External1* and the PMIC DCDC1 does not exceed 3.5A, all these domains can be supplied by DCDC1. Alternatively, all the 0.85V domains can be supplied by the *External1* and the DCDC1 from the PMIC can be re-programmed to supply other power domains in the application.

Note

If all the 0.85V domains are supplied by *External1*, the PMIC Buck1 can be re-programmed to output 3.3V and used to supply the PMIC LDOs to help reduce the power consumption.

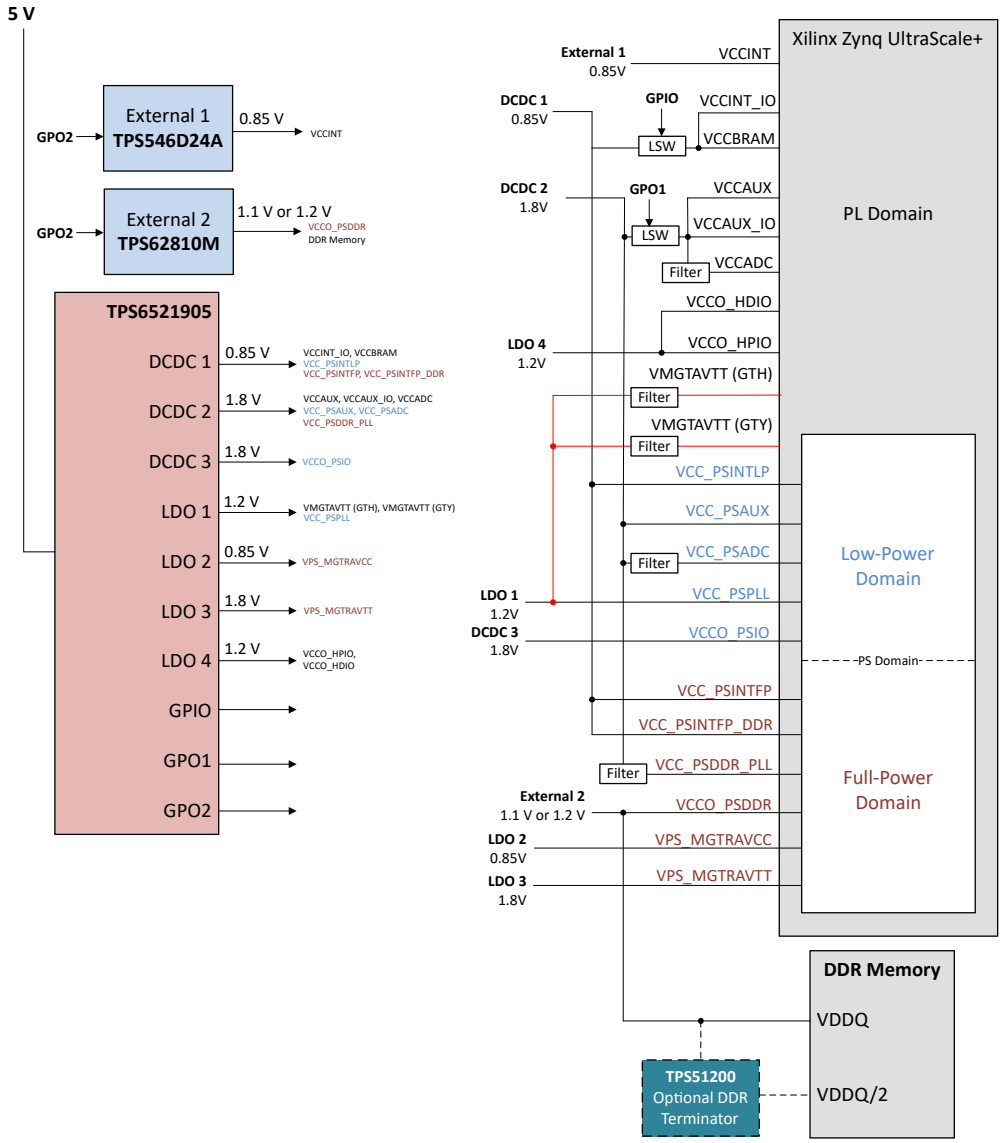

Figure 3-1. Designed for Cost (-1 and -2 Devices) PDN

Note

Designed for Cost (-1 and -2 Devices): TPS6521905 PMIC NVM configuration file link.

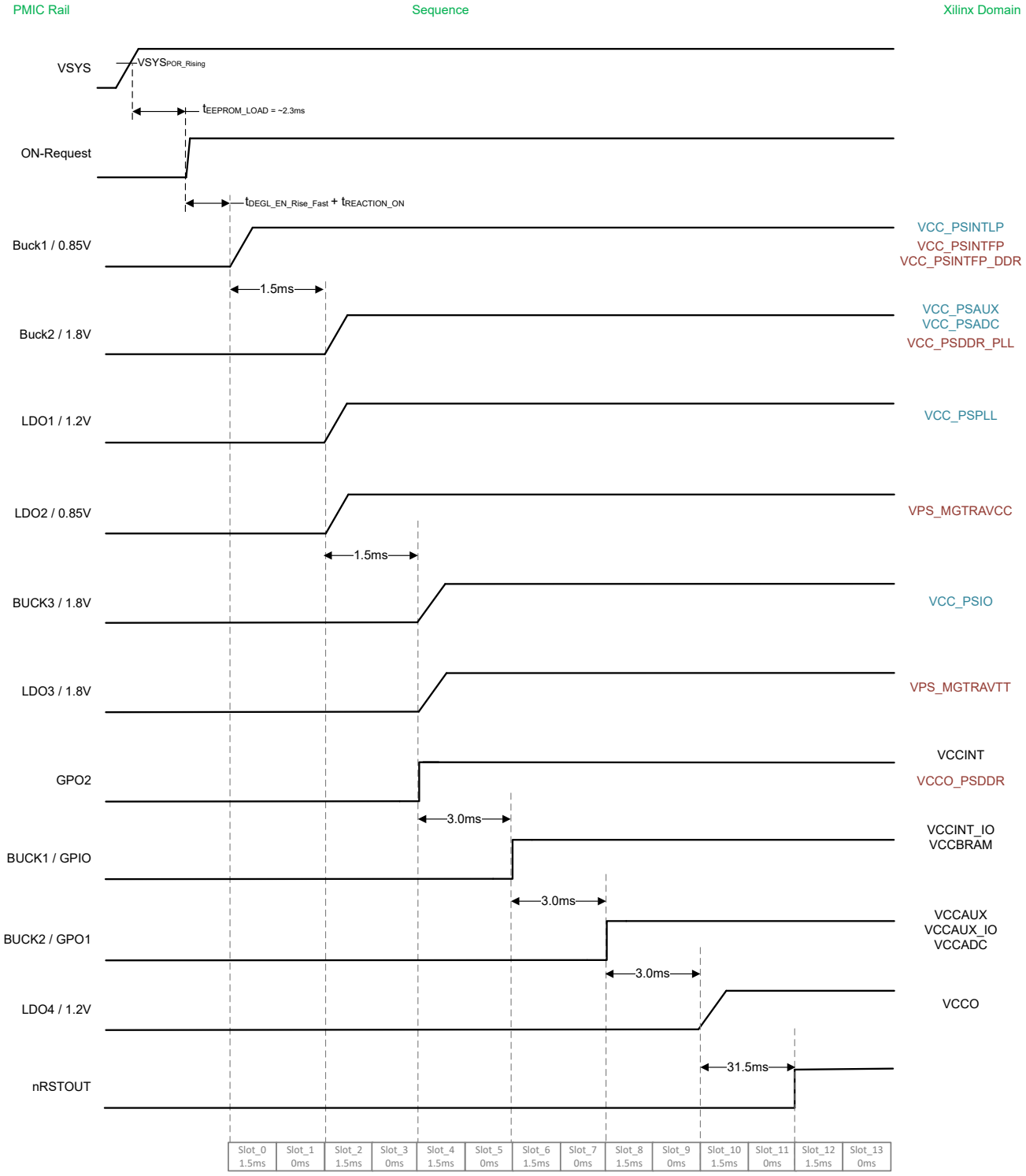

Figure 3-2. Designed for Cost (-1 and -2 Devices) Power-Up Sequence

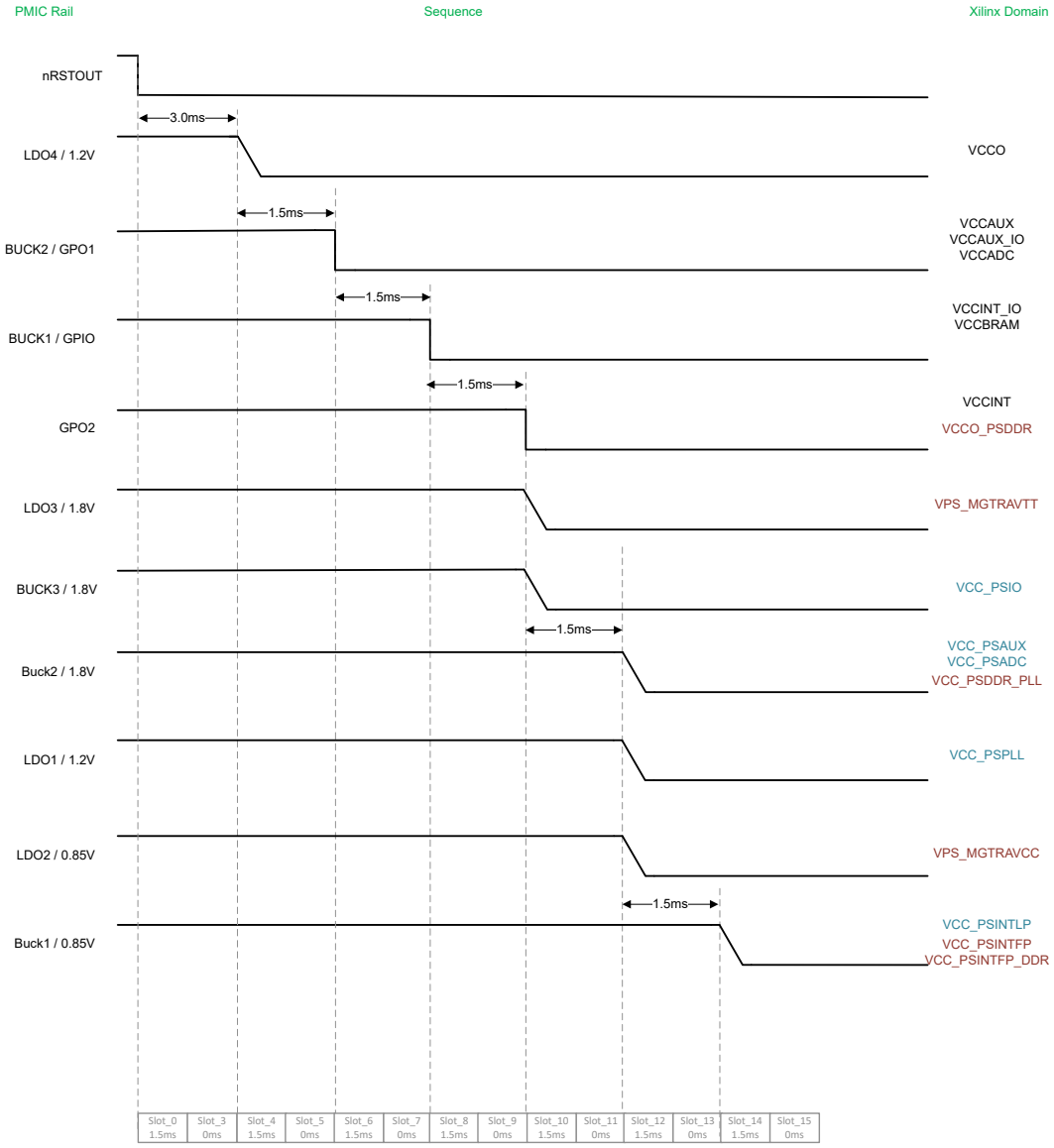

Figure 3-3. Always ON: Designed for Cost (-1 and -2 Devices) Power-Down Sequence

3.2 Always On: Designed for Power and or Efficiency (-1L and -2L Devices)

The always ON-power/efficiency designed power supply consolidation uses the -1L/-2L speed grade devices. This power scheme is similar to the cost optimized optimization. The -1L and -2L devices allow to run VCCINT at 0.72V which helps to reduce power consumption and improve efficiency.

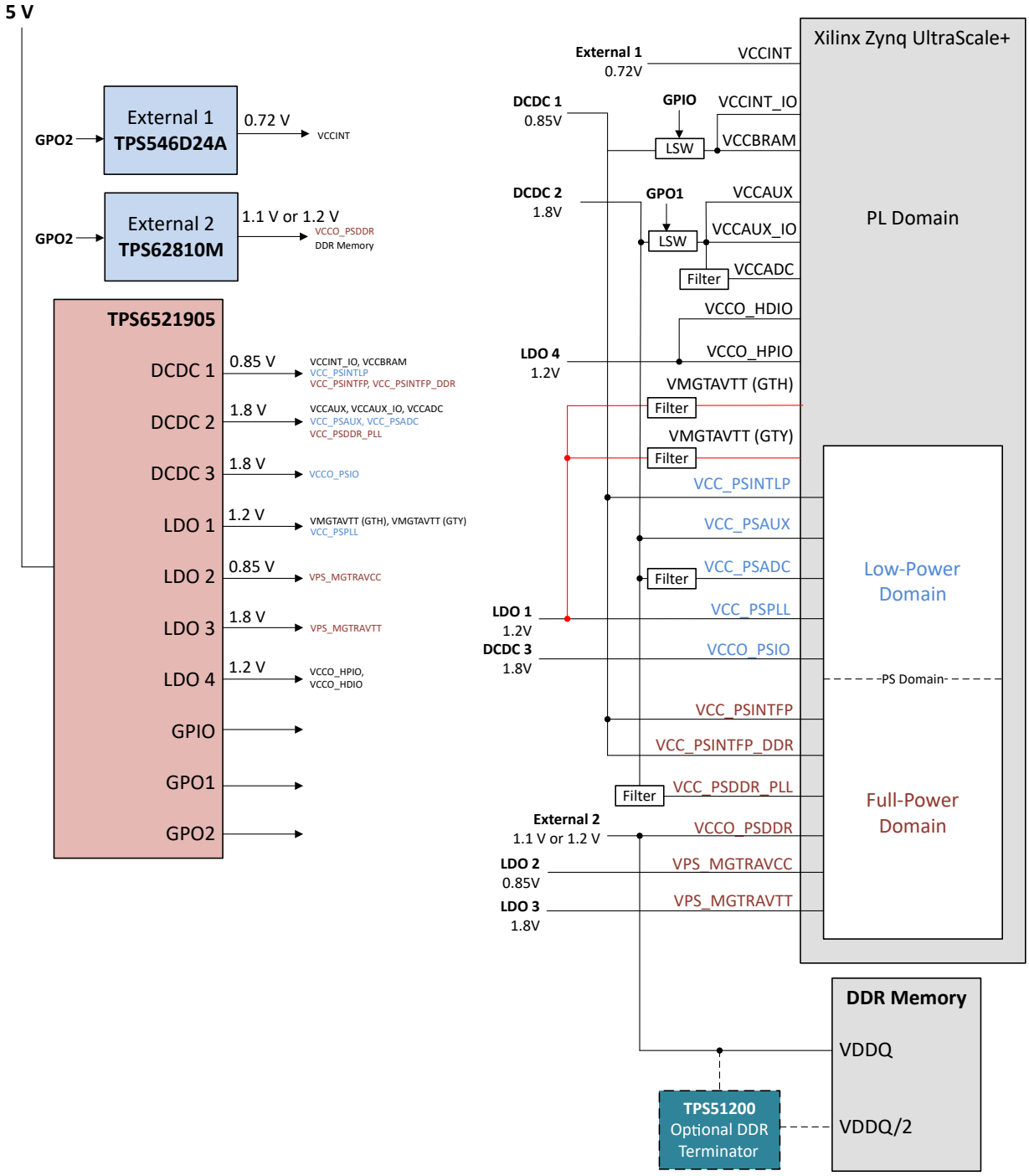

Figure 3-4. Designed for Power and or Efficiency (-1L and -2L Devices) PDN

Note

Designed for Power and or Efficiency (-1L and -2L Devices): TPS6521905 PMIC NVM configuration file link.

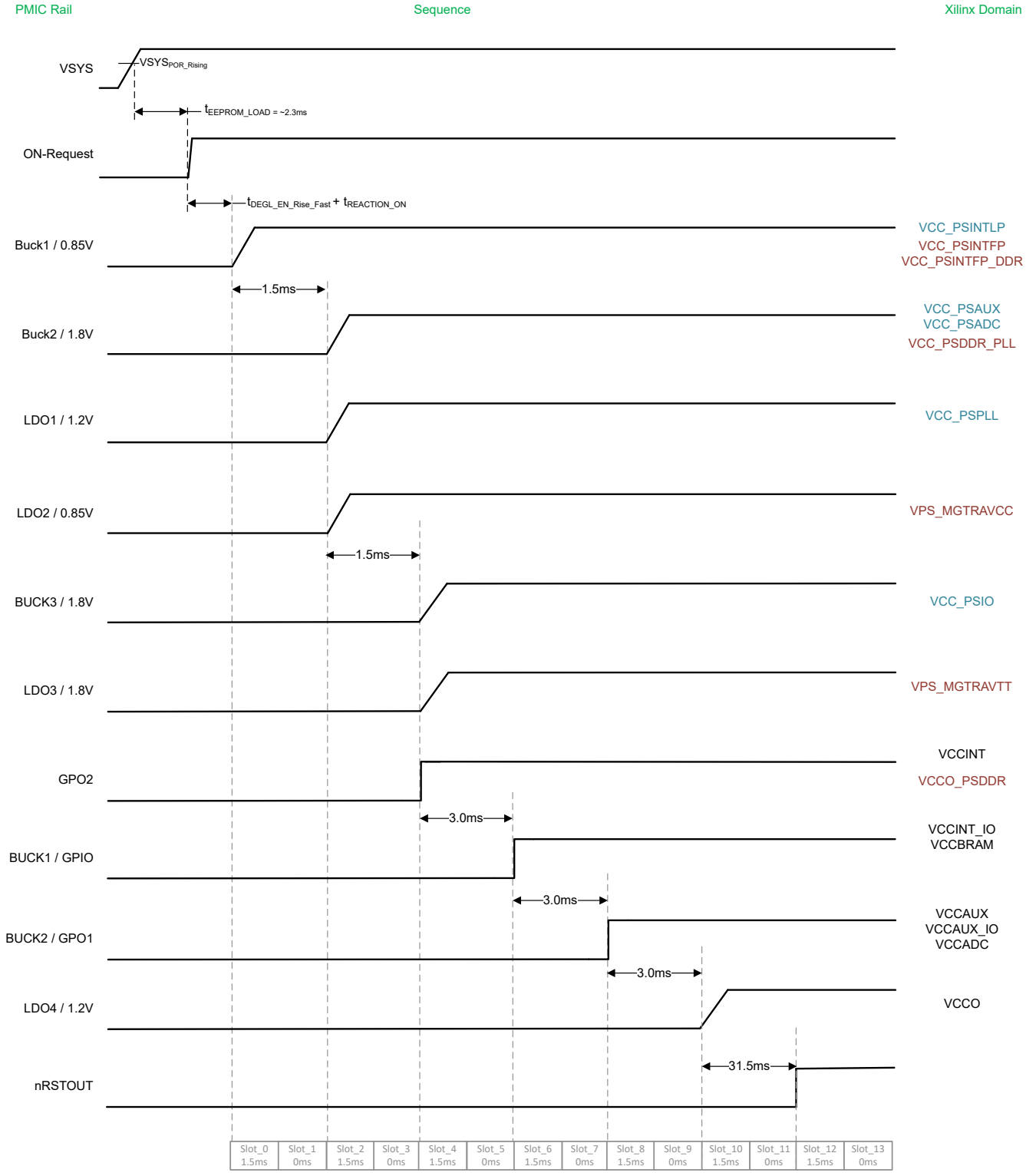

Figure 3-5. Designed for Power and or Efficiency (-1L and -2L Devices) Power-Up Sequence

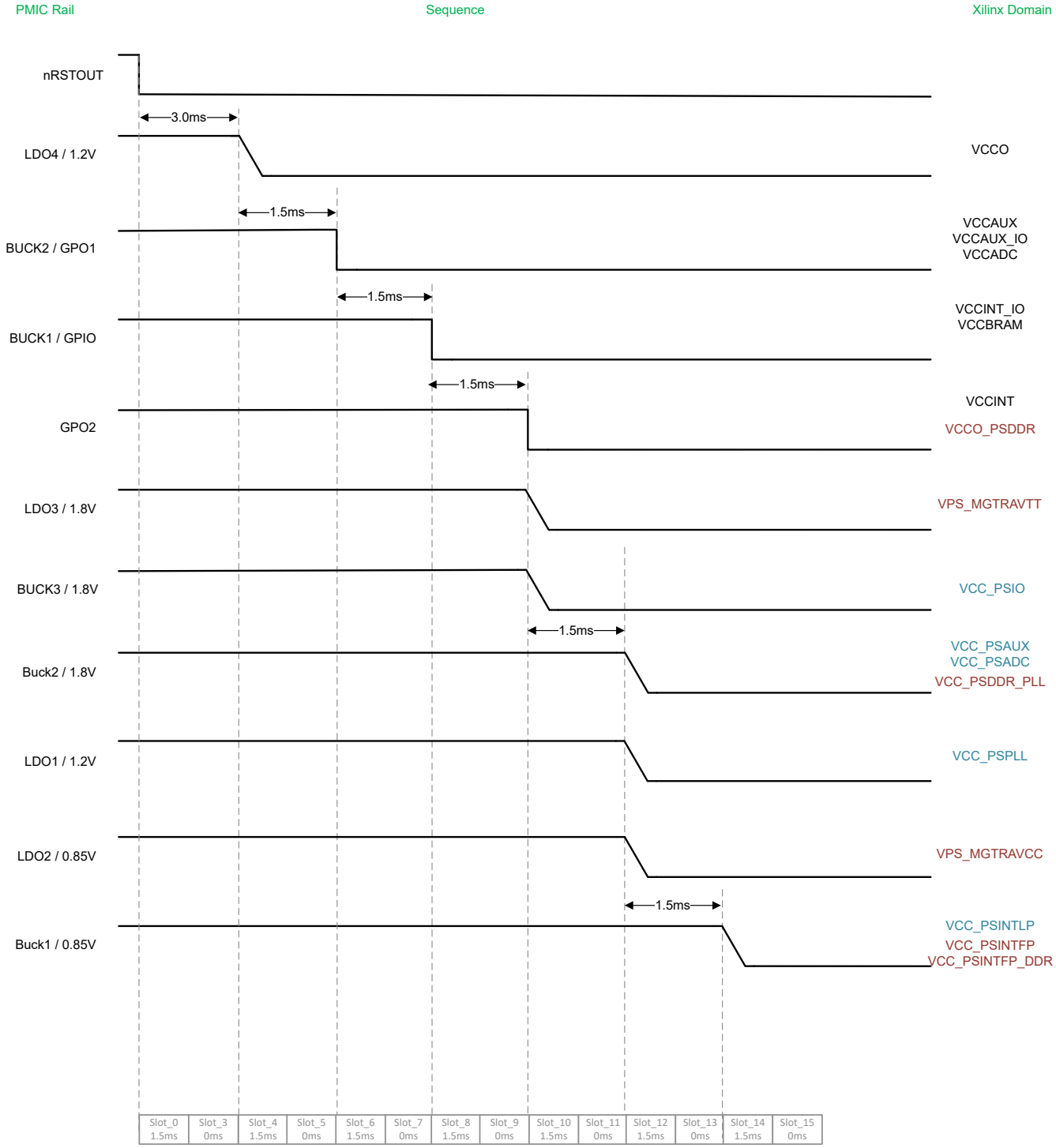

Figure 3-6. Designed for Power and or Efficiency (-1L and -2L Devices) Power-Down Sequence

3.3 Always On: Designed for PL Performance (-3 Devices)

The Always ON-Programmable Logic (PL) performance designed for power consolidation supports the highest PL performance and uses -3 speed grade devices. In this power scheme, all the core rails (VCCINT, VCCINT_VCU, VCCBRAM, VCCINT_IO, VCC_PSINTLP, VCC_PSINTFP, and VCC_PSINTFP_DDR) are run at a nominal voltage of 0.9V.

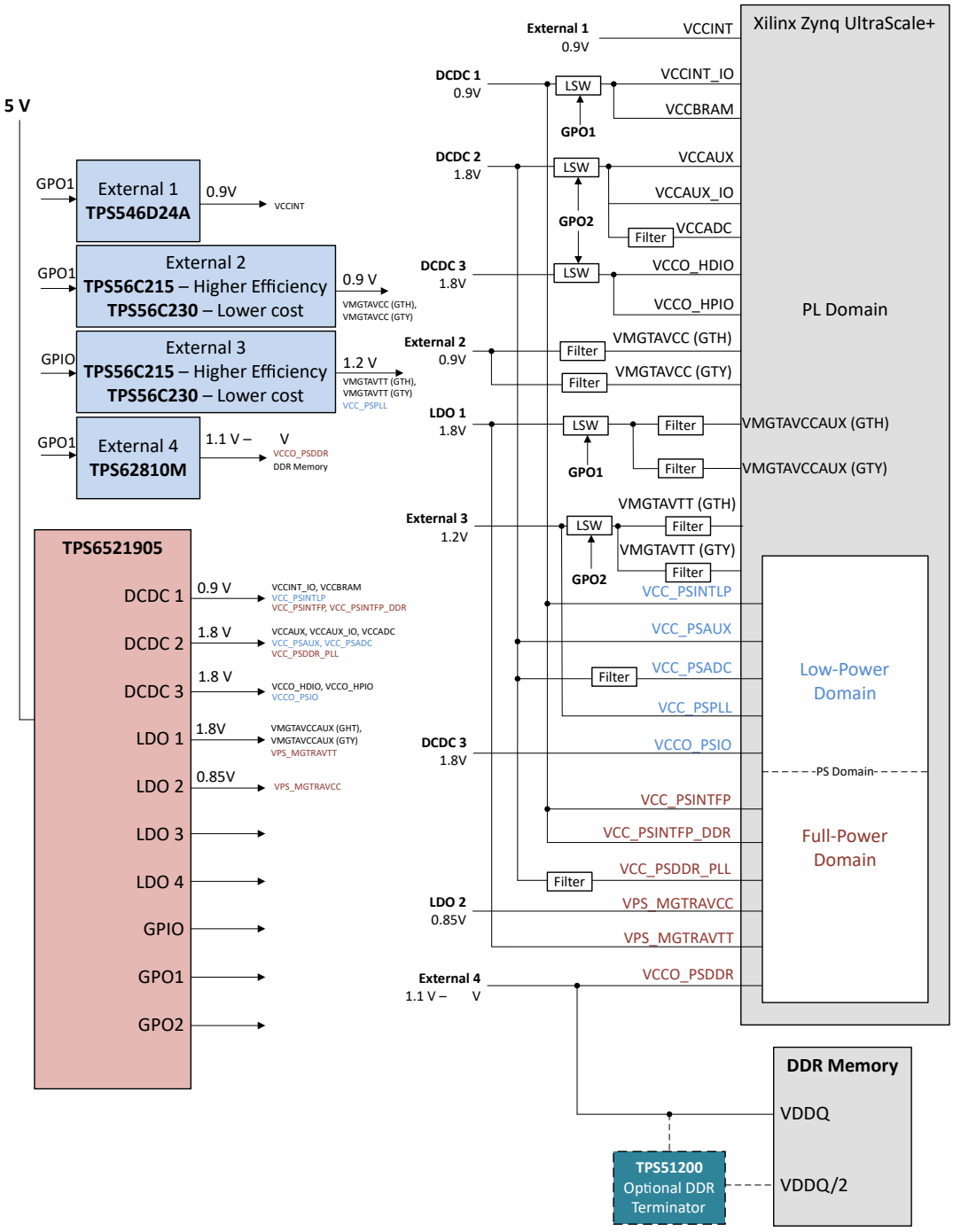

Figure 3-7. Designed for PL Performance (-3 Devices) PDN

Note

Designed for PL Performance (-3 Devices): Please request TPS6521905 PMIC NVM configuration file on the TI Power Management E2E forum.

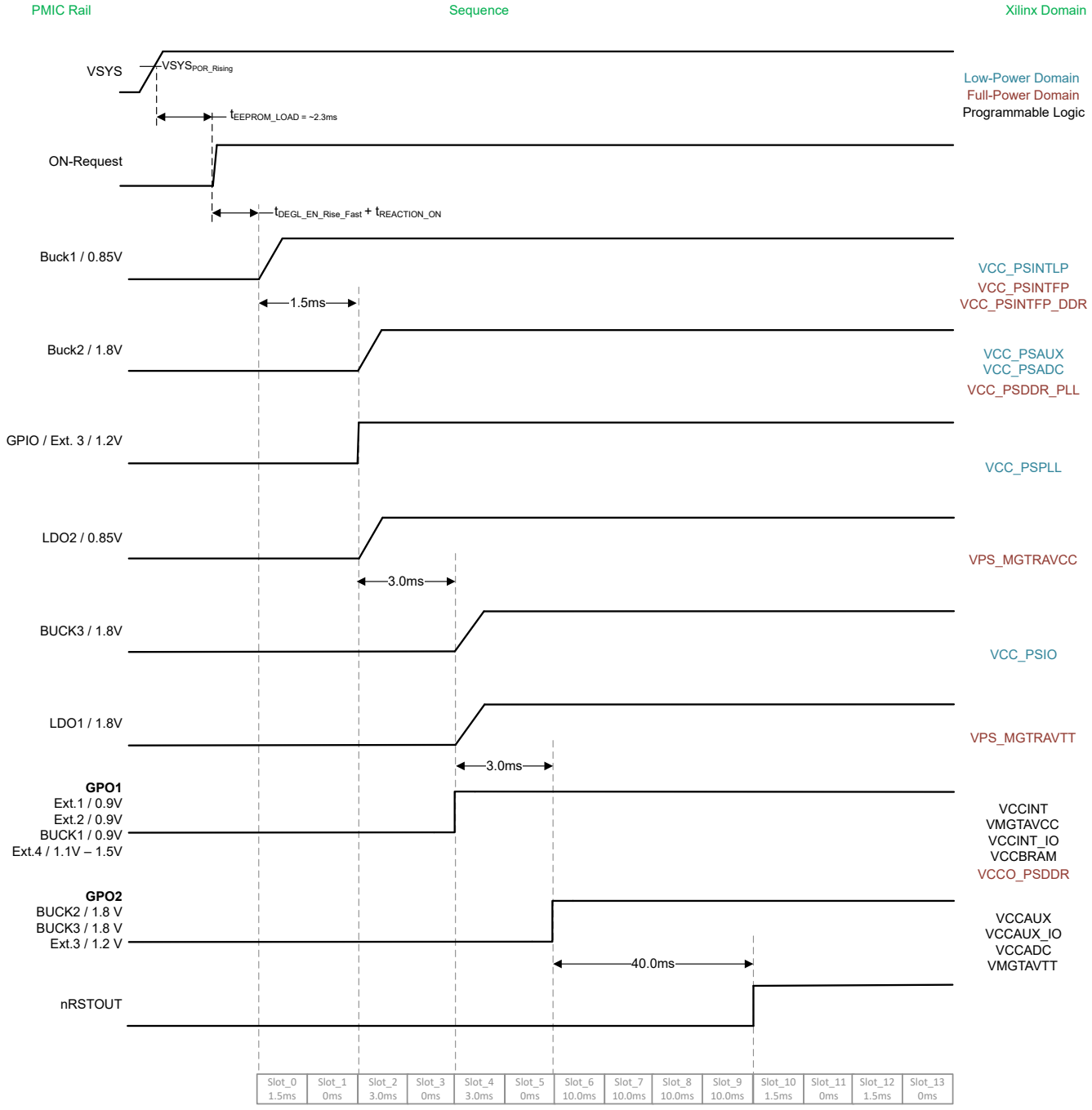

Figure 3-8. Designed for PL Performance (-3 Devices) Power-Up Sequence

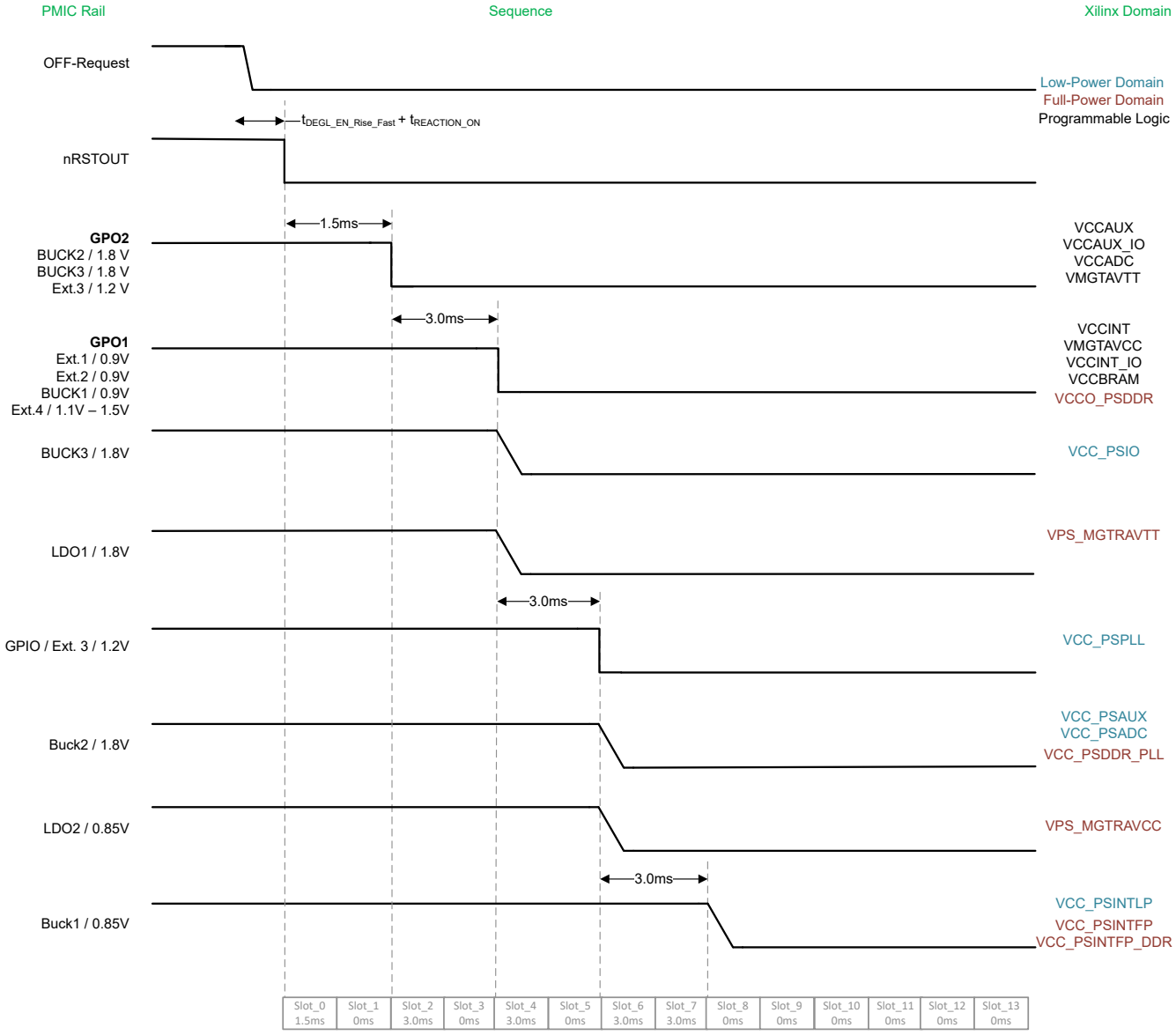

Figure 3-9. Designed for PL Performance (-3 Devices) Power-Down Sequence

3.4 Full Power Management Flexibility (All Speed Grade)

The *Full Power Management flexibility* can be supported with all the speed grade devices. This power scheme significantly reduces the power domain consolidation but allows to use ultra-low power states to reduce overall power consumption and/or maximize battery life. Figure 3-10 shows the TPS65219 multi-PMIC configuration + discrete ICs to powering Xilinx Zynq UltraScale+. This PDN shows how the application can isolate the four independent domains (LPD, FPD, PLPD and BPD) to disable specific power rails when unused.

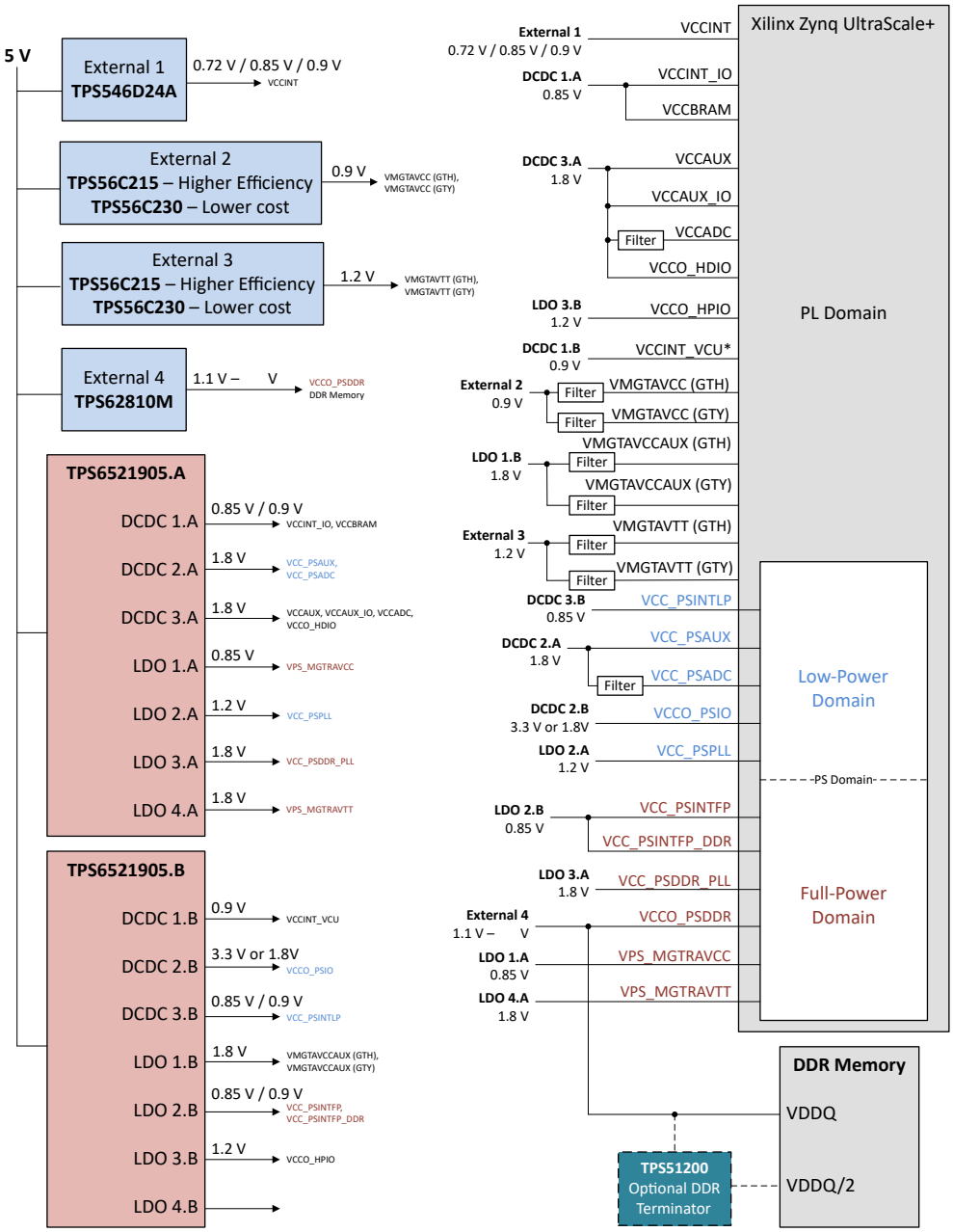

Figure 3-10. Full Power Management PDN

Note

Full Power Managment: Please request TPS6521905 PMIC NVM configuration file on the TI Power Management E2E forum.

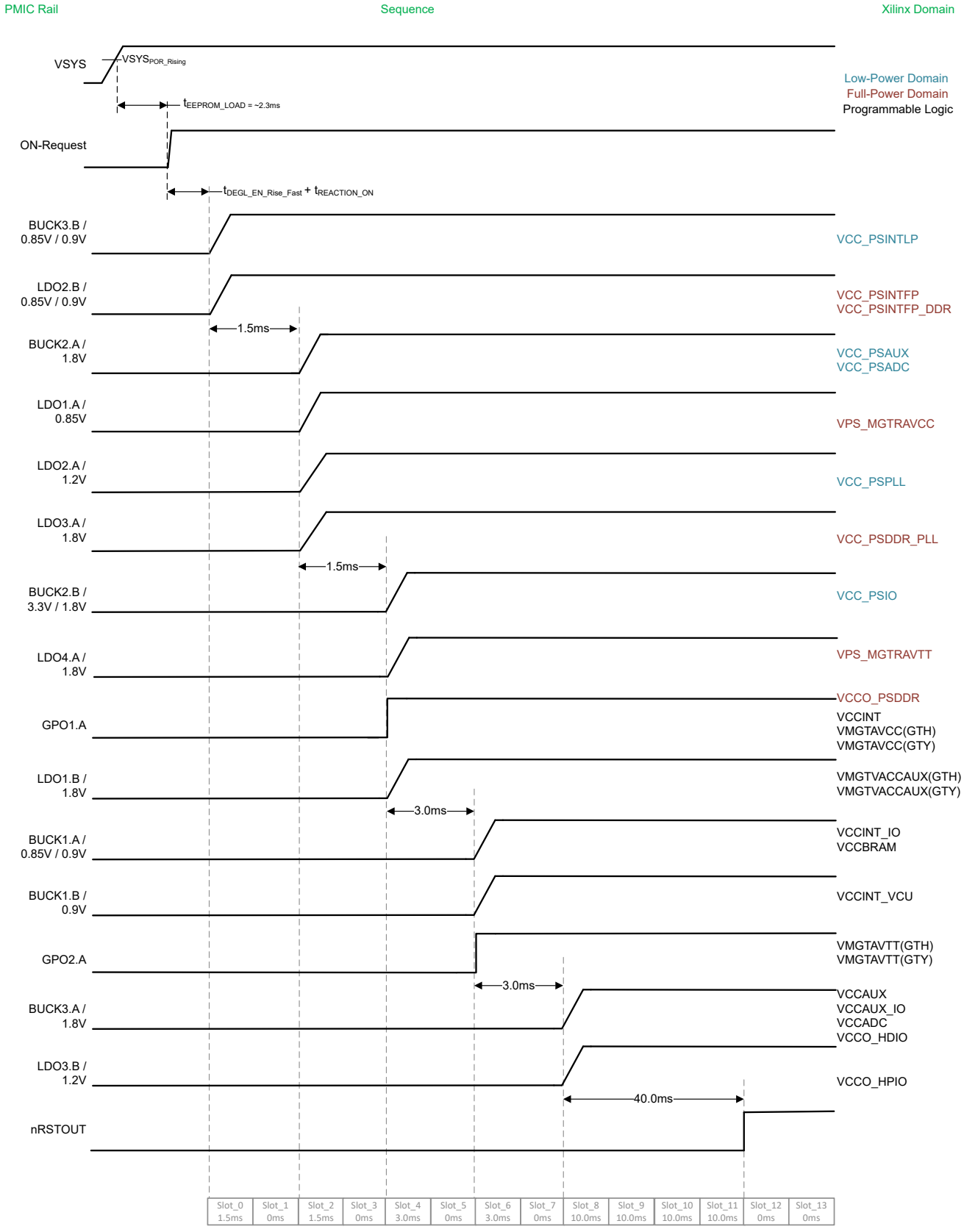

Figure 3-11. Full Power Management - Power-Up Sequence

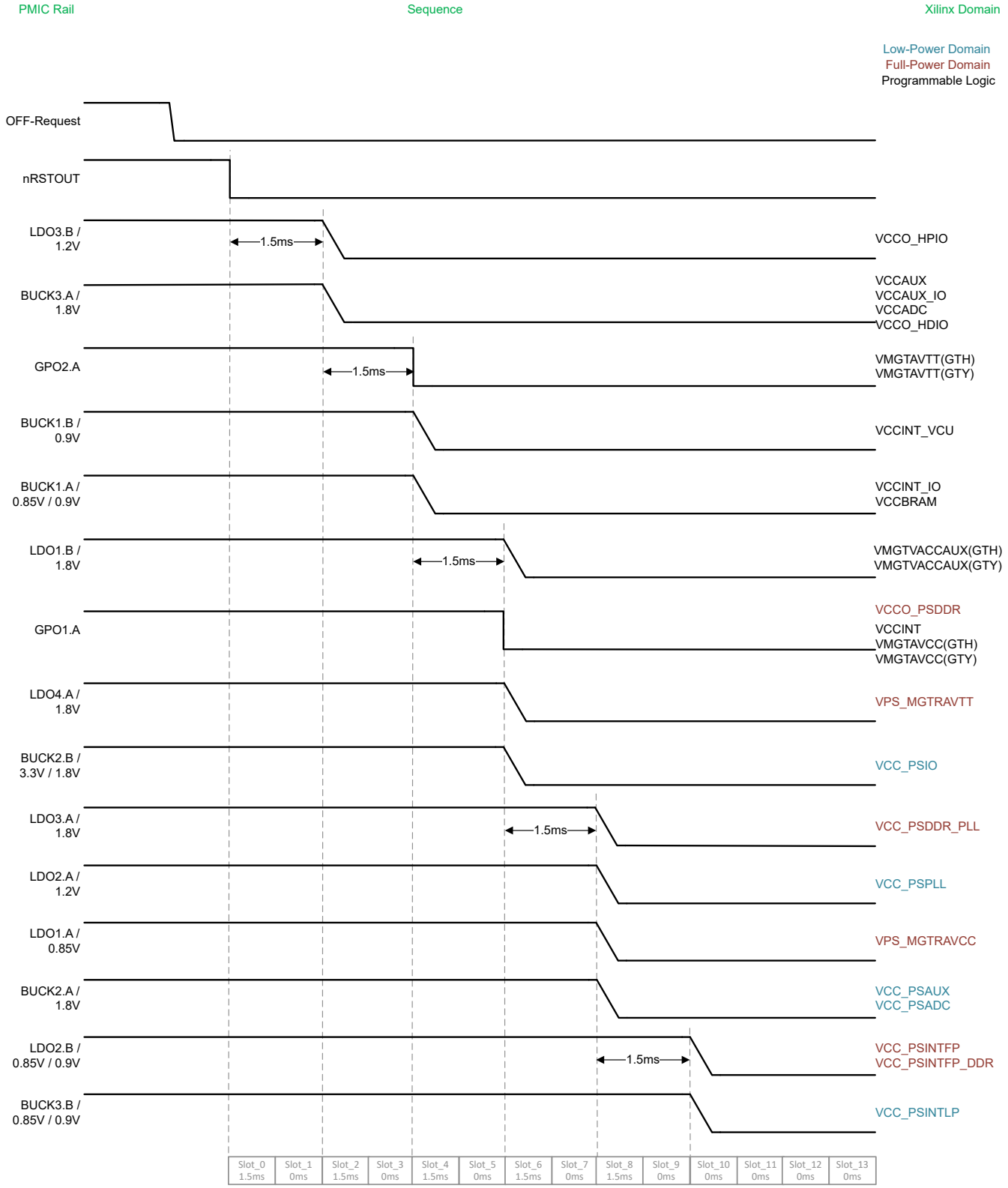

Figure 3-12. Full Power Managements - Power-Down Sequence

4 Loading a NVM Configuration File to PMIC

The diagram shown in Figure 4-1 describes the process to load a pre-configured NVM file (.CSV or .JSON extension) into the PMIC NVM. The soldered down EVM (TPS65219EVM) is used as a reference but the socketed EVM can be used as well. The TPS6521905 product page on ti.com has multiple NVM files that are pre-configured to meet the requirements of specific processors or SoCs. These can be found under *Design tools and simulations*. TI's customers can reuse these files to re-program the PMICs on their production line or by working with a distributor.

Note

If the pre-configured NVM files do not meet all the application requirements, the NVM files can still be loaded to the TPS65219-GUI, make the necessary changes, and generate a new NVM file using.

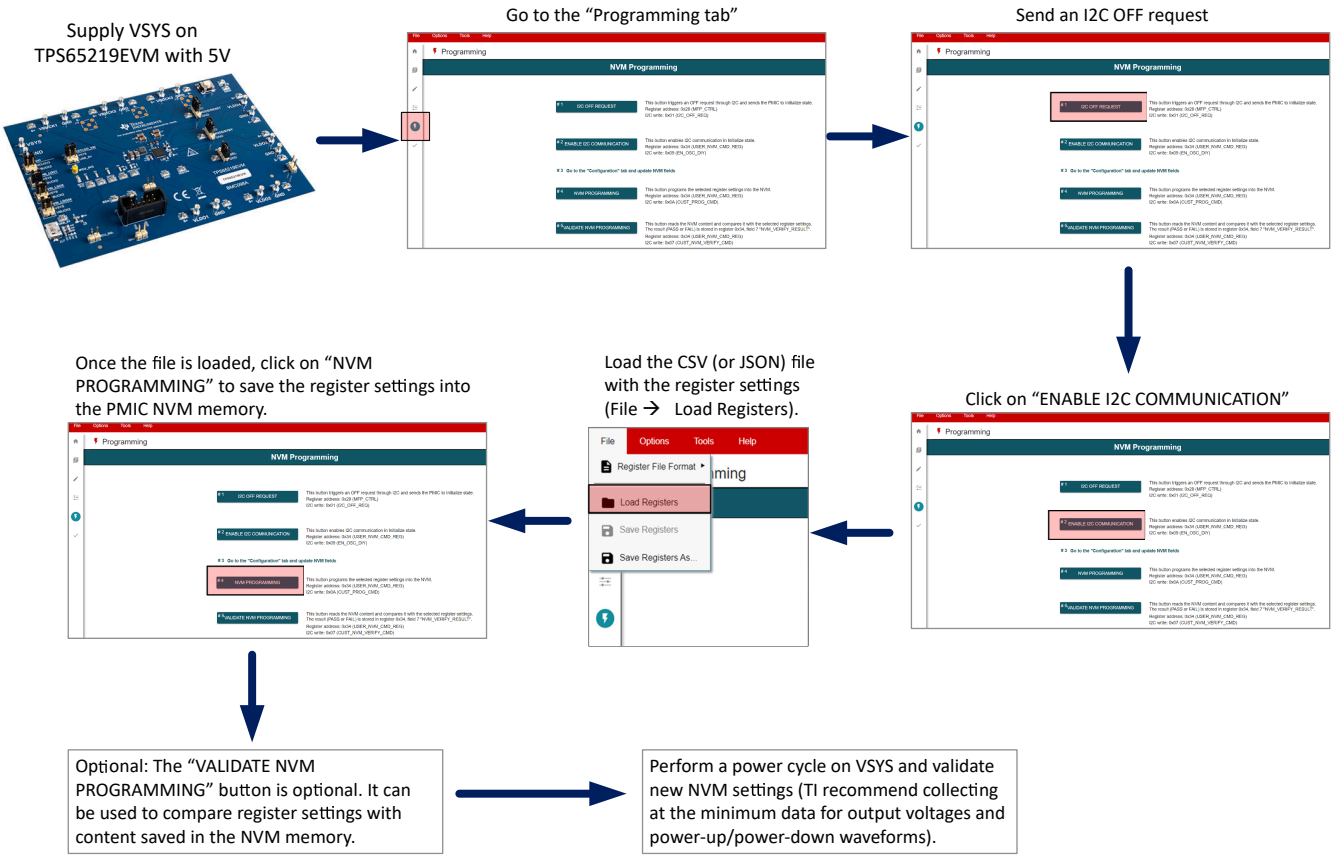

Figure 4-1. Loading NVM Configuration File

5 Summary

The TPS6521905 power management IC (PMIC) integrates flexible analog and digital resources that can be programmed to meet the power requirements of the different supply consolidations of the Xilinx's Zynq UltraScale+ MPSoC. The PMIC programmable NVM memory allows for rapid prototyping and a faster time to market. This PMIC combined with discrete offers a competitive scalable small BOM and low cost power design.

6 References

- Texas Instruments, *User Programmable Power Management IC (PMIC) with Three Step-down DC/DC Converters and Four LDOs*, data sheet.
- AMD Xilinx, *Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics (DS925)*.
- AMD Xilinx, *UltraScale Architecture PCB Design User Guide (UG583)*.

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