Application Note

Analyzing Butterfly-Style Footprint and Input Capacitor Removal Effects

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ABSTRACT

This application note delves into the unique symmetrical butterfly-style footprint of the TPS54KB2x, a highly efficient synchronous buck converter. Experimental data uncovers design intricacies and trade-offs, offering insights into the use for industrial and enterprise applications. The report explores how this footprint minimizes parasitics and the impact of removing input capacitors on one side of the IC package.

Table of Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The report objective is to interpret the distinctive butterfly-style footprint of the TPS54KB20 and how it is affected by removal of input capacitors from one side of the IC, resulting in an asymmetrical configuration. This particular buck converter falls under the TPS54KB2x device family, using an adaptive on-time D-CAP4 control mode, and supporting up to 25A of output current. TPS54KB2x's butterfly footprint proves to exhibit greater efficiency and enhanced device performance compared to its predecessor part. Considering users may seek the reduction of input capacitors to achieve further design flexibility, this device family allows the possibility of using a single VIN rail along with removing numerous input capacitors on one side of the IC package. This application note provides data on how further input capacitor reduction can affect efficiency and SW-node ringing during operation. Bench data is documented presenting SW-node ringing and efficiency results of the alternative input capacitor configuration. The report analyzes the TPS54KB20 SW-node ringing trade-offs when removing input capacitors asymmetrically on one side of the device, reducing area and cost. The data in this report refers to the TPS54KB20 U2 design EVM.

2 Butterfly Footprint Analysis

The butterfly-style footprint is a unique feature to the TPS54KB2x that distinguishes the device from predecessor and competitor devices. The TPS54KB2x features two VIN ports parallel from across the IC package, and two PGND planes similarly parallel so that it resembles the shape of a butterfly, hence the name. The layout method carries advantages as it minimizes parasitics and noise. The parallel VIN and GND planes play a significant role in reducing the excess amounts of unwanted resistance and inductance. In addition, this high power density footprint allows for further performance enhancements including slightly increased efficiency, reduced switch-node ringing, and thermal/electrical specification refinement. In terms of layout area, the TPS54KB2x offers reduction in design size compared to its predecessor part due to the butterfly footprint's ability to compress component placement on the layout.

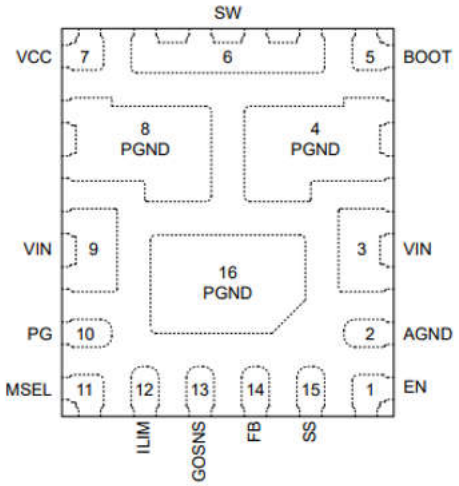

Figure 2-1. Butterfly-Style Outline

Figure 2-1 presents how the distinctive symmetrical layout appears in a pinout format. As previously mentioned, the footprint consists of two parallel VIN rails and two parallel PGND planes divided by the package symmetrically which aids in the reduction of parasitics. Furthermore, the butterfly footprint arranges the input capacitors in such a way that magnetic field cancellation occurs, leading to loop inductance being decreased.

Section 2.1 and Section 2.2 briefly show the efficiency and thermal advantages of TPS54KB20 compared to its predecessor part, TPS54JB20.

2.1 Efficiency

Figure 2-2 presents efficiency data comparing TPS54KB20 and its predecessor part, TPS54JB20. The measurements were taken under identical conditions and tested using internal VCC.

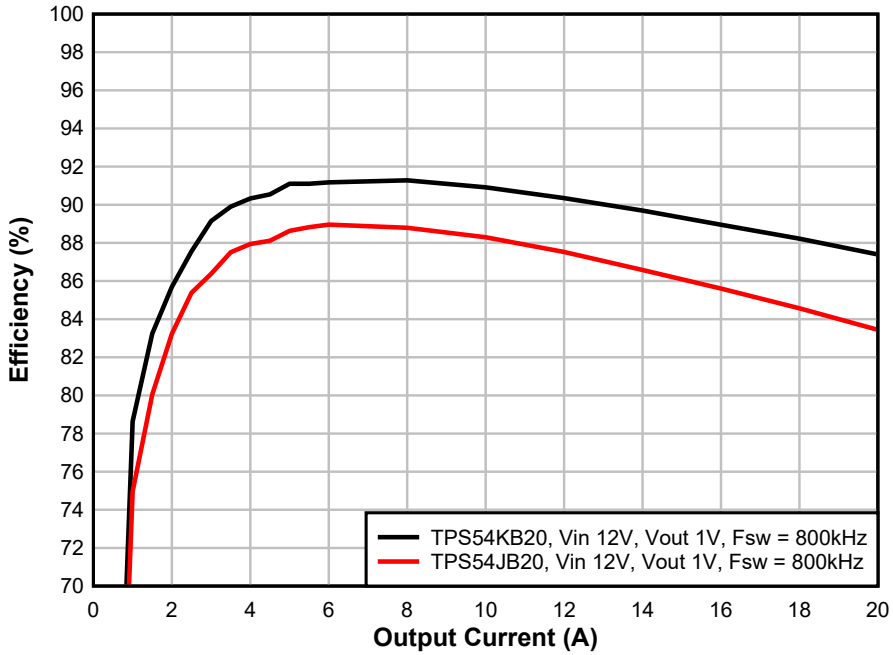

Figure 2-2. TPS54KB20 vs TPS54JB20 Efficiency

2.2 Thermal Performance

Figure 2-3 and Figure 2-4 show a thermal comparison between TPS54KB20 and TPS54JB20. The measurements were taken under identical conditions: 12V input, 1V output, and internal VCC.

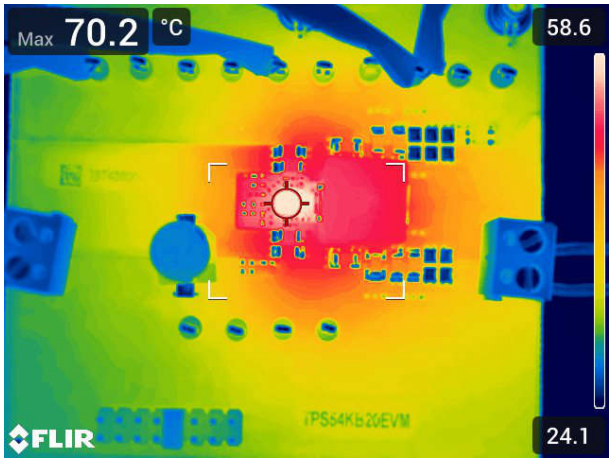

Figure 2-3. TPS54KB20 Thermal Characteristics, 800kHz, 20A Load

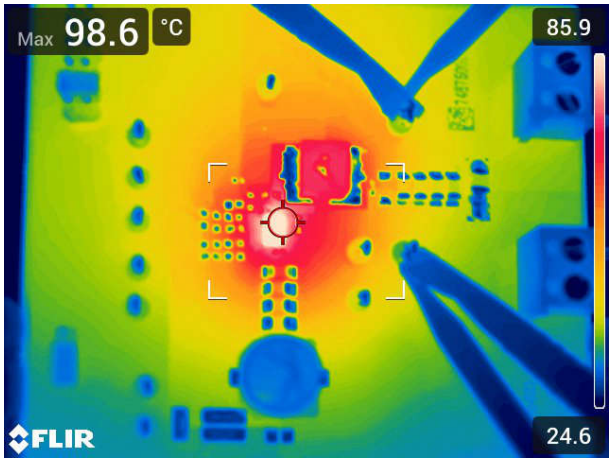

Figure 2-4. TPS54JB20 Thermal Characteristics, 800kHz, 20A Load

3 Symmetrical Footprint

The symmetrical butterfly layout with equal amounts of input capacitors on each side of the package is designed to function with minimal ringing on the SW-node. The recommended BOM layout is included in the default TPS54KB20 EVM, retaining equal amounts of capacitors on each side of the input. These proportional components make sure smaller amounts of SW-node and VIN-SW ringing are present when the device is actively switching under rated operating conditions. The low side and high side MOSFETS have proven to display smaller amounts of ringing on SW-node and VIN-SW when the default symmetrical EVM is tested.

Figure 3-1 depicts the recommended symmetrical schematic for TPS54KB20. Capacitors C21, C23, C37, and C39 have been prematurely removed as a result of the symmetrical EVM. The data provided is taken under the symmetrical TPS54KB20 EVM conditions using the capacitors shown in Figure 3-1.

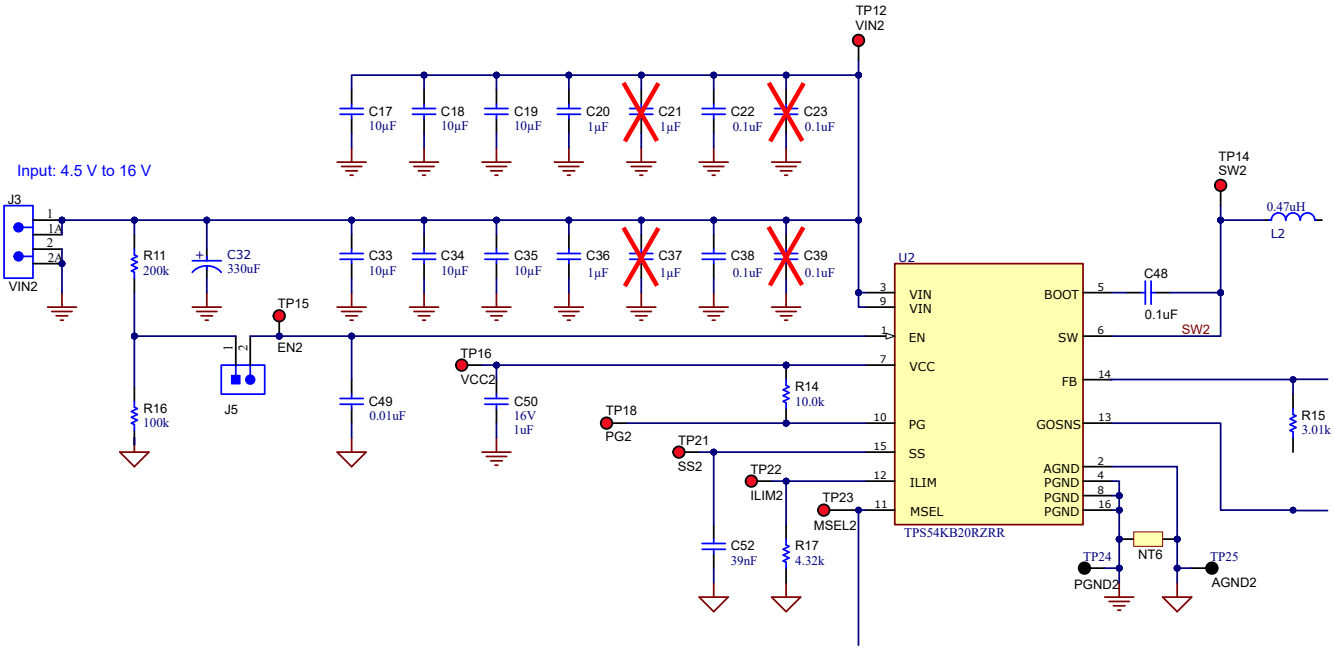

Figure 3-1. Symmetric Schematic

Figure 3-2 and Figure 3-3 are illustrated to represent the EVM symmetrical board layout with the recommended amount of input capacitors present.

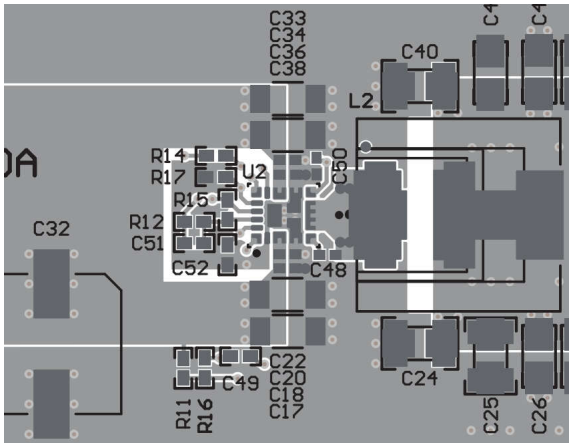

Figure 3-2. Top Layer Recommended Symmetrical Layout

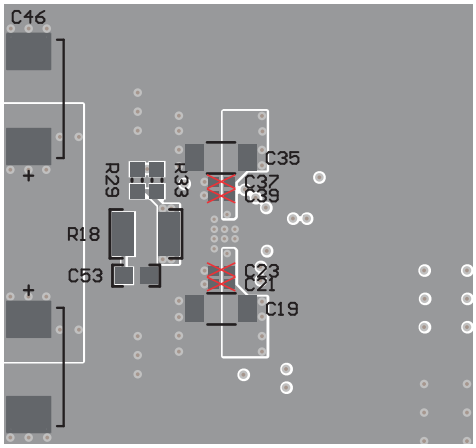

Figure 3-3. Bottom Layer Recommended Symmetrical Layout

4 Asymmetrical Footprint

Removal of input capacitors strictly on one side of the butterfly pinout provides flexibility to users who desire a cost-effective, one-sided input path. Some select system designs can require a VIN entry point exclusively through a single end of the package containing the majority of the capacitors, rather than a double-sided VIN package with capacitors on each end. Although removing a number of input capacitors on a single side allows for design flexibility, it also carries trade-offs in terms of SW-node ringing. Generally, greater SW-node ringing is present when a single VIN rail is used and a number of input capacitors are removed from one side of the package. One can balance the need for reducing SW-node noise and reducing design cost by removing the suggested amount of capacitors. If users choose to proceed with this layout method, the recommended component configuration consists of 4 x 10-µF capacitors, 1 x 1-µF capacitor, and 1 x 0.1-µF capacitor all on one side of the IC, while a single 0.1-µF capacitor will remain on the opposite side of the IC. Referring to Figure 4-1, removing capacitors C36, C35, C34, and C33 from Pin 9, while adding capacitor C100 to Pin 3, would successfully complete the asymmetrical configuration. Capacitors C21, C23, C37, and C39 are prematurely removed from the design. This represents an asymmetrical design with the majority of the input capacitors on a single pin. It is critical that the high frequency bypass capacitor, C38, remains on Pin 9 as this capacitor prevents excess noise and supresses voltage spikes on SW. The data provided is taken under the TPS54KB20 asymmetrical EVM conditions, using the capacitors shown in Figure 4-1 along with utilizing one VIN rail. It is not recommended to operate the asymmetrical configuration in the RAMP1 setting. At their own discretion, if users intend to remove capacitors on one end of the TPS54KB2x butterfly package, using a single asymmetric VIN pin, the recommended schematic and layout are shown in Figure 4-1, Figure 4-2, and Figure 4-3.

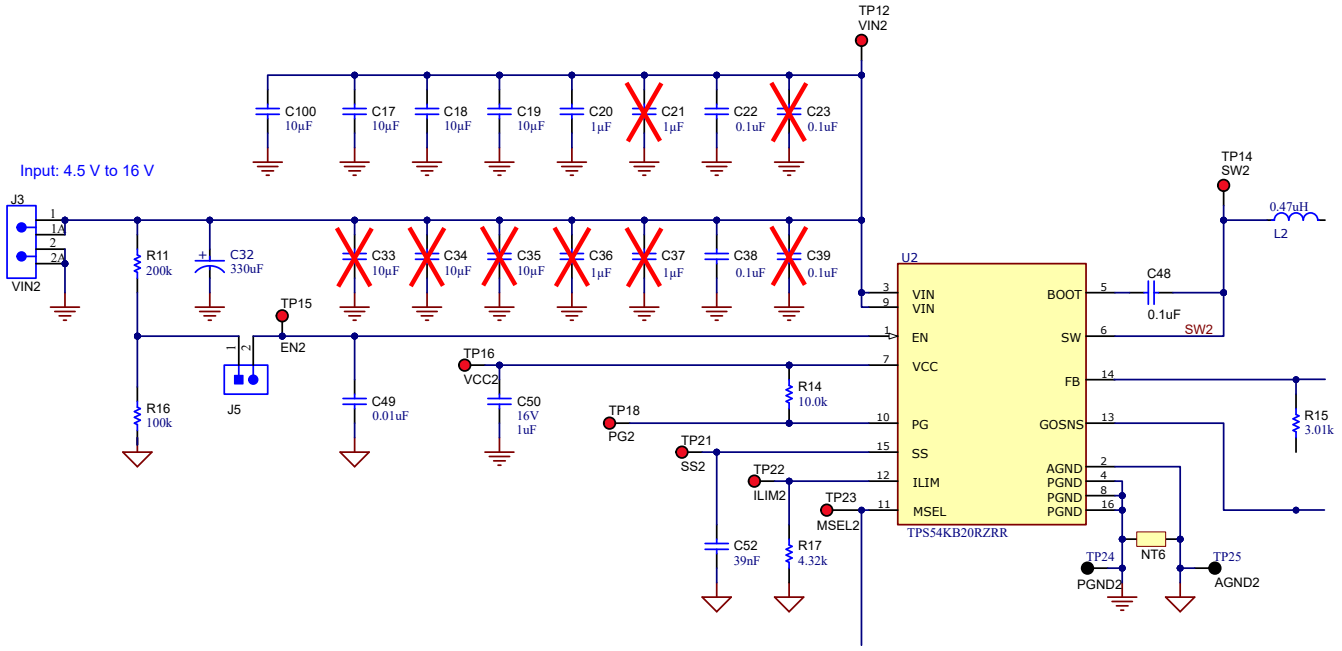

Figure 4-1. Recommended Asymmetric Schematic

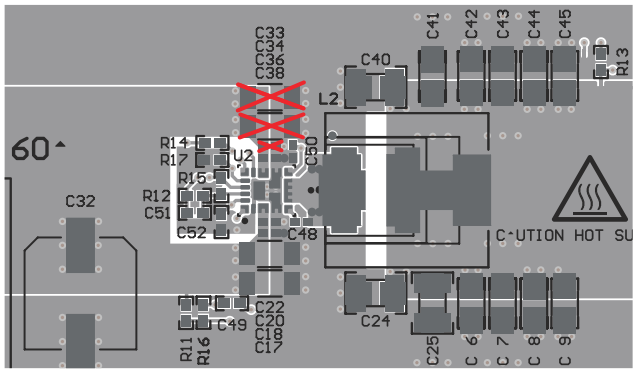

Figure 4-2. Top Layer Recommended Asymmetrical EVM Layout

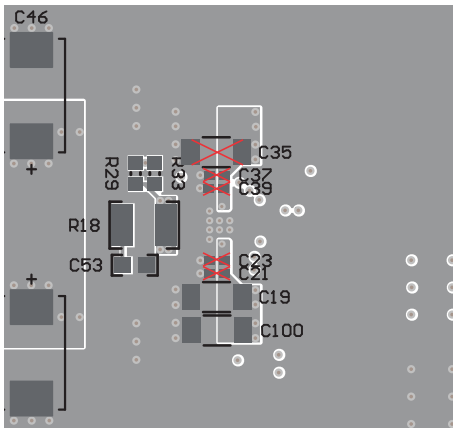

Figure 4-3. Bottom Layer Recommended Asymmetrical EVM Layout

The asymmetrical layout guides are for reference purposes if users intend to design their system based on the TPS54KB20 asymmetrical butterfly footprint. Figure 4-2 and Figure 4-3 are PCB layout images containing red marking on the capacitors recommended for removal to achieve the asymmetrical configuration.

5 Test Data

The experimental data below displays a waveform comparison between the two footprints, showing SW-node and VIN-SW signals. The data is measured at 12V Vin, 3.3V Vout, 25A load, and internal VCC.

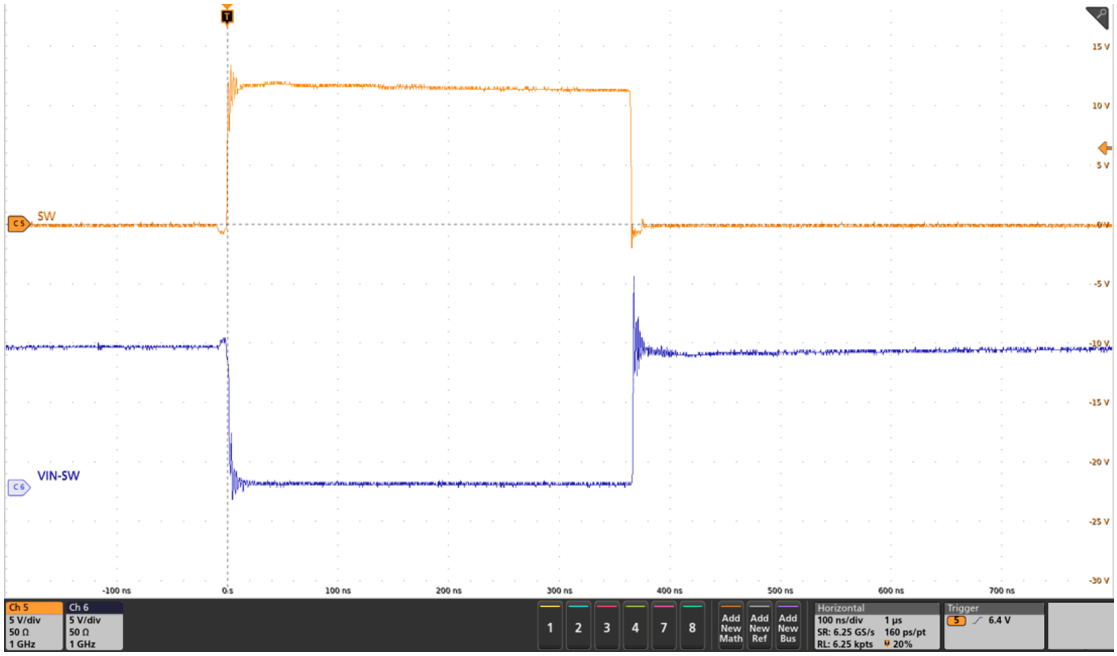

Figure 5-1. Symmetrical Footprint SW-Node and VIN-SW

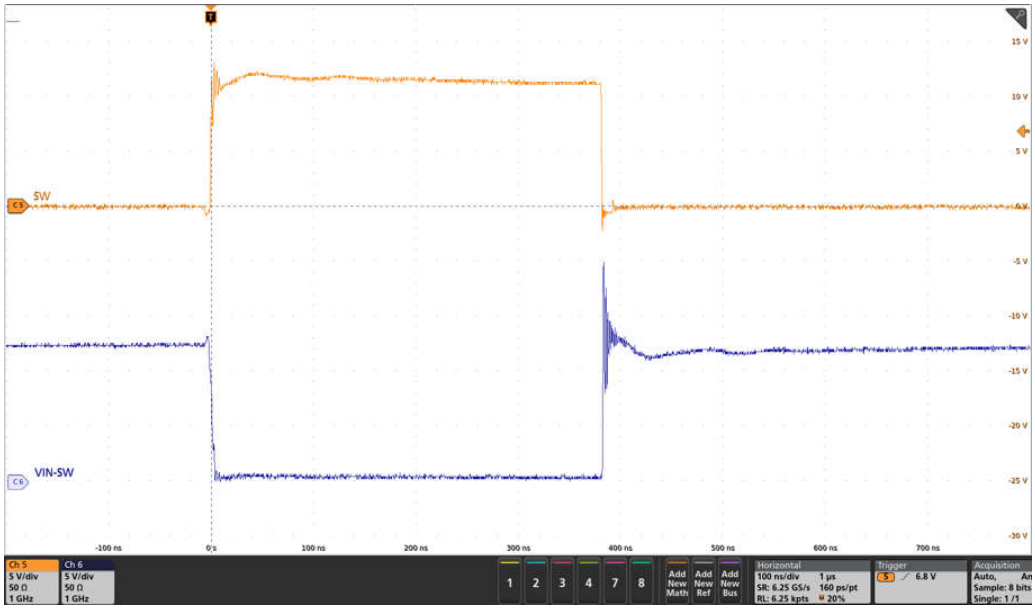

Figure 5-2. Asymmetrical Footprint SW-Node and VIN-SW

Symmetrical bench data, Figure 5-1, and Asymmetrical bench data, Figure 5-2, are compared to reflect the difference in SW-node ringing when tested under identical parameters.

Figure 5-3 compares efficiency data between the symmetrical and asymmetrical layout.

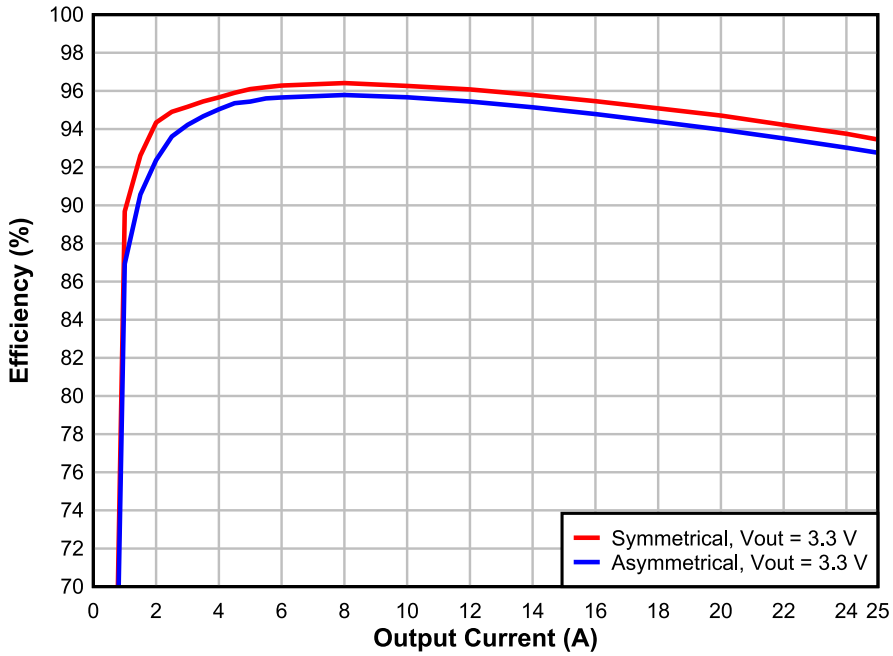

Figure 5-3. Efficiency (Vin = 12V, 800 kHz FCCM)

6 Summary

This application report provides the recommended layout methods if users are seeking to utilize symmetrical input voltage rails or asymmetrical input voltage rails with a number of removed input capacitors. This report also provides bench data supporting each design, making the two layout methods easily comparable. The symmetrical butterfly footprint guarantees the minimum amount of SW-node ringing along with the highest efficiency compared to the asymmetrical design. Although the symmetrical layout is recommended, this document provides users with an alternative if a single input rail and capacitor reduction is essential. Having this alternate selection grants users with design flexibility. The TPS54KB2x utilizes the unique butterfly-style footprint with the capability of retaining a stable SW-node while granting users the option to remove the recommended amount of capacitors from one side of the package.

Table 6-1 lists a table summary for the recommended symmetrical and asymmetrical input capacitor configurations. The table specifies the number of VIN rails and input capacitors for each configuration method.

Table 6-1. Configuration Summary Table

Layout Method	# of VIN Rails	CIN PIN 3	CIN PIN 9
Symmetrical	2	3x10µF, 1x1µf, 1x0.1µF	3x10µF, 1x1µf, 1x0.1µF
Asymmetrical	1	4x10µF, 1x1µf, 1x0.1µF	0x10µF, 0x1µf, 1x0.1µF

7 References

- Texas Instruments, *TPS54KB20 Product Folder*.
- Texas Instruments, *TPS54KB2x 4-V to 16-V Input, 25-A, Remote Sense, D-CAP4 Synchronous Buck Converter*, data sheet.
- Texas Instruments, *Time-Saving and Cost-Effective Innovations for EMI Reduction in Power Supplies*, marketing white paper.

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