Application Note

Layout Optimization of 4-Switch Buck-Boost Converters

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ABSTRACT

A layout is very important when designing a switching regulated power supply. If a layout is not carefully done, the regulator can suffer from instability and noise problems. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. This application note provides guidance on how to route the LM5177 power supply layout which can help to achieve a robust and reliable design.

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Trademarks

1 Importance of DC-DC Power Supply Layout

The PCB layout design is very important when designing a switching power supply. If the PCB layout is inappropriate, the power supply performance can be hindered, up to a damage of the converter. Often, issues with switching power supply prototypes start with the PCB layout.

Poor layout increases the parasitic inductance, capacitance and resistance within the circuit. The poor layout can increase noise pickup between different parts of the circuit, and increase thermal stresses within the regulator.

This application note provides a guideline example for our new LM5177 wide V_{in} bidirectional 4-switch buck-boost regulator. Under the guidance of this application note, the customers can achieve stable operation, and good thermal and low EMI performance. The main content includes identification of the critical switching loops, optimizing the hot loops, separating differential sense lines from power planes, AGND and PGND connection.

2 Steps for a Good Layout

2.1 Identifying Critical Circuit Paths

A good layout begins by identifying these critical components

- High di/dt loops or hot loops.
- High dv/dt nodes.
- Sensitive traces.

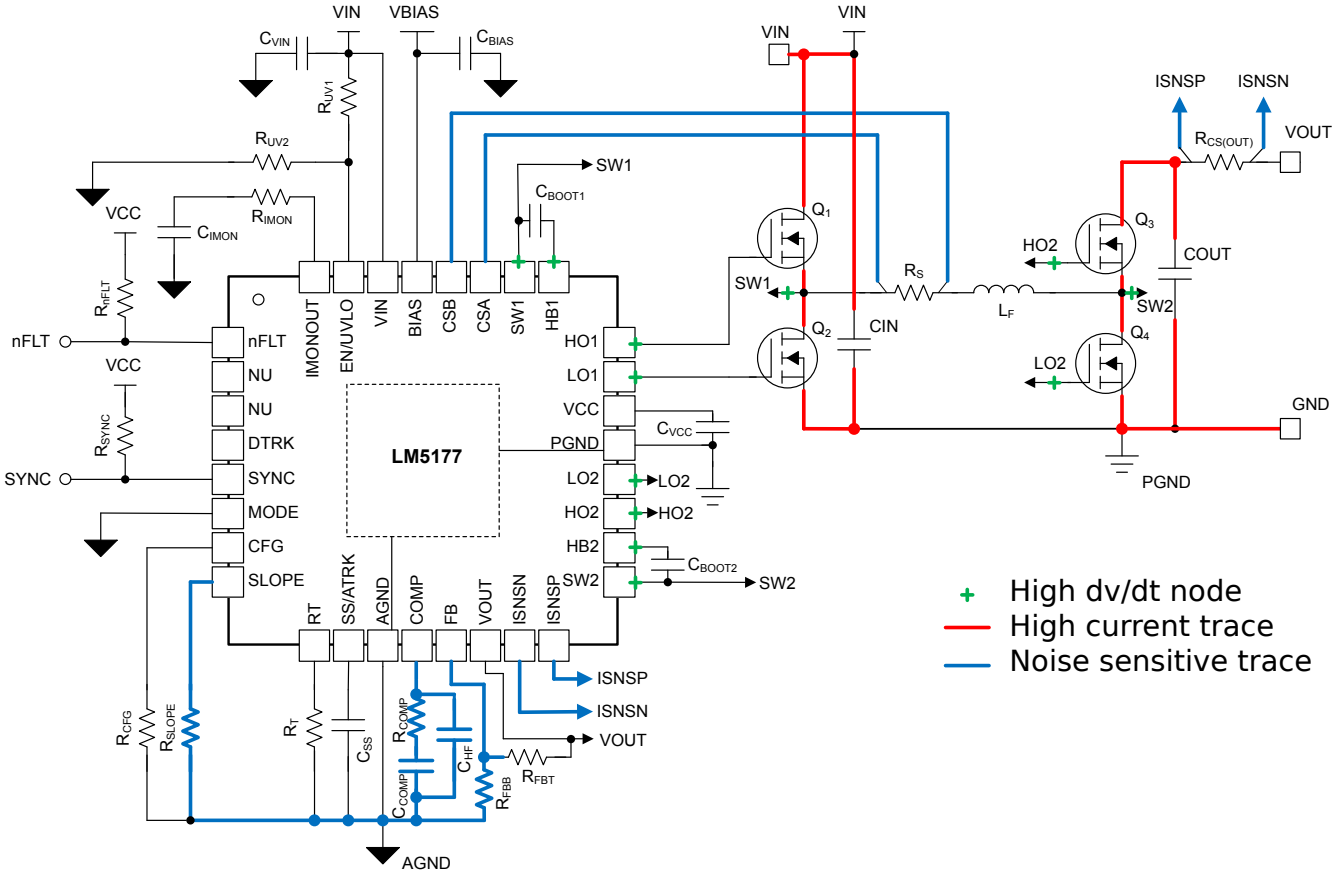

Figure 2-1. Identifying High di/dt Loops, High dv/dt Nodes and Sensitive Traces

Figure 2-1 shows the high di/dt paths in the converter controller by LM5177 . The most dominant high di/dt loops are the input-switching current loop and output-switching current loop. The input loop consists of an input capacitor (CIN), and MOSFETs (Q1 and Q2). The output loop consists of an output capacitor (COUT), and MOSFETs (Q3 and Q4), along with their return paths.

The high dv/dt nodes are those with fast voltage transitions. These nodes are the switch nodes (SW1 and SW2), the boot nodes (HB1 and HB2), and the gate-drive traces (HO1, LO1, HO2 and LO2). The areas of the switching

nodes SW1 and SW2 need to be as small as possible. If the SW1 and SW2 are poured with big area copper planes, the high dv/dt noisy signal can couple into other traces nearby through capacitive coupling, which causes electromagnetic interference issues.

The current-sense traces from resistor R_S to the integrated circuit (IC) pins (CSA and CSB), the input or output sense traces (ISNSP, ISNSN, FB), and the control components (SLOPE, R_{COMP}, C_{COMP}, C_{HF}) form the noise-sensitive traces.

For good layout performance, optimize the surface areas of high dv/dt nodes, and keep the noise-sensitive traces away from the noisy (high di/dt and high dv/dt) portions of the circuit and minimize thier loop areas.

2.2 Optimizing Hot Loops in the Power Stage

Once you have identified the critical parts of your power supply layout, your next task is to minimize any sources of noise and unwanted parasitic. The input-switching current loop and output-switching current loop are the dominant high current loops. Minimize the area of these loops to suppress generated switching noise and optimize switching performance.

The most important loop areas to minimize are the path from the input capacitors through the buck high-side and low-side MOSFETs, and back to the ground connection of the input capacitor and the path from the output capacitors through the boost high-side and low-side MOSFETs, and back to the ground connection of the output capacitor. Connect the negative terminal of the capacitor close to the source of the low-side MOSFETs (at ground). Similarly, connect the positive terminal of the capacitor or capacitors close to the drain of the high-side MOSFETs of both loops.

In addition to these recommendations, follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.

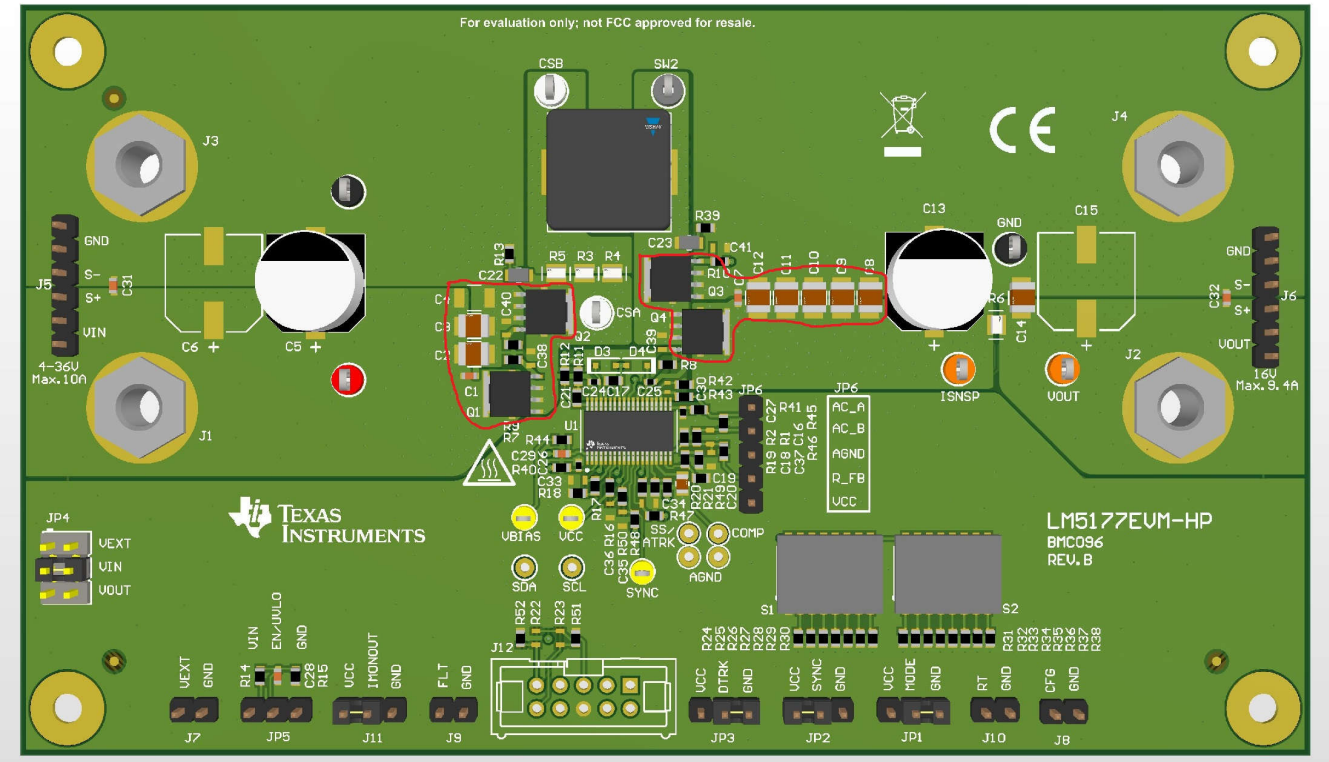

Figure 2-2. Hot Loops in a LM5177 Four Switch Buck - Boost Device

2.3 Separating Differential Sense Lines From Power Planes

The most frequently encountered issue in layout is the incorrect routing of differential sense signals from the sense resistor to TI's LM5177 integrated circuit (IC) pins (the CSA-CSB pair).

Use Kelvin connections to R_{SENSE} (R3, R4, R5) for the current sense signals CSA and CSB and run the lines in parallel from the R_{SENSE} terminals to the IC pins. Avoid crossing noisy areas such as SW1 and SW2 nodes or high-side and low-side gate drive traces. Place the filter capacitor for the current sense signal as close to the IC pins as possible.

In the case of LM5177, one of the sense nodes CSA is electrically the same as SW1. SW1 needs to use a separate routing to avoid noise getting picked up, as this is the return path of the buck high side switch.

2.3.1 Using Net Ties to Separate Routing

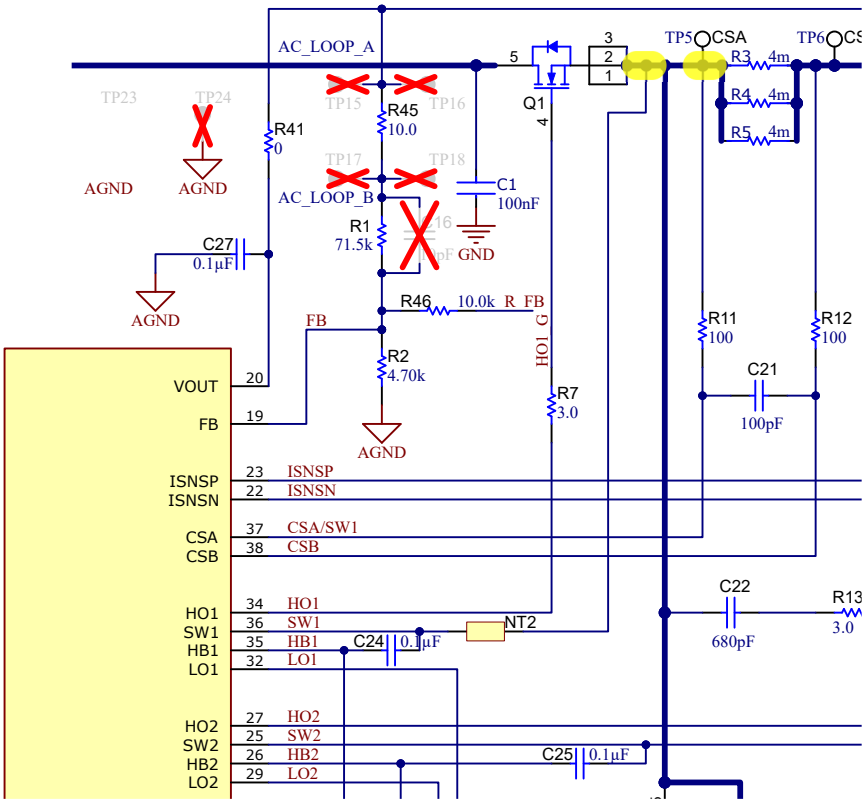

Figure 2-3. Example of Using the Net-Tie to Treat CSA and SW1 as Separate Nodes

In some cases, the designer does recognize the need of two separate nodes. But during the finishing of the board, the layout treats the CSA and SW1 as same nets. This unintended connection can happen anywhere along the trace. A net tie allows an artificial separation of net names in the schematic as shown in Figure 2-3. This allows the layout tool to treat CSA and SW1 as separate nodes and protects the differential trace (CSA) from accidental connections . The pins CSA and SW1 are marked as shown in Figure 2-3. Net ties act like a zero-ohm resistor and allow to define the connection point of the two nets on the PCB.

2.4 Routing Gate-Drive and Return Paths

The LM5177 high-side and low-side gate drivers incorporate short propagation delays, frequency depended dead-time control, and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turn-on and turn-off transitions of the external power MOSFETs.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, and thereby increasing MOSFET switching times.

The PCB trace capacitance for the gate drive is normally negligible, so it will be ignored here. Figure 2-4 shows the equivalent gate-drive circuit. R_{Trace1} is the PCB drive trace resistance, R_{Trace2} is the drive return trace resistance, L_{Trace1} is the drive trace stray inductance, L_{Trace2} is the return path inductance and C_{iss} is the MOSFET gate input capacitance. The trace resistances and inductance can cause gate signal delays; therefore, it's best to keep the drive and return traces as short as possible.

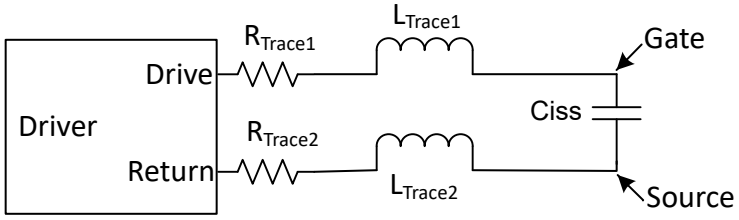

Figure 2-4. Gate – Drive Equivalent Circuit

Given board area limitations, it is often not possible to place the driver very close to the MOSFET. Even if the MOSFET is not very close, it is possible to make R_{Trace1} and R_{Trace2} <1 Ω in most designs. However, L_{Trace1} and L_{Trace2} can become significant if the trace routing is poor.An inductance of just a few nanohenries may resonate wildly with the MOSFET gate capacitance and create gate voltage ringing, as shown in Figure 2-5. If the magnitude of the ringing exceeds the MOSFET gate threshold voltage, Vth, it will cause unwanted extra switching action and result in severe switching losses inside the MOSFETs. Also, the negative peak can exceed the allowed gate signal level of the MOSFET.

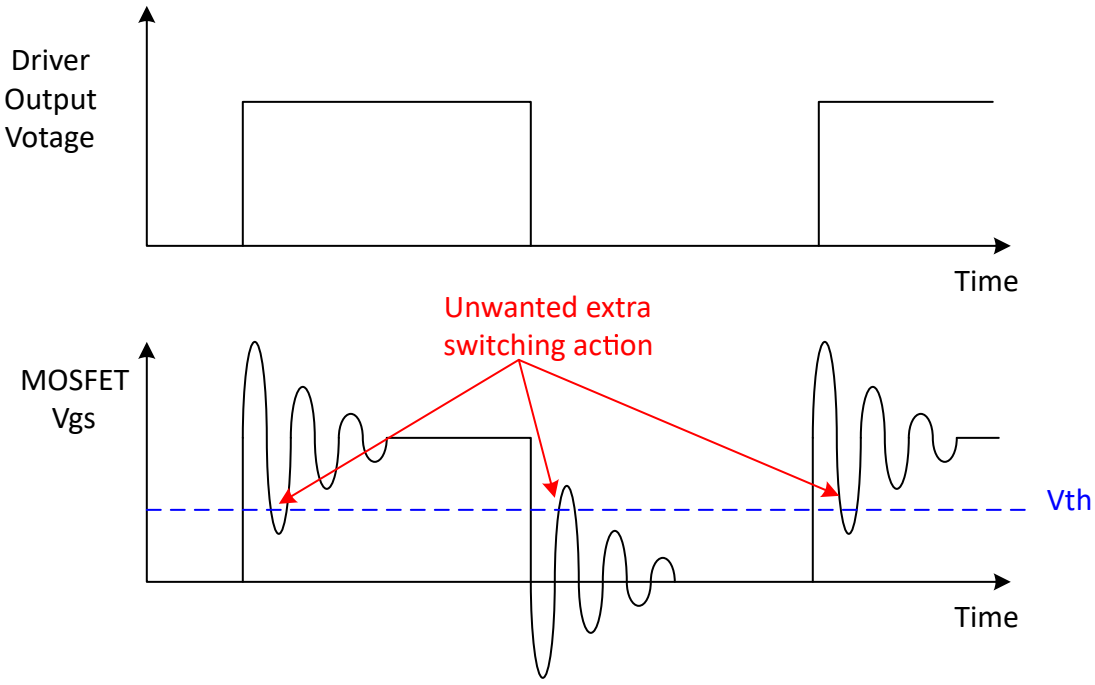

Figure 2-5. Gate Ringing and Unwanted Extra Switching Action

How can you minimize the gate-drive inductance? According to physics, the gate-drive inductance is proportional to the spatial area enclosed by the drive current loop, which is the area defined by the actual drive and return traces. Minimizing the spatial area of the drive current loop needs to be your main focus in routing the MOSFET drive and return paths.

Assume that the drive is at point A and the MOSFET is at point B on the PCB; the drive trace must be routed from point A to point B and return back to point A. Also assume that a straight trace from A to B is not possible because other components are in the way. Figure 2-6 shows two different routing patterns. Obviously, option Number 2 encloses a minimal spatial area and thus produces the least inductance, even though the total trace length is almost the same as option Number 1. This example clearly shows that the optimal routing is to place the drive and return traces closely side by side for the entire distance between the driver and the MOSFET.

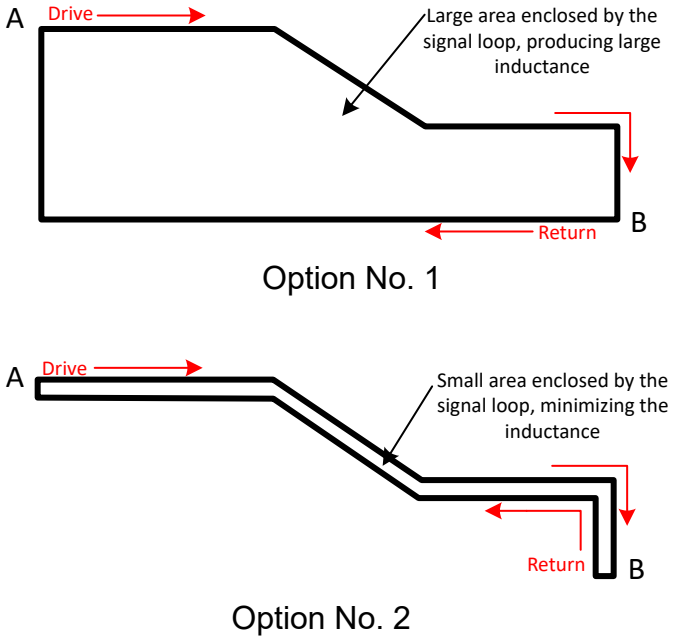

Figure 2-6. Routing patterns for current loop traces between point A and B on the PCB

Again, given board area limitations, sometimes there is no space to place the pair of drive and return traces side by side on the same layer. A design is to route the return trace in the shadow of the drive trace on the adjacent layer, as shown in Figure 2-7, where the drive trace runs from point A (Drive) on Layer 1 to point B (MOSFET), and takes the via hole to Layer 2, and runs back to point A in the shadow of the drive trace. In this way, the drive and return traces basically run closely side by side in the vertical direction, minimizing the spatial area enclosed by the signal loop.

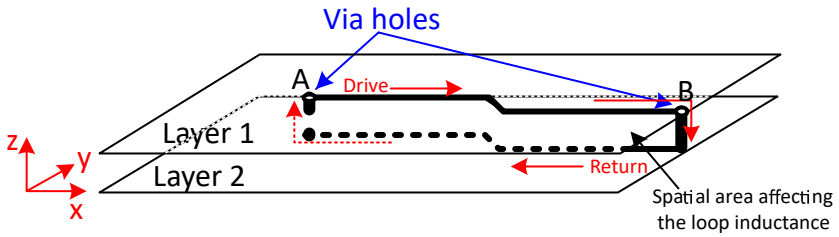

Figure 2-7. Routing the Return Trace in the Shadow of the Drive Trace on an Adjacent Layer to Minimize Loop Inductance

In LM5177, connections from the gate driver outputs, HO1 and HO2, to the respective gates of the high-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route HO1 and HO2 and SW1 and SW2 gate traces as a differential pair from the device pin to the high-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Connections from gate driver outputs, LO1 and LO2, to the respective gates of the low-side MOSFETs must be as short as possible to reduce series parasitic inductance. Route LO1 and LO2, and PGND traces as a

differential pair from the device pin to the low-side MOSFET, taking advantage of flux cancellation by reducing the loop area.

Minimize the current loop paths from the VCC, HB1, and HB2 pins through their respective capacitors as these provide the high instantaneous current.

2.5 Controller Layout

With the provision to locate the controller as close as possible to the power MOSFETs to minimize gate driver traces, the components related to the analog and feedback signals as well as current sensing are considered in the following:

- Separate power and signal traces, and use a ground plane to provide noise shielding.
- Place all sensitive analog traces and components related to COMP, FB, SLOPE, SS/ATRK, and RT away from high-voltage switching nodes such as the following to avoid mutual coupling:
  - SW1
  - SW2
  - HO1
  - HO2
  - LO1
  - LO2
  - HB1
  - HB2
- Use an internal layer or layers as ground plane or planes. Pay particular attention to shielding the feedback (FB) trace from power traces and components.
- Route the CSA and CSB and ISNSP and ISNSN traces as differential pairs to minimize noise pickup and use Kelvin connections to the applicable shunt resistor. Place the filter components of these sense signals close to the controller to minimize noise pickup after them.
- Locate the upper and lower feedback resistors close to the FB pin, keeping the FB traces as short as possible. Route the trace from the upper feedback resistor or resistors to the output voltage sense point.

2.6 Separate AGND and PGND

In power supply layout, separating the signal system is important, such as the feedback path which is susceptible to noise and the switching nodes that switch large current. The same hold good for the ground wiring too which requires special considerations.

- AGND: a quiet ground reference for control signals (analog ground)
- PGND: a noisy ground reference for power signals (power ground)

AGND is used for the ground lines that are susceptible to noise such as feedback pins and PGND is used as return path for large current signals.

Though the DC ground potential is the same, measure must be taken to separate these AGND and PGND planes to make sure noise arising from digital or high-power signals is not conducted between them to interfere with analog signals. AGND is used for control signals and should be closer to the IC and should have its own polygon. It is also important to make sure AGND and PGND are on the same potential and ultimately should be connected together at one point.

Also, it is recommended having two ground signs in your schematic already as it becomes difficult to visualize sensitive and noisy potentials on the layout if the same GND sign is used on the schematic. Hence, it is better to start with split GND in the schematic level and connect them with a net tie.

2.7 Thermal Vias

Surface mount components only dissipate heat through the PCB. The amount of heat dissipated depends on the thickness and area of the copper foil on the PCB. The thickness and the area need to follow standard specifications, as via holes also have inductance and need to be used only when necessary. For the effective usage of thermal vias, they need to be placed close to the heating element.

The HTSSOP package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally and weak electrically connected to the substrate (ground) of the device. This connection allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal system.

3 Tips for Layout Optimization

- Do the placement of the power circuit first.
  - Change part locations, and importantly the orientations, to make the high current flow along a short and straightforward path. Prevent unnecessary zigzag patterns.
  - Try to avoid using via holes on the high current path unless they are necessary. When using vias, you need to use an adequate number of via holes.
  - There is a tradeoff to make among the number of, and spacing between, the via holes. Too many via holes crowded in a small area can hinder current flow due to the loss of copper area.
- Find a location for the controller IC, not too far from the MOSFETs that it will drive. The location needs to allow a decent AGND polygon to accommodate all control signals. The AGND and PGND connection point needs to be the thermal pad. Place the critical control components next to the controller IC, and visualize the signal routes. Move the components and change their orientations to simplify the routing
- Route high current traces as well as the critical control signal paths before routing other traces.
- Optimal layout of the switch mode power supply is always the result of iterations. There is no short cut that can lead to an optimal layout in one shot.

4 Layout Example

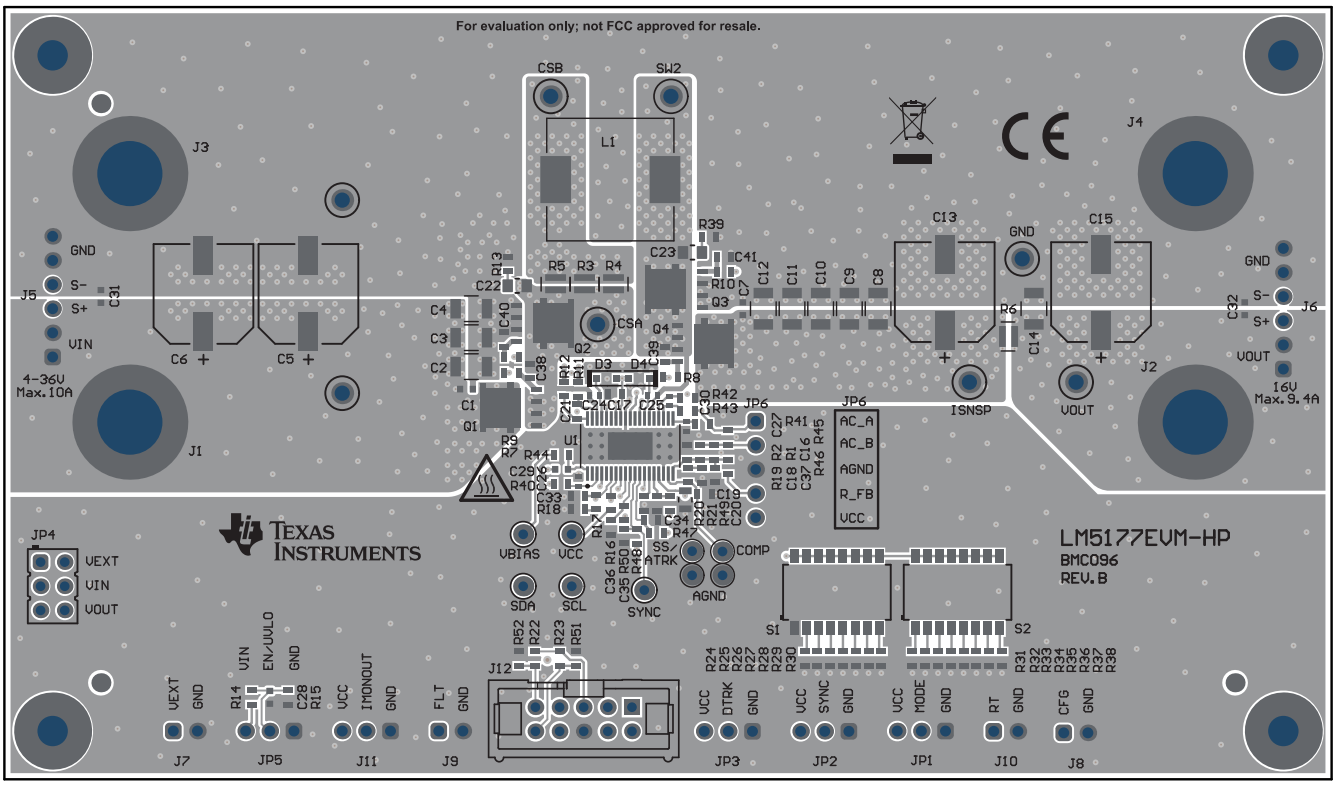

Figure 4-1. LM5177 Top Layer Routing Example

5 Summary

Printed circuit board (PCB) layout design plays a critical role in achieving high performance for a four-switch buck-boost regulator. Every layout is different, but what remains consistent is that to produce a good layout, you must understand the circuit fully and the environment or application that the board will be a part of. Carefully consider each block of components on the schematic, whether they are there for safety, EMI, feedback, thermal relief, and so on.

This application note describes the layout steps for good layout for LM5177. The document begins with the identification of the critical switching loops. By proper power component placement, keeping critical loops small, and carefully routing the sensitive traces, you can achieve a good and robust power supply layout.

6 References

1. Texas Instruments, *TPS55165-Q1 Layout Guidelines*, application note.
2. Texas Instruments, *TPS55288 Layout Guideline*, application note
3. Texas Instruments, *LM5177 80-V Wide VIN Bidirectional 4-Switch Buck-Boost Controller*, data sheet.
4. Texas Instruments, *Four-Switch-Buck-Boost-Layout-Tip-No-1-Identifying-the-Critical-Parts-for-Layout*
5. Texas Instruments, *Four-Switch-Buck-Boost-Layout-Tip-No-2-Optimizing-Hot-Loops-in-the-Power-Stage*
6. Texas Instruments, *Four-Switch-Buck-Boost-Layout-Tip-No-3-Separating-Differential-Sense-Lines-From-Power-Planes*
7. Texas Instruments, *Four-Switch-Buck-Boost-Layout-Tip-No-4-Routing-Gate-Drive-and-Return-Paths*

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