Application Note

Operating TPS6287X-Q1 Devices in a Stacked Configuration

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ABSTRACT

Non isolated inductive step-down converters designed with integrated solutions similar to TPS6287x are using only a few passive components to complete the circuit. Usually this is already a small design. In some cases, the passive components are still too large or just too high to fit in the application environment or the current rating of suitable components is not sufficient. To address this, multiple converters can be operated in parallel to supply the same load. Devices of the TPS6287x family support this type of configuration. Those devices have functions integrated which facilitate operating the devices in a stack in parallel. This application note describes in detail how such a stacked configuration compares to a single converter solution.

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Trademarks

1 Introduction

Although it sounds simple to just use converters in parallel, there are certain important details to take care of. To avoid beat frequencies causing unpredictable input and output voltage ripple and noise, the switching frequency of the converters in a stack must be synchronized. Adding a phase shift to the synchronization is also beneficial to ensure that the converters are not switching at the same time. This process minimizes the peak input current of the converter design. The process is also beneficial if the load current always is equally shared among the converters in a stack to use each converter and its directly attached passive components to their maximum capability. This way, the stack can be designed to be most area and cost efficient. The TPS6287x devices have features implemented to properly support such configurations in a way which is easy to design with. More details can be found in the *TPS6287x Data Sheet*. In this application note a single stage converter design is compared to a dual stage converter design supplying the same load. Both designs are based on converters of the TPS6287x family with different output current ratings.

2 Configurations

For the comparison in this application note, the TPS62873EVM-143 is used for the measurements at the single stage converter design and the TPS62873EVM-144 is used for the measurements at the dual converter design. Both circuits are configured to supply a 12-A load at 0.75 V. The circuits are also configured to support a fast load transient from 4.5 A to 12 A in 1 µs, allowing an output voltage deviation of less than 3.3%.

The TPS62873EVM-143 is already configured for this specification, so no modifications are needed for the measurements. The device was used with its default configuration. Figure 2-1 shows an overview of the critical components of the schematic and details of the BOM are listed in Table 2-1.

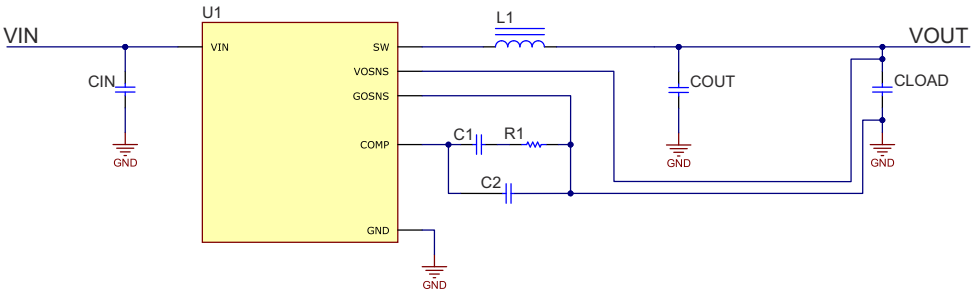

Figure 2-1. Single Converter Schematic

Table 2-1. Single Converter BOM

Ref	Qty	Value	Description	Size	Part Number
CIN	2	0.47 µF	Ceramic Capacitor, 10V, X7S	0402	GCM155C71A474KE36D
	2	2.2 µF	Ceramic Capacitor, 10V, X7S	0603	CGA3E3X7S1A225K080AB
	2	10 µF	Ceramic Capacitor, 10V, X7R	0805	GCM21BR71A106KE22
U1	1		2.7-V to 6-V Input, 12A, Fast Transient Synchronous Step-Down Converter with I2C Interface, Remote Sense and Stackability	WQFN-FCRLF16	TPS62872QWRXSRQ1
L1	1	110 nH	Inductor	4.0 × 4.0 × 2.0 mm	XGL4020-111MEC
C1	1	1800 pF	Ceramic Capacitor, 50V, X7R	0402	
R1	1	2.43 kΩ	Resistor 1%, 0.1 W	0402	
C2	1	10pF	Ceramic Capacitor, 50V, COG/NPO	0402	
COUT	2	0.47 µF	Ceramic Capacitor, 10V, X7S	0402	GCM155C71A474KE36D
	2	22 µF	Ceramic Capacitor, 10V, X7R	1206	GCM31CR71A226KE02
CLOAD	2	47 µF	Ceramic Capacitor, 6.3V, X7R	1210	GCM32ER70J476ME19L
	2	100 µF	Ceramic Capacitor, 6.3V, X5R	1210	GRT32ER60J107ME13L
	2	0.47 µF	Ceramic Capacitor, 10V, X7S	0402	GCM155C71A474KE36D

The TPS62873EVM-144 by default is configured for an output current of 30 A. For the measurements for this application note the TPS62873 devices are changed to the lower current rated TPS62870 devices of the same device family. Since the current rating of the inductor can be lower as well a smaller inductor, the VCTA32252E-R11 was used to replace the larger XGL4020-110. With this modification the required PCB area for the two inductors in the stack is about the same as the required area for the single inductor in the single converter design. The amount of capacitors in the load side capacitor bank is also reduced from the default assembly which was designed to support higher output currents to the same configuration as it is used on the TPS62873EVM-143. Figure 2-2 shows an overview of the critical components of the dual converter schematic. Details of the BOM are listed in Table 2-2.

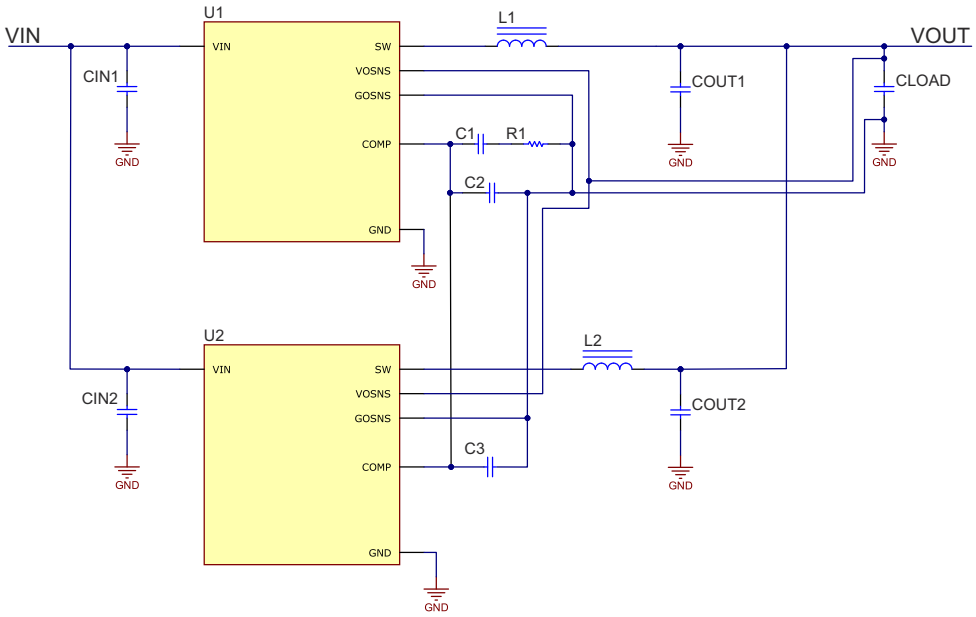

Figure 2-2. Dual Converter Schematic

Table 2-2. Dual Converter BOM

Ref	Qty	Value	Description	Size	Part Number
CIN1, CIN2	2 × 2	0.47 µF	Ceramic Capacitor, 10V, X7S	0402	GCM155C71A474KE36D
	2 × 2	2.2 µF	Ceramic Capacitor, 10V, X7S	0603	CGA3E3X7S1A225K080AB
	2 × 2	10 µF	Ceramic Capacitor, 10V, X7R	0805	GCM21BR71A106KE22
U1,U2	2 × 1		2.7-V to 6-V Input, 6 A, Fast Transient Synchronous Step-Down Converter with I2C Interface, Remote Sense and Stackability	WQFN-FCRLF16	TPS62870QWRXSRQ1
L1, L2	2 × 1	110 nH	Inductor	3.2 × 3.2 × 2.5 mm	VCTA32252E-R11
C1	1	6800 pF	Ceramic Capacitor, 50V, X7R	0402	
R1	1	820 Ω	Resistor 1%, 0.1 W	0402	
C2, C3	2	10 pF	Ceramic Capacitor, 50 V, COG/NPO	0402	
COUT1, COUT2	2 × 2	0.47 µF	Ceramic Capacitor, 10 V, X7S	0402	GCM155C71A474KE36D
	2 × 2	22 µF	Ceramic Capacitor, 10 V, X7R	1206	GCM31CR71A226KE02
CLOAD	2	47 µF	Ceramic Capacitor, 6.3V, X7R	1210	GCM32ER70J476ME19L
	2	100 µF	Ceramic Capacitor, 6.3 V, X5R	1210	GRT32ER60J107ME13L
	2	0.47 µF	Ceramic Capacitor, 10 V, X7S	0402	GCM155C71A474KE36D

More details of the test boards can be found in the EVM Users Guides for the *TPS62873EVM-143* and *TPS62873EVM-144*.

3 Measurements

3.1 Efficiency

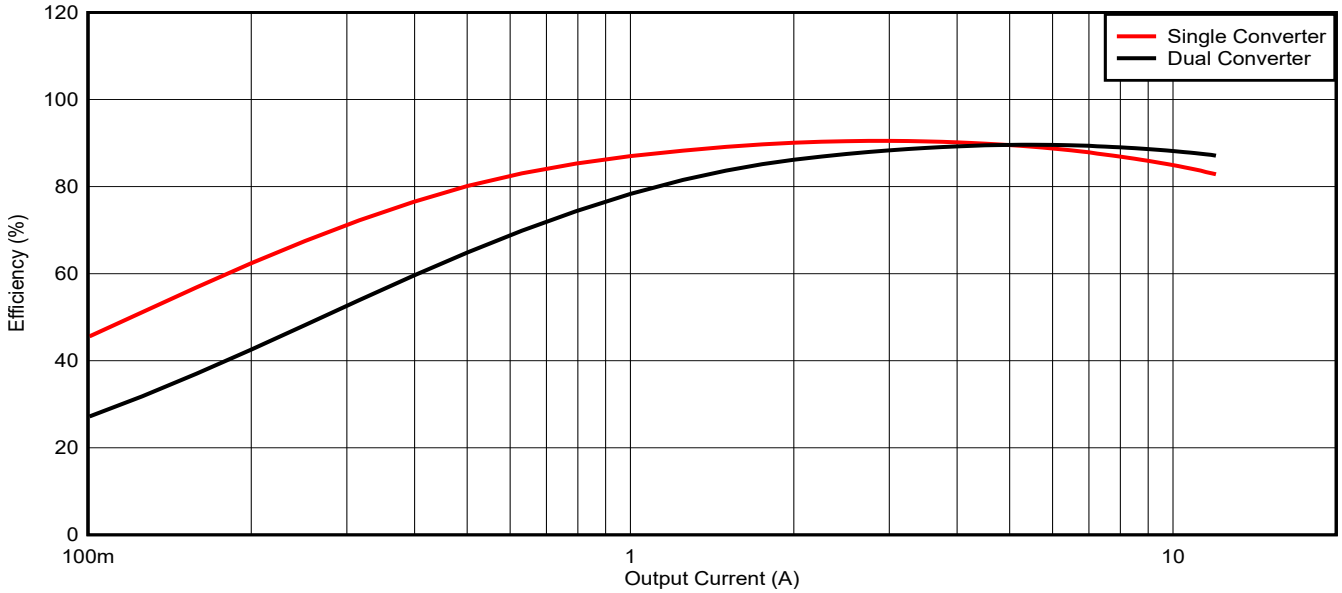

Figure 3-1. Efficiency of the Single Converter and Dual Converter

Figure 3-1 shows the result of the efficiency measurements of the single and the dual converter implementation. Since in the dual converter implementation two converters are operated in parallel, the efficiency at light load is lower. This is caused by having twice the quiescent current and increased total switching losses. At higher currents the lower RMS currents in the switches dominate the losses. For that reason the efficiency of the dual converter implementation is higher at higher output currents.

3.2 Input Voltage Ripple

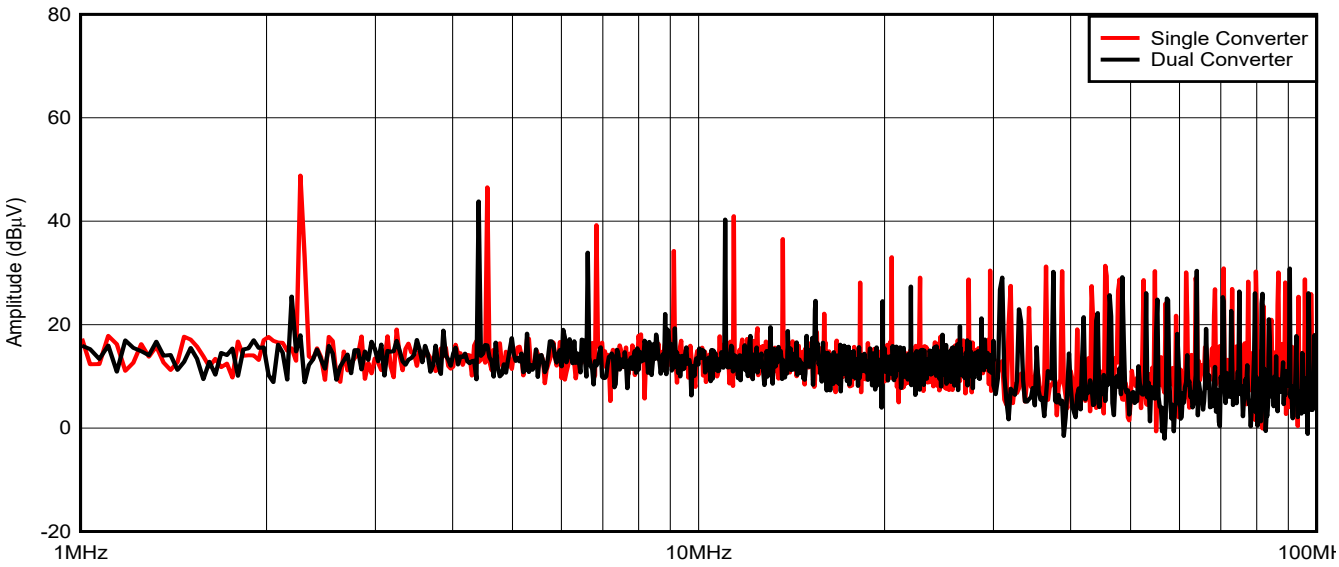

Figure 3-2. Input Voltage Ripple of the Single Converter and Dual Converter

Figure 3-2 shows the spectrum of the ripple voltage measured at the input capacitor CIN in the single converter implementation and CIN1 in the dual converter implementation. The dual converter implementation obviously shows a lower ripple at the switching frequency. This is mainly caused by the lower current in the individual converters combined with the higher total decoupling capacitance at the input of the converter, since each of the converters uses the same capacitor bank at the input.

3.3 Output Voltage Ripple

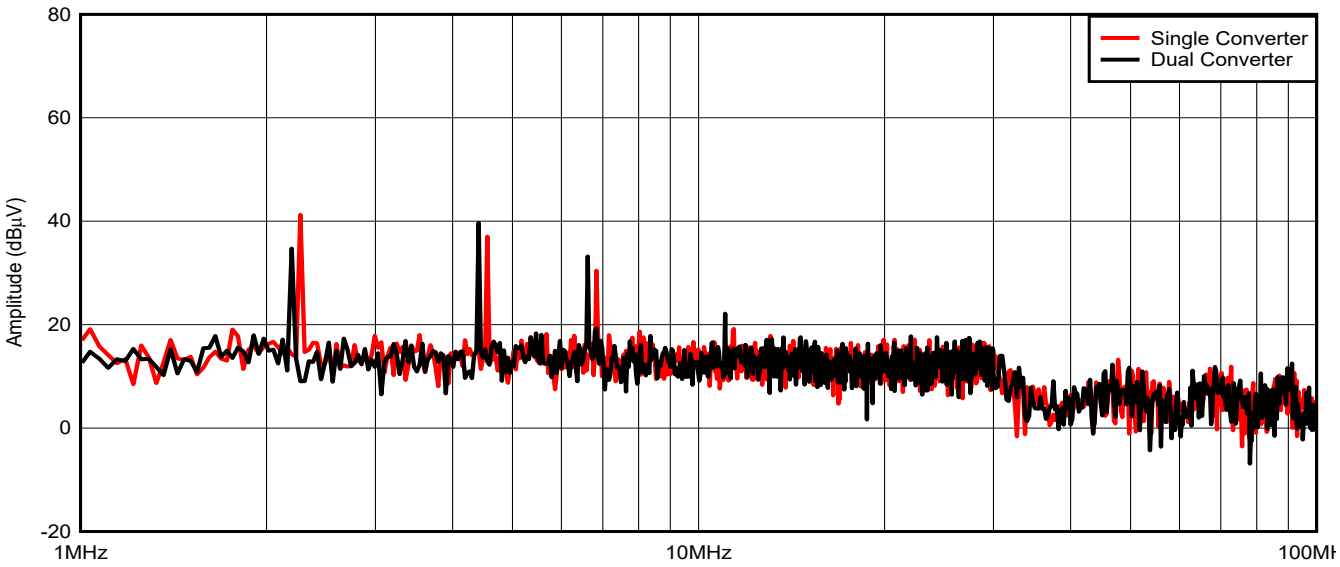

Figure 3-3. Output Voltage Ripple of the Single 5onverter and Dual Converter

The output voltage measurements shown in Figure 3-3 show no significant differences of the two converter implementations. The phase shifted synchronization of the dual converter implementation results in a minor improvement at the switching frequency. Since the capacitor bank is the same for both converters and very large in respect to filtering the switching frequency due to load transient requirements the differences in the spectrum are negligible.

3.4 Load Transient

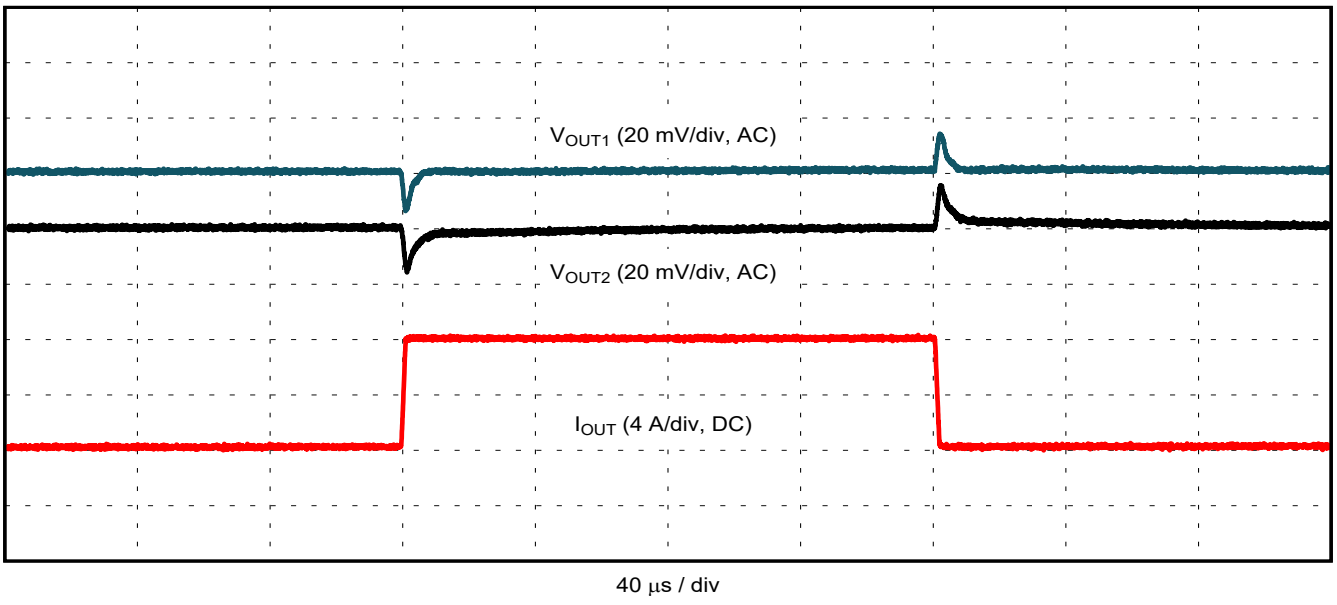

Figure 3-4. Load Transient of the Single Converter and Dual Converter

Figure 3-4 shows the load transient response to a load increase from 4.5 A to 12 A in 1 µs and a decrease back to 4.5 A with the same slope for both converter implementations. The single converter implementation (V_{OUT1}) and the dual converter implementation (V_{OUT2}) show no difference in maximum voltage deviation. The output voltage settling shows minor differences though. This is caused by the different component values required for R1 and C1 in the compensation network.

3.5 Heat Distribution

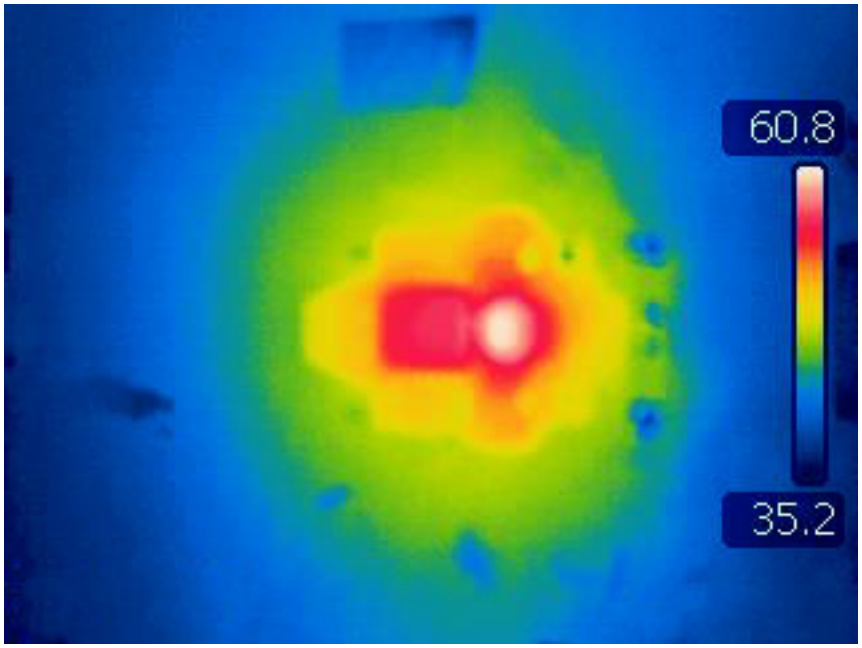

Figure 3-5. Heat Distribution of Single Converter

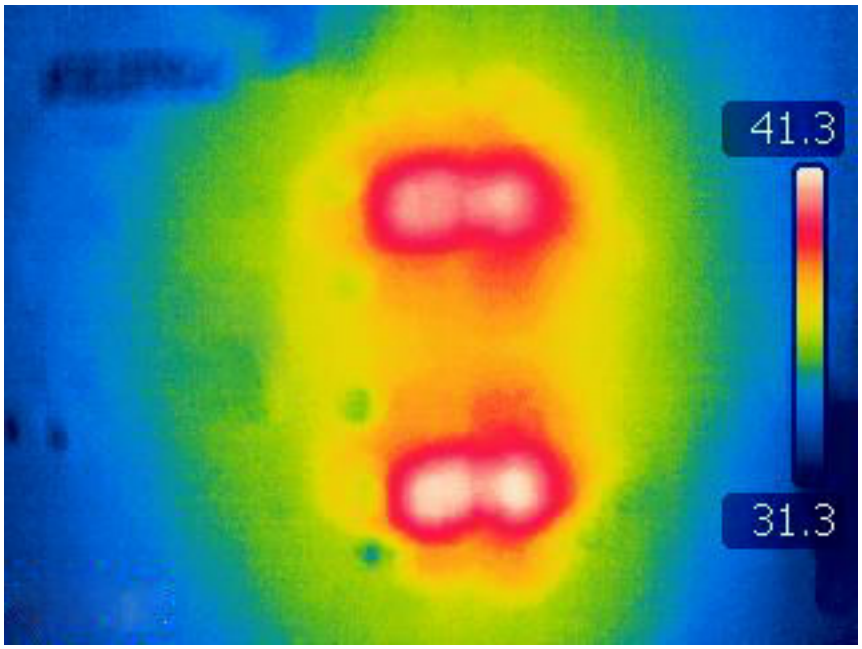

Figure 3-6. Heat Distribution of Dual Converter

Figure 3-5 and Figure 3-6 show thermal images of both converter implementations operating at 12 A output current. The higher efficiency of the dual converter implementation and the wider PCB area used to spread the heat allows the dual converter implementation to operate at almost 20°C lower temperature compared to the single converter implementation.

4 Summary

The stacked configuration uses only a few more components due to fact that two IC's are used and need to be configured properly. The output filter is basically the same. The inductor in the single converter design uses the same PCB area as both inductors in the dual configuration. The load side capacitors are the same. This results in similar efficiency and load transient performance for both designs.

But, as the measurements show, the dual converter design has lower input voltage ripple and noise. This design can be beneficial for EMI optimization and filter design. The dual converter design also shows a significant improvement in thermal performance. Using two converters allows to distribute the losses more even across the PCB in a wider area. This process can relax the challenges related to dealing with the losses in the converter and related application design.

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