Application Note

How eFuse Ensures Integrated FET Operation in Safe Operating Area

Kunal Goel
Rakesh Panguloori

ABSTRACT

Applications such as Hot-swap where Power FET is operated in saturation region under high stress, FET safe operating area (SOA) is a major concern for system designers. Designers need to study the FET SOA curve available in the manufacturers data sheet and determine if the FET can handle the power stress without undergoing damage. This application report covers the significance of FET SOA, how the manufacturers derive SOA plot, and how the hot-swaps designers make sure that external FET is operated within specified SOA. Then, the eFuse protection schemes which help to ensure SOA of the integrated FET are discussed and a detailed method of deriving AOA (Allowed Operating Area) plot from the eFuse data sheet is presented. Finally, design recommendations are shared to prevent violation of eFuse abs maximum rating, and to provide long term reliability of eFuse.

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Trademarks

1 Understanding the FET SOA

SOA defines the maximum value of V_{DS}, I_{DS}, and time envelope of operation which the device can be expected to operate without getting damaged.

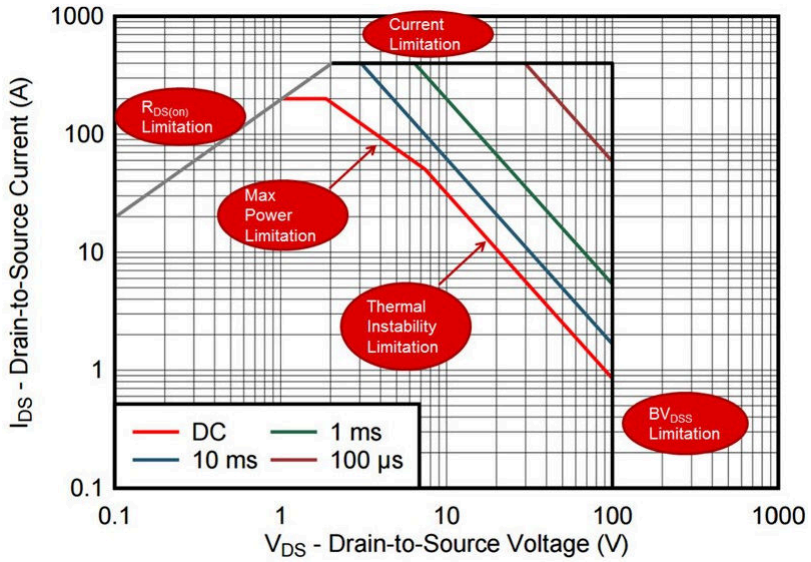

Figure 1-1. Data Sheet SOA of the CSD19536KTT

The entire SOA is made up of five distinct limitations, each of which shape the overall curve, as shown in Figure 1-1, the SOA for TI's 100 V D2PAK CSD19536KTT.

Four of these limitations can be easily calculated from the known FET parameters – the $R_{DS(ON)}$ limit, the current limit, the maximum power limit, and the B_{VDSS} limit.

- $R_{DS(ON)}$ limit is the maximum $R_{DS(ON)}$ of FET at maximum operating junction temperature.
- Current limit is constrained because of maximum rated junction temperature, package capability and other factors. This region can also be called electrical SOA.
- For power limit calculation, the temperature rise for a given pulse duration is calculated using transient thermal impedance plot in the FET data sheet. Power profile which gives temperature rise close to the maximum junction temperature decides the boundary of the SOA curve. Power limit region can also be referred as thermal SOA.
- B_{VDSS} limit is the FET breakdown voltage, defined by FET technology and comes under electrical SOA.

The fifth and the most critical region is the thermal instability region, which cannot be determined with formulas, but must be tested. This portion of the SOA, noted by where the curve deviates from the constant power line that necessarily has a slope of -1 on a current vs. voltage log-log scale, indicates where thermal runaway can occur. The steeper the slope, the more prone the FET is to enter into thermal runaway condition at higher operating voltages. This region can also be called electro-thermal SOA as explained in Section 3. To plot thermal instability region there are two methods:

1. The most accurate method is the measurement method which is followed at TI. Computer-aided test system is used for the measurement. The FET is stressed with a known current and VDS pulse of certain time duration. If the FET survives this pulse then the drain to source current is increased. This process is repeated till the FET fails.
2. Another method is power limit calculation where the boundary is calculated based on safe junction temperature rise. This method is not an accurate method and does not present true picture of thermal instability region.

After having looked in detail about FET SOA , here are some FET failure modes that can occur on violating SOA.

1. B_{VDSS} violation - Causes reverse-biased body-drift diode break down and large amount of current starts to flow between the source and drain due to the avalanche multiplication process.

2. Power limit violation - On operating FET for higher power than the SOA boundary for a given time causes die junction temperature to cross the safe threshold and FET will damage due to excessive heat.
3. Current limit violation - Current limit is a function of maximum junction temperature, internal materials and connection between silicon and plastic package. Violating this can cause failure mechanisms such as excessive heating up of die, wire infusion, thermal degradation of molding compound, and electromigration.

Overall, it can be shown that the violation of maximum junction temperature specification of FET causes the FET to fail. Ensuring FET junction temperature is always at a safe level, also helps in ensuring that FET operates in SOA.

2 Ensuring FET SOA in Hot-Swap Design

Since mechanism to limit external FET junction temperature is not present in traditional hot-swap design, external FET SOA operation is made sure by system designer. First, external FET, power limit, and fault timer are selected. The next task for the designer is to verify FET SOA by calculations and do necessary iterations on the power limit and fault timer values. Once the power limit and fault timer are chosen, critical requirement to check is that the FET will stay within its SOA during all the stressful conditions. Please refer to Section 3.1 in the *Robust Hot Swap Design* application note for step-by-step design procedure and FET SOA verification in a traditional hot-swap design.

For example, during a *Hot-Short* the circuit breaker trips and the LM5066I re-start into power limit until the timer runs out. In the worst case, the MOSFET's VDS equal (VINMAX), IDS equal (PLIM / VINMAX) and the stress event lasts for set fault time. The SOA for chosen fault timer duration can be extrapolated by approximating SOA vs time as a power function as shown in *Robust Hot Swap Design* application note. Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be much higher during a hot-short. The SOA has to be de-rated based on case temperature.

The following section describes how eFuse manages SOA of its integrated FET through robust protection mechanisms.

3 eFuse Ensuring Integrated FET SOA Operation

To achieve robust, high power density and lower cost power path protection design, system designers are using eFuse. eFuse provides the same functionality as hot-swap controllers but it also integrates power FET, and thus eliminates lot of complexities compared to the designs using external FETs. eFuse is designed using protection schemes like thermal shutdown, current limit, fast-trip that ensures integrated FET SOA operation under stress conditions. In external FET design, integrated thermal shutdown feature is not available because of which system designer needs to manage FET SOA.

SOA of an eFuse can be interpreted similar to external FET SOA. eFuse SOA can be divided into regions and region boundary is decided by parameters like $R_{DS(ON)}$ and protection schemes of eFuse. The following show which protection scheme takes care of which region of SOA.

- **Electrical SOA** – It is the region of SOA which is limited by maximum current supported for different pulse durations. Current limit and short circuit protection features ensure that eFuse does not operate beyond this boundary.
- **Thermal SOA** – This region is the same as power limit region of FET SOA. eFuse thermal shutdown protection feature decides boundary of this region.eFuse supports certain pulse power before thermal shutdown would turn it off.
- **Electro-thermal SOA** – Industry is shifting towards high-power density designs that offer high current with very low $R_{DS(ON)}$ and area. FETs offering such specifications have reduced available SOA at higher V_{DS} known as spirito effect. Mismatch in current among multiple parallel cells increases power dissipation in those cells which further increases mismatch in current and forms a positive feedback loop between electrical and thermal parameter resulting in formation of hot-spots on FET die. Thermal instability region of FET SOA depicts this effect.

Our high power density eFuses such as TPS25947, TPS2597, TPS25981, and TPS25985 have a proprietary protection mechanism. This mechanism anticipates that integrated FET may go into thermal runaway condition and turn off the FET early thus ensuring the FET operation in SOA. When eFuse turns-on under output short circuit condition, the integrated FET experiences the most VDS stress and the chances of thermal runaway are the highest. Therefore, Texas Instrument eFuses are subjected to such tests repetitively during the qualification process. This qualification process ensures robustness of TI eFuse and proves the working of the integrated protection mechanisms.

SOA of eFuse can be termed as AOA (allowed operating area) as the safe region of operation is decided by protection schemes and eFuse is not allowed to operate beyond that AOA.

3.1 Thermal Shutdown

Discrete protection realizations need careful selection of pass FET and thermal design to keep the device in SOA limits under all fault conditions. However, TI eFuses come with inbuilt over temperature protection and shuts down if the eFuse junction temperature, T_J , exceeds 154°C (typ). A thermal shutdown circuit typically detects that a power IC is overheating, by measuring the absolute junction temperature of the hottest areas on the chip. Thermal monitors are usually positioned in the power transistor area where most of the power dissipates. A thermal monitoring circuit translates the junction temperature to a voltage or current level that is then compared to a reference level (the absolute threshold, or TABS) corresponding to a temperature below the safe limit for the IC. If the junction temperature is above TABS, then the eFuse shuts down. For more detail on thermal shutdown scheme, please refer to chapter 7 of this *11 Ways to Protect Your Power Path* white paper.

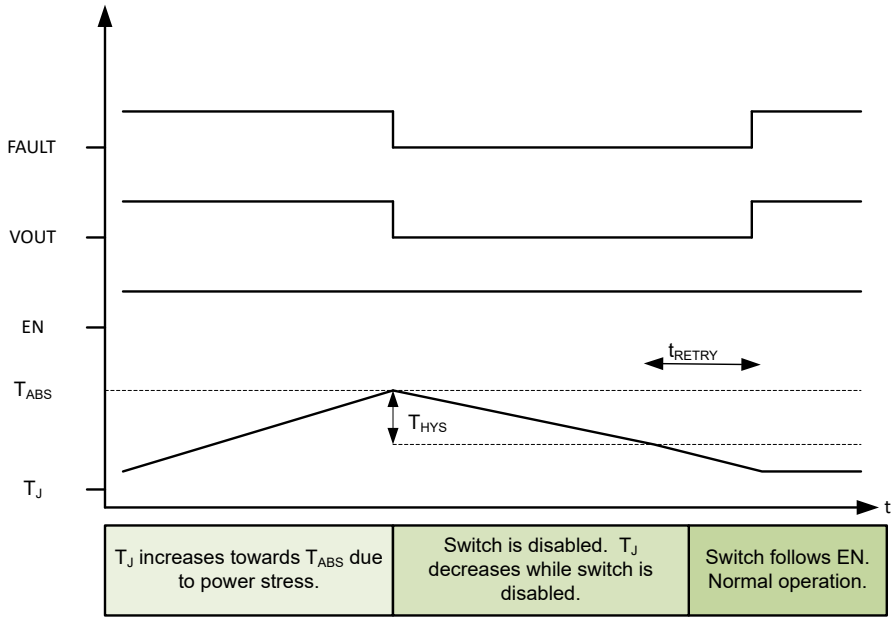

Figure 3-1. Thermal Shutdown Scheme

3.2 eFuse Response to Events Stressing Integrated FET

Table 3-1. eFuse Response to Stress Events

Stress event	Sequence of events	Probable SOA region to violate	Protection Scheme	Test Waveforms For TPS2597
Startup	High voltage drop and inrush current ->high power dissipation->FET junction temperature rises and reaches TSD threshold -> TSD scheme turns off eFuse	Thermal and electro-thermal SOA	Thermal shutdown and proprietary protection	Figure 3-2
Power up into short circuit	Enable eFuse-> starts into current limit-> very high power dissipation due to high V_{DS}-> additional proprietary layer of thermal protection ensures that FET will not enter into thermal instability region by turning off FET prior.	Electrothermal, thermal and electrical SOA	Proprietary protection, thermal shutdown and current limit	Figure 3-3 As as shown in Figure 3-3 that since Vds stress is high as compared to Figure 3-4 for same current limit setting of 8 A, time for eFuse to shutdown is lower here.
Overload during steady state	eFuse limits the current first->the output voltage drops ->increased power dissipation in the integrated FET ->rise in junction temperature->Thermal shutdown scheme takes care of FET SOA here by turning off FET when temperature reaches TSD threshold.	Electrical and thermal SOA	Current limit and thermal shutdown	Figure 3-4
Hard short circuit during steady state	eFuse performs a fast-trip within 1 us thus not letting high current build inside FET and letting the eFuse operate in SOA.	Electrical and thermal SOA	Fast-trip	Figure 3-5

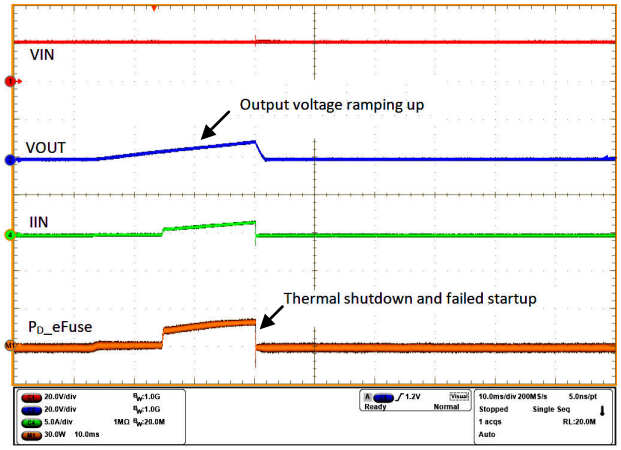

Figure 3-2. Failed Startup

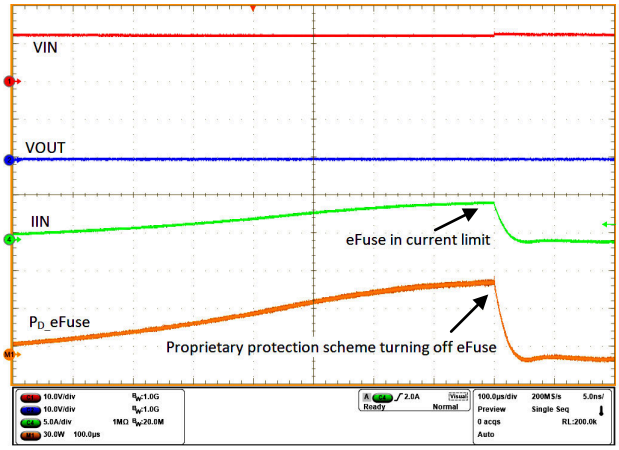

Figure 3-3. Power up into Short-circuit

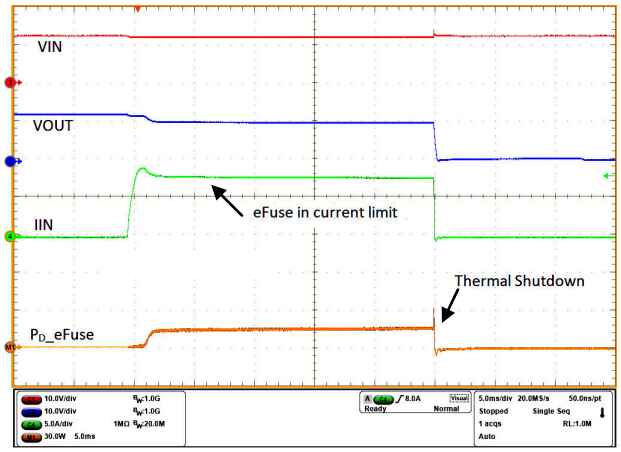

Figure 3-4. Current Limiting

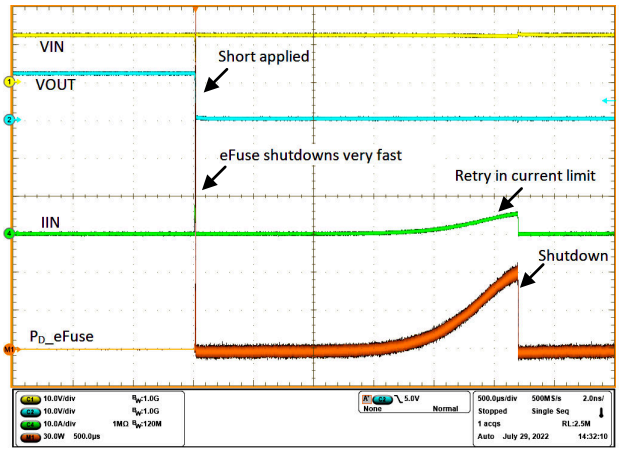

Figure 3-5. Output Short-Circuit During Steady State

4 Plotting eFuse AOA

Graphical representation of eFuse Allowed Operating Area (AOA) similarly like FET SOA can be obtained as discussed below. For example of TPS2597 eFuse and see how the boundary imposed by these protection schemes, eFuse $R_{DS(ON)}$ and maximum recommended VIN rating can be plotted on a log-log graph at 25°C ambient temperature.

1. $R_{DS(ON)}$ limited region is a line with slope equal to maximum RON of TPS2597 at 25°C which is 18.3 mΩ.
2. B_{VDSS} limited region is a line parallel to Y axis that intersects X-axis at maximum recommended VIN of 23 V.
3. Current limit region for DC power is a line parallel to X-axis with height equal to maximum dc continuous current spec of eFuse which is 7 A. In TPS2597 because of ITIMER feature we can allow current greater than 7.7A and less than 2×7.7=15.4 A for ITIMER duration. For power pulses of duration less than equal to 10 ms a zero slope line of height 14 A represents current limit line. 14A is double the minimum current limit value of 7 A (value in the electrical characteristics table of the data sheet) for 8 A current limit setting.
4. Power limit region:
   a. To plot this region for lower VDS range, steady state time to thermal shutdown vs. power dissipation plot at 25°C in the data sheet can be used. This plot tells that for a certain power how much time will it take for eFuse to thermal shutdown. This curve can also be interpreted as for a pulse of certain time duration how much maximum power can be supported before eFuse hits thermal shutdown. Also this data is provided at different ambient temperatures, so to plot AOA at different temperature this data can be used directly unlike in external FET design where derating has to be done on FET SOA at 25°C to obtain SOA at other temperatures.
   b. Suppose power limit for 10 ms pulse is to be plotted. Power value that causes TSD in 10 ms can be obtained from TSD curve. Then a line can be plotted on AOA curve such that product of V_{DS} and I_{DS} is equal to that power value.
   c. Similar procedure can be repeated for pulses of other duration.
   d. For higher VDS range inrush Time to TSD vs PD curve present in data sheet needs to be used. Boundary of AOA obtained from this curve is imposed by proprietary protection mechanism that is not letting integrated FET to thermal runaway.

Figure 4-1 plot is obtained for TPS2597.

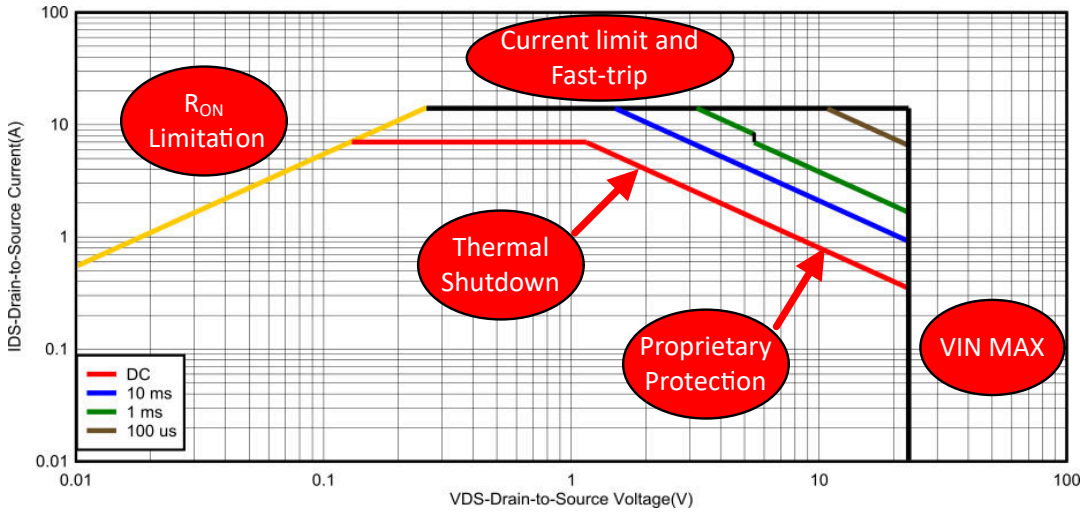

Figure 4-1. TPS2597 AOA

5 eFuse Application Design Recommendations to Ensure Integrated FET Reliability

System designer can consider below recommendations to make sure that unknowingly FET SOA is not violated and FET reliability does not worsen adversely over time.

1. B_{VDSS} limitation – as shown from the FET SOA curve that there is a limit on voltage which can be applied to FET. Similarly in eFuse data sheet recommended maximum and absolute maximum VIN is mentioned. EFuse can easily operate continuously up to recommended maximum without any long term reliability issues. But transients on VIN pin beyond absolute maximum rating can violate FET SOA and cause electrical overstress damage. To mitigate, it is recommended to use TVS diode close to the eFuse VIN pin. Please refer to this blog for more details. Also, it is recommended to use Schottky diode at output to clamp negative transients below absolute minimum rating of VOUT pin and example part number can be found in eFuse EVM schematic.
2. During steady state operation junction temperature of integrated FET can be calculated as:

$$T_J = T_A + \left(P_{diss} \times R_{\theta JA}\right) \quad (1)$$

$$P_{diss} = I_{LOAD}2 \times R_{ON} \quad (2)$$

   Board layout has to be optimized to achieve lower $R_{\theta JA}$ so that during steady state for maximum current the junction temperature is below the absolute maximum junction temperature specification in the data sheet which is typically 125°C. Operating eFuse for long time between 125°C and TSD threshold can cause long term reliability issue to eFuse. Please follow the EVM layout for reference.
3. Persistent fault with auto retry variant- The auto-retry function helps to improve the system uptime without the need of manual intervention, but there is a concern in a scenario where the fault is real and persistent. Indefinite auto-retries will not cause immediate failure of eFuse but average eFuse junction temperature increases and can be close to the maximum recommended junction temperature thus raising concern on the long-term reliability under persistent fault as depicted in *Reducing Power Loss and Overheating During Faults with eFuses* application note. To assess reliability of eFuse in system FIT rate available on ti.com can be used. Using mission profile of eFuse, which is percentage of lifetime spent at different temperatures in application, final FIT can be calculated as shown in *Calculating FIT for a Mission Profile* application note.

6 Summary

Designs using eFuse do not need to worry about integrated FET SOA unlike in traditional hot swap design. AOA plot of eFuse serves as a visual representation of eFuse protection mechanisms, $R_{DS(ON)}$ and recommended maximum input voltage. AOA or SOA plot for eFuse is not necessarily needed as the robust protection schemes of eFuse take care of integrated FET SOA.

7 References

1. Texas Instruments, *Understanding MOSFET data sheets, Part 2 - Safe operating area (SOA) graph*, E2E™ Forum
2. Texas Instruments, *Robust Hot Swap Design*, application note
3. G. Breglio, F. Frisina, A. Magri, and P. Spirito, *Electro-Thermal Instability in Low Voltage Power MOS: Experimental Characterization*, IEEE Proceedings ISPSD 1999, Toronto, p233
4. Texas Instruments, *11 Ways to Protect Your Power Path*
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6. Texas Instruments, *Selecting TVS diodes in hot-swap and ORing applications*, E2E™ Forum
7. Texas Instruments, *Reducing Power Loss and Overheating During Faults with eFuses*, application note
8. Texas Instruments, *Calculating FIT for a Mission Profile*, application note

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