Application Note

Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part I: Filter Design for Output Ripple Reduction

Andrew Xiong, Miranda Gu

ABSTRACT

In power design for applications such as ADC, RF transceiver and analog front end (AFE), output voltage ripple is an important factor for power quality evaluation. In previous DC-DC power supply, two-stage power design, including buck converter and LDO, are normally used to support low output voltage ripple requirement. In recent years, a type of power design using buck converter and secondary stage passive filter attracts more attention. Compared with conventional design with LDO, reduced design size and total efficiency improvement can be achieved. But a pair of conjugate poles can be introduced by the added passive filter, which threatens the loop stability.

In buck regulators portfolio of TI, low ripple and low noise power designs TPS6291x and TPSM8291x (3V-17V input) with unique integrated compensation can cover 12V input rail. To fill the gap of one-stage low ripple power design with higher input voltage, the design method of second stage filter for a general purpose peak current mode buck converter is introduced in this application note series. TPS62933F with 3.8V to 30V input and 3A max current is used as the example to illustrate the design method.

Table of Contents

List of Figures

Trademarks

1 Introduction

For the power of signal processing system design utilizing ADCs, PLLs and RF transceivers, low output voltage ripple is an important factor for power quality evaluation. In some power design designed to achieve low output voltage ripple, normally a buck converter is used for voltage step down as first stage and an LDO is used to filter ripple as second stage. However, the BOM cost, design size and conversion efficiency can cause concern in some compact or cost-effective application.

In recent years, a new low ripple power design attracts more attention by using a secondary stage passive LC filter combined with buck converter. Compared with conventional design with LDO, reduced design size and efficiency improvement can be achieved. See Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter application note. But a pair of conjugate poles can be introduced by the added passive filter, which threatens the loop stability. To overcome the challenge, some buck converters are designed with unique internal compensation to support second stage LC filter, such as TPS62912/3 and TPSM82912/3 known as low noise and low ripple power design. See TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation data sheet.

Low ripple and low noise normally indicate two different features of power supply. Ripple refers to the output voltage variation with switching frequency, which is measured by scope and reduced by using second stage LC filter. Noise normally refers to the voltage variation in frequency range of 100Hz-100kHz, which is usually measured with noise spectrum and limited by unique IC design.

For some application which only requires low ripple but not low noise, a second stage LC filter design method is proposed in this application note for general purpose peak current mode buck regulators, which can reduce output voltage ripple amplitude effectively with ensured loop stability. In Part I, the second stage filter components selection method to achieve required output voltage ripple is introduced. In Part II, the stability analysis and design methods are introduced. The proposed method is validated by experiments with internally compensated peak current mode converter TPS62933F. See TPS6293x 3.8-V to 30-V, 2-A, 3-A Synchronous Buck Converters in a SOT583 Package data sheet.

2 Components Selection for Secondary Stage Filter

Figure 2-1 shows the scheme of buck converter with second stage filter. A second-order low pass filter is formed by inductor L_2 and capacitor C_2. A new pair of conjugate poles is introduced with the filter, which can reduce the output voltage ripple and noise at switching frequency through the high frequency gain attenuation. The selection method of inductor L_2 and capacitor C_2 is analyzed in this section.

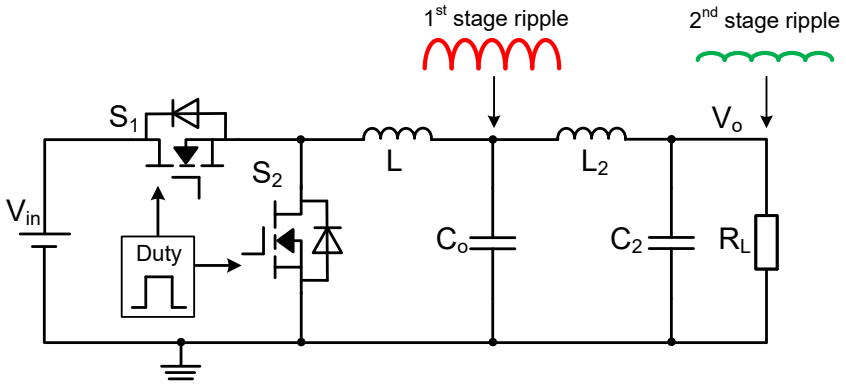

Figure 2-1. Buck Converter with Second Stage Filter

In several previous studies, the expression of output voltage ripple after the 1st stage LC filter is already derived, as shown in Equation 1. Also see the Output Ripple Voltage for Buck Switching Regulator application note.

$$V_{o1\text{-}ripple}=\frac{V_o\left(1-\frac{V_o}{V_{in}}\right)}{f_{sw}L}\left(r_c+\frac{1}{8f_{sw}C_o}\right) \quad (1)$$

where, $V_{o1\text{-}ripple}$ is the peak to peak amplitude of output voltage ripple after 1st stage. V_o is output voltage and V_{in} is input voltage of buck converter. f_{sw} is switching frequency. L and C_o are the inductance and capacitance of the 1st stage filter respectively. r_c is the ESR of capacitor C_o.

The transfer function of second stage filter is shown as Equation 2.

$$G_{vv\text{-}2nd}(s)=\frac{R_L}{s^2R_LL_2C_2+sL_2+R_L} \tag{2}$$

where R_L is output load resistance. Since MLCC is normally used as capacitor C_2 to reduce output ripple for second stage, the ESR of C_2 is ignored.

A pair of conjugate poles is included in transfer function Equation 2. The poles frequency can be approximately expressed as Equation 3. The loop gain amplitude plot is shown as Figure 2-2.

$$f_2\approx\frac{1}{2\pi}\sqrt{\frac{1}{L_2C_2}} \tag{3}$$

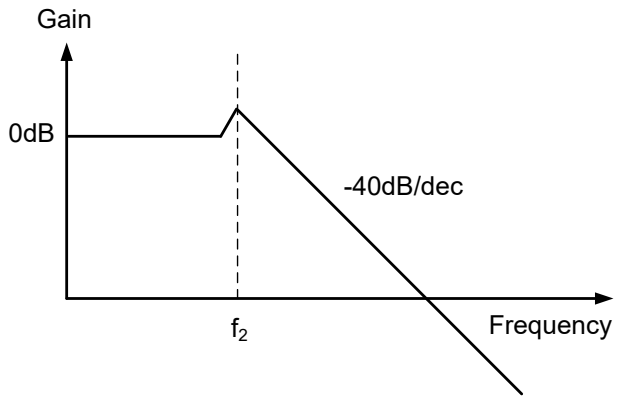

Figure 2-2. Loop Gain Magnitude Plot of Equation (2)

To simplify the relation, the effects of conjugate poles quality factor are ignored and the gain is seen as attenuation with -40dB/dec slope after frequency f_2. The relation as Equation 4 can be derived then.

$$\frac{0dB-20\lg(A_{sw})}{\lg(f_2)-\lg(f_{sw})}=-40dB/dec \tag{4}$$

where, A_{sw} is the gain amplitude at switching frequency f_{sw}.

The expression of A_{sw} can be derived with Equation 5.

$$A_{sw}=\frac{f_2^2}{f_{sw}^2}=\frac{1}{4\pi^2f_{sw}^2L_2C_2} \tag{5}$$

Applying the attenuation gain A_{sw} on $V_{o\text{-}1ripple}$, second stage ripple $V_{o2\text{-}ripple}$ is expressed as Equation 6.

$$V_{o2\text{-}ripple}=A_{sw}V_{o1\text{-}ripple}=\frac{V_o\left(1-\frac{V_o}{V_{in}}\right)\left(r_c+\frac{1}{8f_{sw}C_o}\right)}{4\pi^2f_{sw}^3LL_2C_2} \tag{6}$$

To meet the requirement $V_{o2\text{-}ripple}\leq V_{o2\text{-}ripple\text{-}target}$, the limitation for the selection of L_2 and C_2 can be received with Equation 7.

$$L_2C_2\geq\frac{V_o\left(1-\frac{V_o}{V_{in}}\right)\left(r_c+\frac{1}{8f_{sw}C_o}\right)}{4\pi^2f_{sw}^3LV_{o2\text{-}ripple\text{-}target}} \tag{7}$$

As shown, only the limitation for (L_2 x C_2) is given in Equation 7, while no limitation is given for L_2 and C_2 respectively. The inductance and capacitance can be determined with the consideration of BOM cost, DCR loss, and so on.

In Part II of this application note series, the impacts of added passive filter on loop stability can be further analyzed and the components selection range with stability restriction can be further derived then. The completed components selection range and application design method is received by considering both output voltage ripple restriction in this paper and stability restriction in next papers.

3 Experimental Validation

The experimental validation is completed with PCM converter TPS62933F. Operating condition is: V_{in}=24V, V_{out}=1.2V, f_{sw}=500kHz, I_{out}=0A. Required output voltage ripple amplitude is smaller than 800uV pk-pk.

As comparison, an application case without second stage filter is given at first. With typical recommended components value in data sheet, L=2.2 uH and C_o=94uF are selected for this operating condition. 2 x 47uF capacitors are used for the 94uF C_o.

The output voltage ripple test waveform is shown as Figure 3-1, the output voltage ripple pk-pk amplitude is about 5.7mV and it is much larger than the requirement.

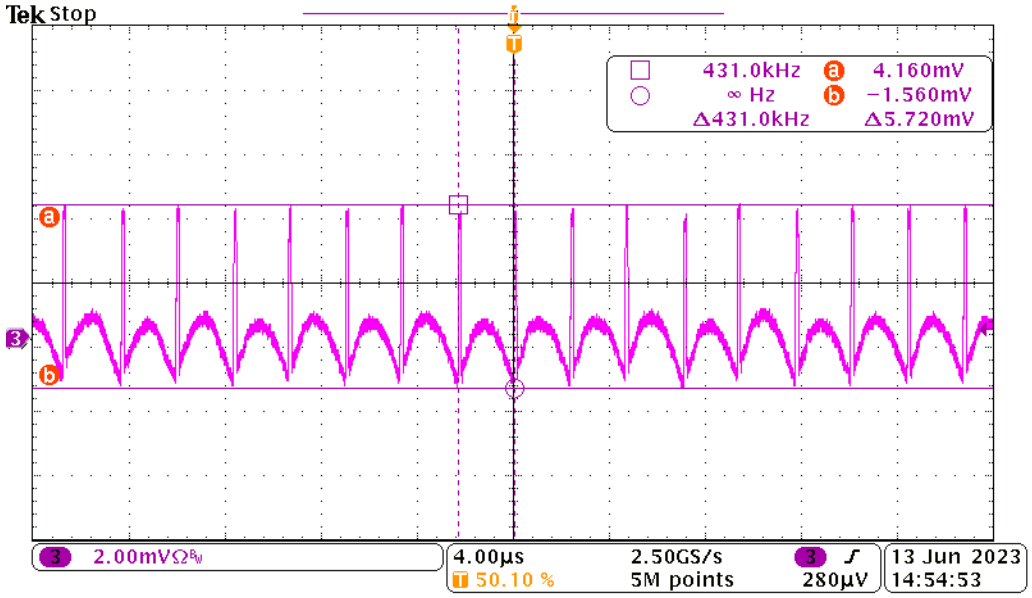

Figure 3-1. Output Voltage Ripple Without Second Stage Filter

Then the proposed components selection method of second stage filter is verified. With same 2 x 47uF as the total capacitance for both first stage and second stage filters, we set the C_o=1x47uF and C_2=1 x 47uF. Substituting all parameters into Equation 7, L_2≥14.9nH could be got as the restriction for 800uV output voltage ripple.

Select L_2=20nH and Figure 3-2 shows the output voltage ripple with second stage filter. The output voltage ripple amplitude is 640uV pk-pk and could satisfy the 800uV requirement.

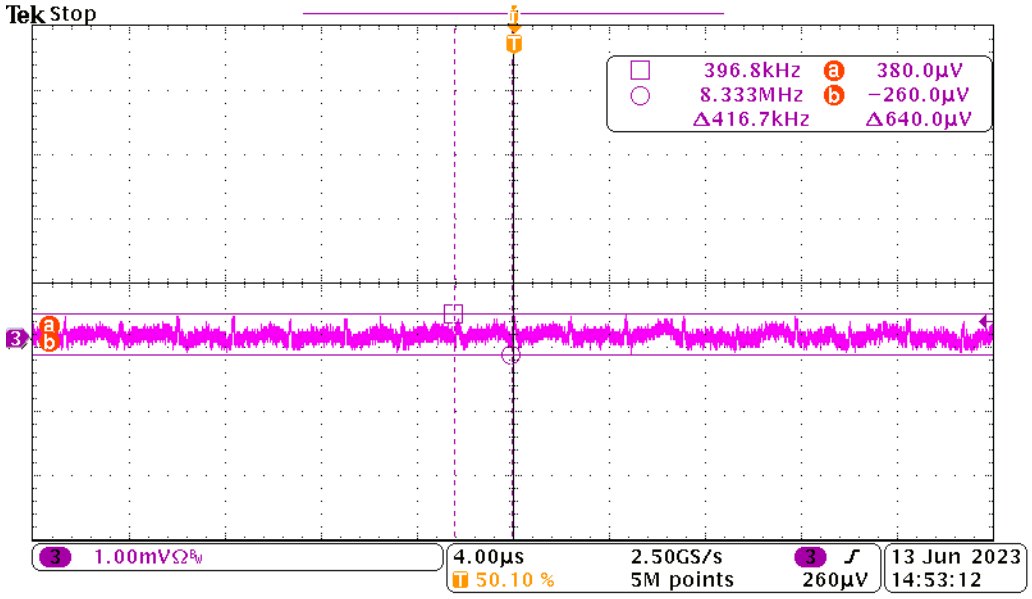

Figure 3-2. Output Voltage Ripple with Second Stage Filter

The effectiveness of proposed design method is verified by the example. More experimental results are shown in Section 7.

4 How to Estimate Inductance of Ferrite Bead for Ripple Reduction

In real implementation of 2nd stage filter, ferrite beads are often used as the L_2 of 2nd stage filter to provide nH level inductance. In the specs and data of a ferrite bead, normally an impedance value at a certain frequency at 100MHz and an impedance curve related with frequency are given.

An intuitive approach to estimate the inductance is dividing the given impedance by 2πF (like 2π x 100MHz). But that is not always correct, and we need to read the impedance curve to check if the inductance is dominant factor at given frequency point. Here we use two ferrite beads from Murata as examples for illustration: BLE18PS080SN1 and BLM18SN220TH1.

In the specs of those two ferrite beads, the impedance value at 100MHz are given. But as shown in Figure 4-1 and Figure 4-2, the dominant factors of impedance are different in those two parts at 100MHz frequency.

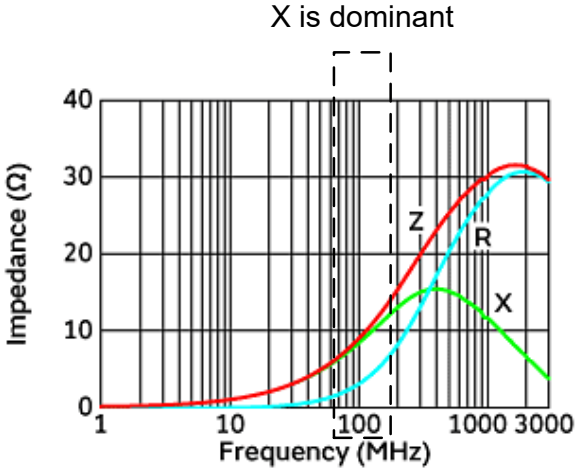

Figure 4-1. BLE18PS080SN1 Impedance VS Frequency

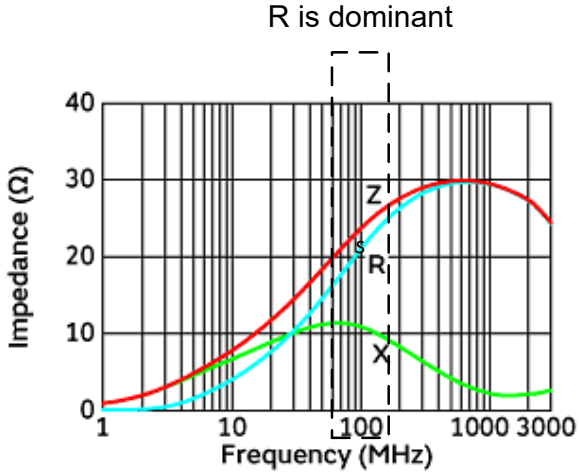

Figure 4-2. BLM18SN220TH1 Impedance VS Frequency

In Figure 4-1, inductive reactance X determined by L is the dominant part of impedance Z at 100MHz for BLE18PS080SN1. So, if assuming the inductance has small variation with frequency, it makes sense to estimate the L value by using impedance 8.5Ω divide (2π x 100MHz), and we can get inductance 13.5nH at 100MHz.

But in Figure 4-2, the inductive reactance X determined by L is not the dominant part of impedance Z at 100MHz for BLM18SN220TH1. So we cannot use similar method to directly calculate inductance based on the given impedance value at 100MHz. Instead, we can read an inductive reactance value from impedance at lower frequency.

Consider that we use 500kHz switching frequency of TPS62933F, a more accurate value can be read from lowest frequency in the given curve, which is 1MHz point.

Figure 4-3 and Figure 4-4 show above two beads inductance VS frequency curves [7]. We can use BLE18PS080SN1 1MHz inductance 15.3nH, BLM18SN220TH1 1MHz inductance 103.4nH during 2nd LC filter design.

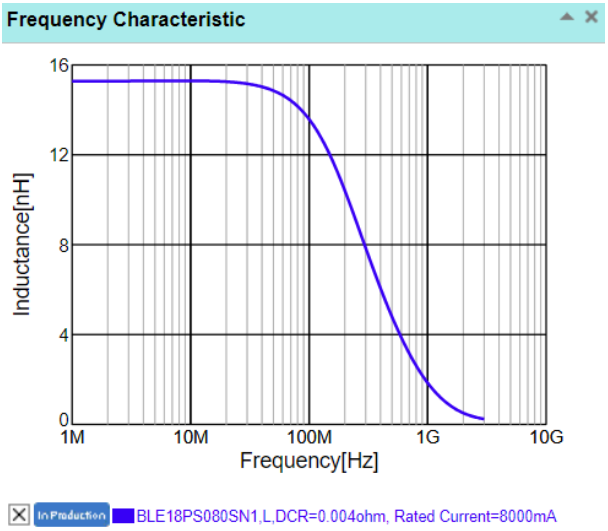

Figure 4-3. BLE18PS080SN1 Inductance VS Frequency

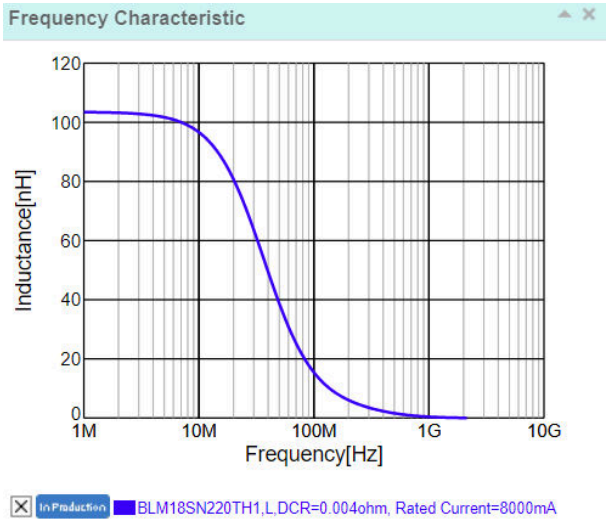

Figure 4-4. BLM18SN220TH1 Inductance VS Frequency

5 Summary

A components selection method for second stage filter is proposed in this application note to satisfy low output ripple requirement. With frequency domain analysis, the high frequency gain attenuation effects of second stage filter are studied first. Applying the gain attenuation effects on first stage output voltage ripple, the relation between second stage filter components value and second stage output voltage ripple is derived, which can directly guide the components selection.

To be noted, the effects of second stage filter on converter loop stability is not considered in this application note. In the *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part II: Hybrid Sense Network Design for Stability* application note, the stability analysis and components selection method for stability restriction are discussed.

6 References

1. Texas Instruments, *Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter*, application note.
2. Texas Instruments, *TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation*, data sheet.
3. Texas Instruments, *TPS6293x 3.8-V to 30-V, 2-A, 3-A Synchronous Buck Converters in a SOT583 Package*, data sheet.
4. Texas Instruments, *Output Ripple Voltage for Buck Switching Regulator*, application note.
5. Murata, *SimSurfing Design Tool,* simulation tool.
6. Texas Instruments, *Peak Current Mode Converter Secondary Stage Filter Design for Low Ripple Power – Part II: Hybrid Sense Network Design for Stability*, application note.

7 Appendix

For easy validation, the components value L, C_o and L_2 are fixed and given first. The limits of C_2 are calculated with Equation 7 and verified by experiments.

V_{in} (V)	V_o (V)	f_{sw} (kHz)	L (uH)	C_o (uF)	L_2 (nH)	Required Ripple (mV)	C_2 Low Limit (uF)	C_2 selection (uF)	Measured Ripple (mV)
12	1.2	1000	1	47	20	1	3.64	4.7	<0.8
12	1.6	1000	1.5	47	20	1	3.11	4.7	<0.8
24	1.2	500	2.2	47	20	1	27.96	30	<0.8
24	1.6	500	3.3	47	20	1	24.44	30	<0.8

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265