Application Note

Using the TPS629210-Q1 in an Inverting Buck – Boost Topology

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ABSTRACT

The need to generate negative rail for electronic designs is a common challenge. This application note illustrates how to design an inverting buck – boost using the highly efficient TPS629210-Q1. Such that a positive input voltage can be used to create a regulated negative output voltage. This application report details component selection criteria and equations, so that designers can appropriately scale the solution to their own requirements. The document also includes a design example along with captured waveforms. The same design is applicable to the TPS629210 and TPS629210E devices which are pin to pin compatible to TPS629210-Q1.

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1 Inverting Buck – Boost Topology

1.1 Concept

The inverting buck – boost topology is very similar to the buck topology. In the buck configuration shown in Figure 1-1, the positive connection (V_{OUT}) is connected to the inductor and the return is connected to the integrated circuit (IC) ground. However, in the inverting buck – boost configuration shown in Figure 1-2, the IC ground is used as the negative output voltage (labeled as $-V_{OUT}$). What used to be the positive output in buck configuration is used as the ground (GND). This inverting buck – boost topology allows the output voltage to be inverted and is always lower than the ground.

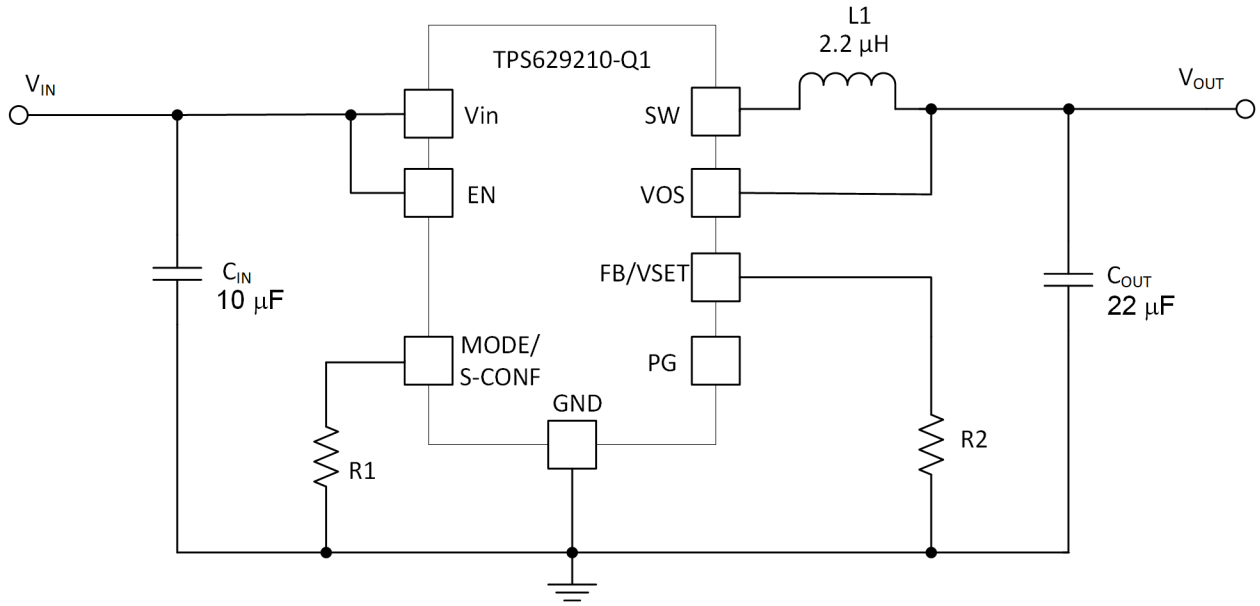


Figure 1-1. TPS629210-Q1 Buck Topology

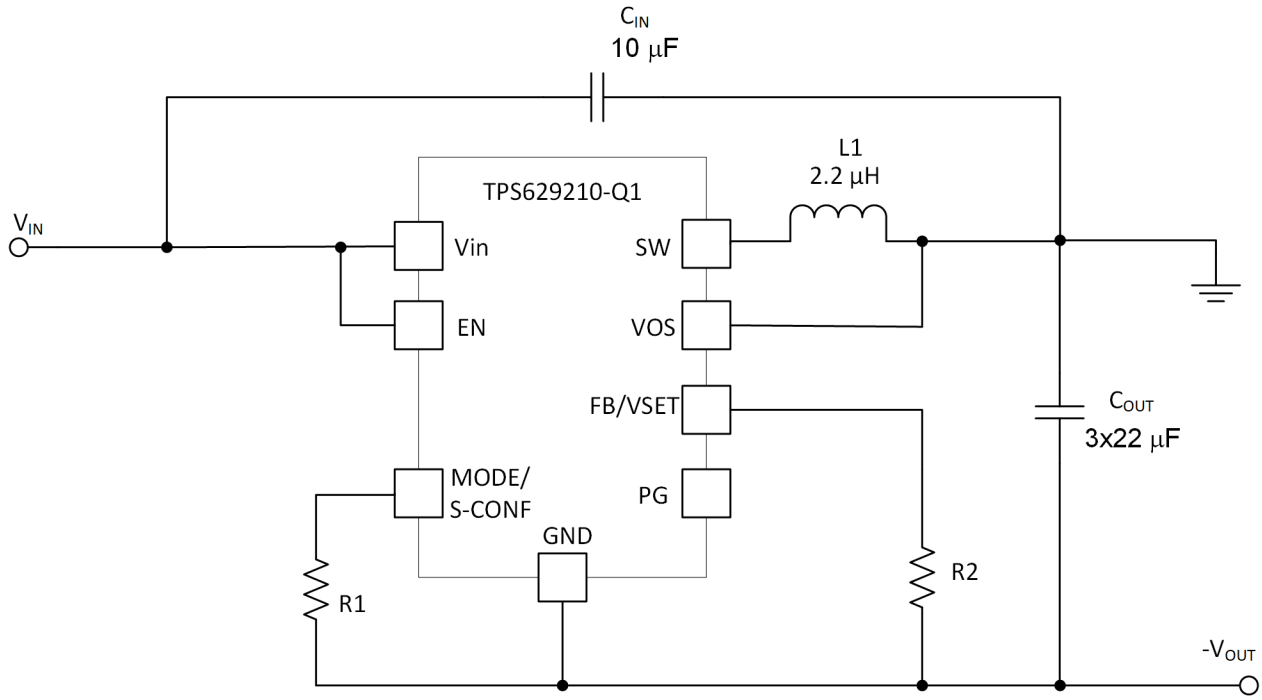


Figure 1-2. TPS629210-Q1 Inverting Buck – Boost Topology

The circuit operation is different in the inverting buck - boost topology than in the buck topology. Figure 1-3 (a) illustrates that the output voltage terminals are reversed, though the components are wired the same as a buck converter. During the on time of the control MOSFET, shown in Figure 1-3 (b), the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the off time of the control MOSFET and the on time of the synchronous MOSFET, shown in Figure 1-3 (c), the inductor provides current to the load and the output capacitor. These changes affect many parameters described in the upcoming sections.

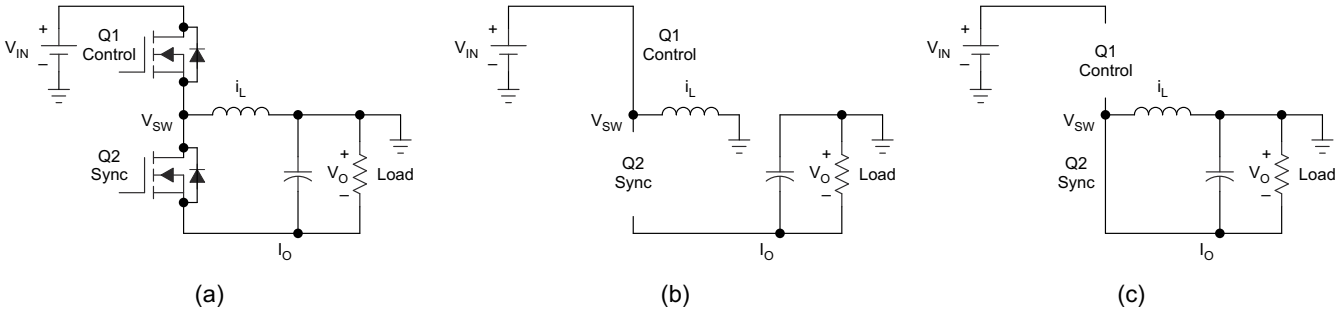


Figure 1-3. Inverting Buck – Boost Configuration

1.2 Output Current Calculations

The average inductor current is affected in this topology. In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck - boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output capacitor and the load (see Figure 1-3). Knowing that the off time is 1-D of the switching period, then the average inductor current is:

$$I_{L(avg)} = \frac{I_{OUT}}{1 - D} \tag{1}$$

The duty cycle for the typical buck converter is simply V_{OUT} / V_{IN} but the duty cycle for an inverting buck - boost converter becomes:

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} x \frac{1}{\eta} \tag{2}$$

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses and yields a more accurate maximum output current result. Where V_{OUT} is a negative value. The peak to peak inductor ripple current is calculated as:

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} \tag{3}$$

Where,

ΔI_L (A): Peak to peak inductor ripple current

D: Duty cycle

η: Efficiency

f_S (MHz): Switching frequency

L (µH): Inductance

V_{IN} (V): Input voltage with respect to ground, instead of IC ground or -V_{OUT}.

Finally, the maximum inductor current becomes:

$$I_{L(max)} = I_{L(avg)} + \frac{\Delta I_L}{2} \quad (4)$$

For an output voltage of –3.3 V, 2.5 MHz switching frequency, 2.2 µH inductor, and an input voltage of 12 V, the following calculations produce the maximum allowable output current that can be delivered based on the 1.3 A minimum current limit (I_{LIM}) of TPS629210-Q1. The efficiency term is estimated at 85%.

$$D = \frac{V_{OUT}}{V_{OUT} - V_{IN}} x \frac{1}{\eta} = \frac{-3.3}{-3.3 - 12} x \frac{1}{0.85} = 0.254 \quad (5)$$

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} = \frac{12 \times 0.254}{2.5MHz \times 2.2\mu H} = 0.554\ A \quad (6)$$

Rearranging Equation 4 and setting $I_{L(max)}$ equal to the minimum value of I_{LIM}, as specified in the data sheet, gives:

$$I_{L(avg)} = I_{L(max)} - \frac{\Delta I_L}{2} = 1.3 - \frac{0.554}{2} = 1.023\ A \quad (7)$$

This result is then used in Equation 1 to calculate the maximum achievable output current:

$$I_{OUT} = I_{L(avg)} \times (1 - D) = 1.023 \times \left(1 - 0.254\right) = 0.763\ A \quad (8)$$

Table 1-1 provides several examples of the calculated maximum output current for different output voltages (–5 V, –3.3 V and –1.2 V) based on an inductor value of 2.2 µH and 3.3 µH with 2.5 MHz switching frequency, respectively. Increasing the inductance and/or input voltage allows higher output current in the inverting buck - boost topology. The maximum output current for the TPS629210-Q1 in the inverting buck - boost topology are frequently lower than 1 A due to the fact that the average inductor current is higher than that of a typical buck. The output current for the same three output voltages and different input voltages are displayed in Figure 1-4.

Table 1-1. Maximum Output Current Calculation for Different Values of V_{IN}, V_{OUT} and Inductance

V_{IN} (V)	12	12	12	12	12	12	5	5	5	5	5	5
V_{OUT} (V)	–5	-3.3	–1.2	-5	–3.3	-1.2	-5	-3.3	-1.2	-5	-3.3	-1.2
L(µH)	2.2	2.2	2.2	3.3	3.3	3.3	2.2	2.2	2.2	3.3	3.3	3.3
f_S (MHz)	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5
η (%)	86	85	80	86	85	80	86	85	80	86	85	80
I_{LIM}(A)	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
D	0.342	0.254	0.114	0.342	0.254	0.114	0.581	0.468	0.242	0.581	0.468	0.242
ΔI_L (A)	0.746	0.554	0.248	0.497	0.369	0.165	0.529	0.425	0.22	0.352	0.283	0.147
$I_{L(avg)}$ (A)	0.927	1.023	1.176	1.051	1.115	1.217	1.036	1.087	1.19	1.124	1.158	1.227
I_{OUT} (A)	0.610	0.763	1.0	0.692	0.832	1.0	0.434	0.579	0.902	0.470	0.616	0.93

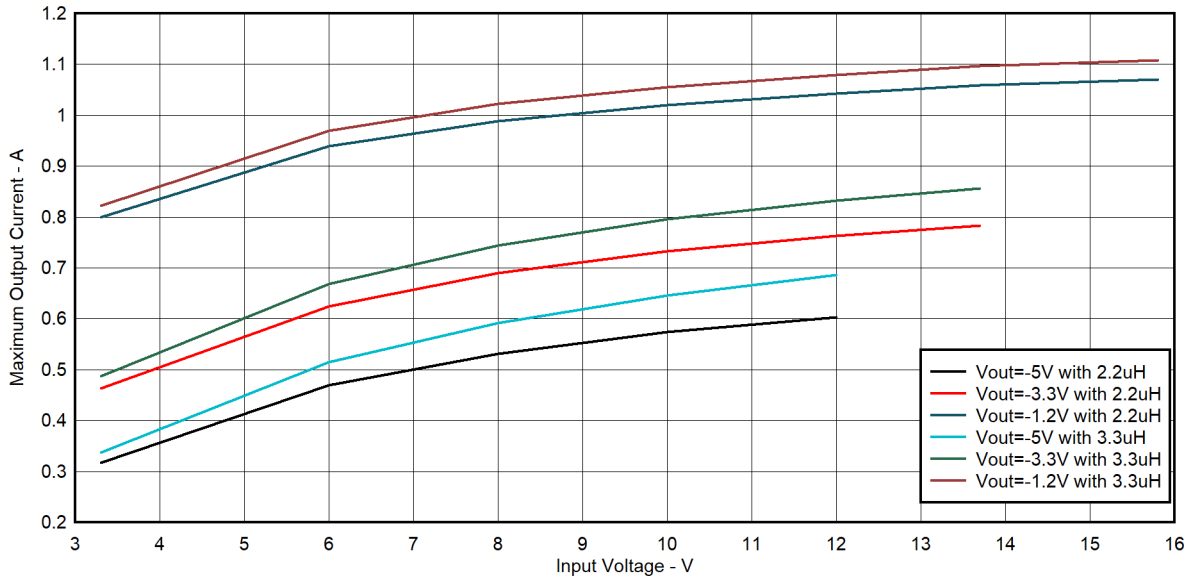


Figure 1-4. Maximum Output Current vs Input Voltage

1.3 V_{IN} and V_{OUT} Range

The input voltage that can be applied to an inverting buck - boost converter is less than the input voltage that can be applied to the same buck converter. This is because the ground pin of the IC is connected to the negative output voltage. Therefore, the input voltage across the device is V_{IN} to $-V_{OUT}$, not V_{IN} to ground. Thus, the input voltage range of the TPS629210-Q1 is 3 V + V_{OUT} to 17 V+ V_{OUT}, where V_{OUT} is a negative value.

The output voltage range is the same as when configured as a buck converter, but negative. The TPS629210-Q1 output voltage for the inverting buck - boost topology should be set between –0.6 V to –5.5 V for external divider and -0.4 V to -5.5V for internal divider (VSET). It can be set the same way as in the buck configuration, with two resistors connected to the FB pin or VSET configuration. Due to the increased noise of the inverting buck - boost topology, for a more robust design, recommend use internal feedback (VSET) or use smaller value resistors than are used for the buck configuration.

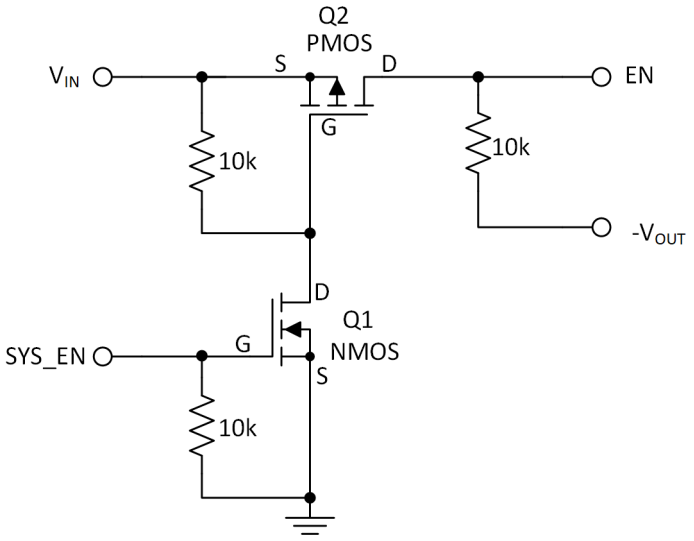
2 Digital Pin Configurations

2.1 Enable Pin

The TPS629210-Q1 is enabled once the voltage at the EN pin trips its threshold and the input voltage is above the UVLO threshold. The device stops operation once the voltage on the EN pin falls below its threshold or the input voltage falls below UVLO threshold.

Because $-V_{OUT}$ is the IC ground in this configuration, the EN pin must be referenced to $-V_{OUT}$ instead of ground. In the buck configuration, 1 V is considered to turn on and less than 0.9 V is considered to turn off. In the inverting buck-boost configuration, however, the $-V_{OUT}$ voltage is the reference; therefore, the high threshold is 1 V + V_{OUT} and the low threshold is 0.9 V + V_{OUT}. Where V_{OUT} is a negative value. For example, if V_{OUT} = –3.3 V, the V_{EN} is considered at a high level for voltages above –2.3 V and at a low level for voltages below –2.4 V.

This behavior can cause difficulties enabling or disabling the device, since in some applications, the IC providing the EN signal might not be able to produce negative voltages. The level shifter circuit shown in Figure 2-1 alleviates any difficulties associated with the offset EN threshold voltages by eliminating the need for negative EN signals.



$-V_{OUT}$ is the negative output voltage of the inverting buck-boost converter

Figure 2-1. EN Pin Level Shifter

The positive signal (SYS_EN) that originally drove EN is instead tied to the gate of Q1. When Q1 is off , Q2 sees 0 V across its V_{GS}, and also remains off. In this state, the EN pin sees –3.3 V for $-V_{OUT}$= - 3.3 V which is below the low level threshold and it disables the device.

When SYS_EN provides enough positive voltage to turn Q1 on (V_{GS} threshold as specified in the MOSFET data sheet), the gate of Q2 sees ground through Q1. This drives the V_{GS} of Q2 negative and turns Q2 on. Now, V_{IN} ties to EN through Q2 and the pin is above the high level threshold, turning the device on. Be careful to ensure that the V_{GD} and V_{GS} of Q2 remain within the MOSFET ratings during both the enabled and disabled states. Failing to adhere to this constraint might result in MOSFET damage. A small size complementary N and P Channel 60V (D-S) MOSFET Si1029X from Vishay is used in the design.

If the system enabling and disabling of the TPS629210-Q1 is not desired, the EN pin can be directly connected to V_{IN} or a voltage divider connected to V_{IN}. We strongly recommend to add a voltage divider placeholder (R3/R4) between V_{IN} and EN pin which is shown in Figure 2-2. Recommend R3:R4≥2:1 ratio to ensure V_{IN} >2.85 V UVLO before EN> 1V which the internal circuit of device is ready before EN is fully enabled. UVLO and EN falling thresholds become relative to $-V_{OUT}$ instead of GND . For example, UVLO falling=2.75 V +V_{OUT} and EN falling= 0.9 V + V_{OUT}. Where V_{OUT} is a negative value. Customer can scale the voltage divider R3/R4 ratio based on the real application. This is a reliable solution to eliminate any start up and shut down related issues.

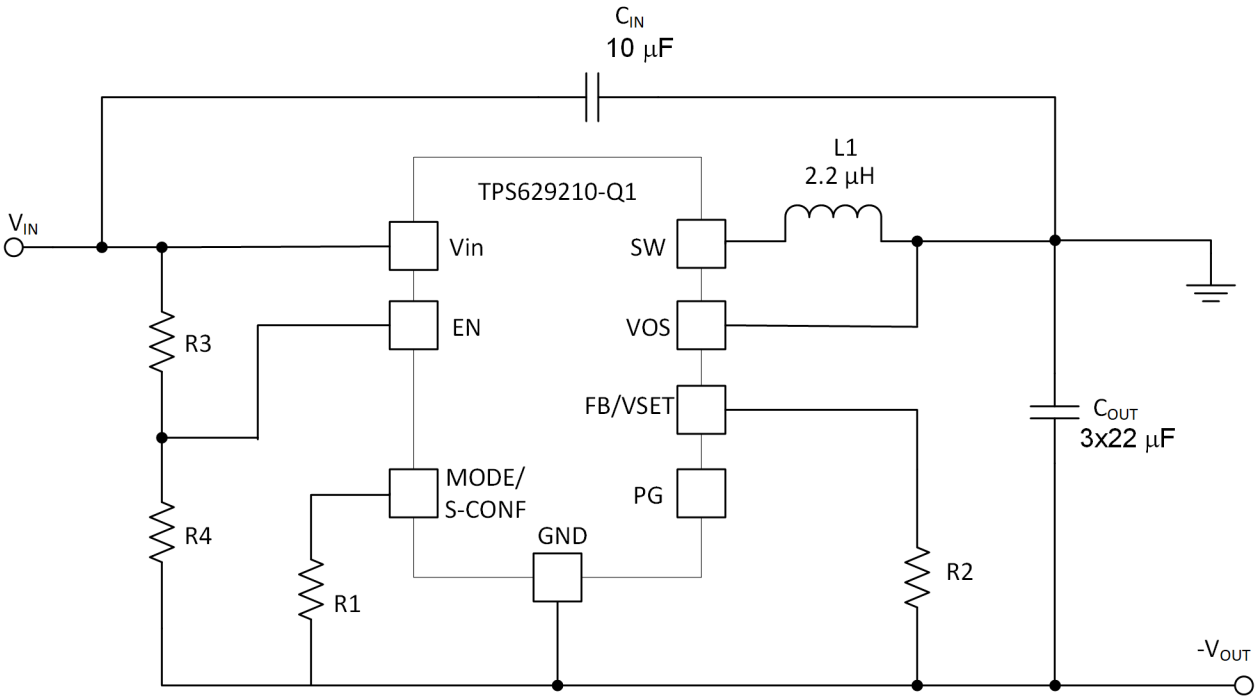


Figure 2-2. EN pin with voltage divider

2.2 MODE/S-CONF Pin

TPS629210-Q1 has a MODE/S-CONF pin which can be used to customize the device behavior. Refer to schematic in Figure 2-2 and Figure 2-3

- Selects device configuration (switching frequency, internal or external feedback, output discharge, Forced PWM and Auto PFM/PWM mode) by connecting a single resistor between this pin and $-V_{OUT}$ (IC GND pin) or connecting directly to V_{IN} or $-V_{OUT}$ (IC GND pin).
  - A 2.5 MHz switching frequency setting is recommended for inverting buck-boost application due to lower inductor ripple current. The design example selects MODE/S-CONF resistor as 27.4 k which configures internal feedback, 2.5 MHz switching frequency, Auto PFM/PWM with AEE and output discharge enabled.
  - Note that the maximum output current will be reduced while using 2.2uH inductor and 1MHz switching frequency. 3.3 uH or larger inductance is strongly recommended for 1 MHz switching frequency configuration, otherwise special care has to be taken to make sure the half ripple current doesn't trip the negative current limit under no load condition.
- Dynamic MODE option is an advance feature which allows MODE/S-CONF pin to actively switch between Forced PWM and Auto PFM/PWM during operation. This feature provides user with the option of controlling when/if the device enters power save mode (DCM). In the inverting buck-boost topology, V_{IN} is HIGH and $-V_{OUT}$ is LOW, but this is only possible by driving the MODE/S-CONF pin between V_{IN} and $-V_{OUT}$. This can be done with the same type of circuit used to drive the EN pin HIGH and LOW as shown in Figure 2-1
- The external feedback configuration shown in Figure 2-3 , where the MODE/S-CONF pin can be tied to $-V_{OUT}$ directly to configure as 2.5 MHz switching frequency, Auto PFM/PWM with AEE and output discharge enabled.

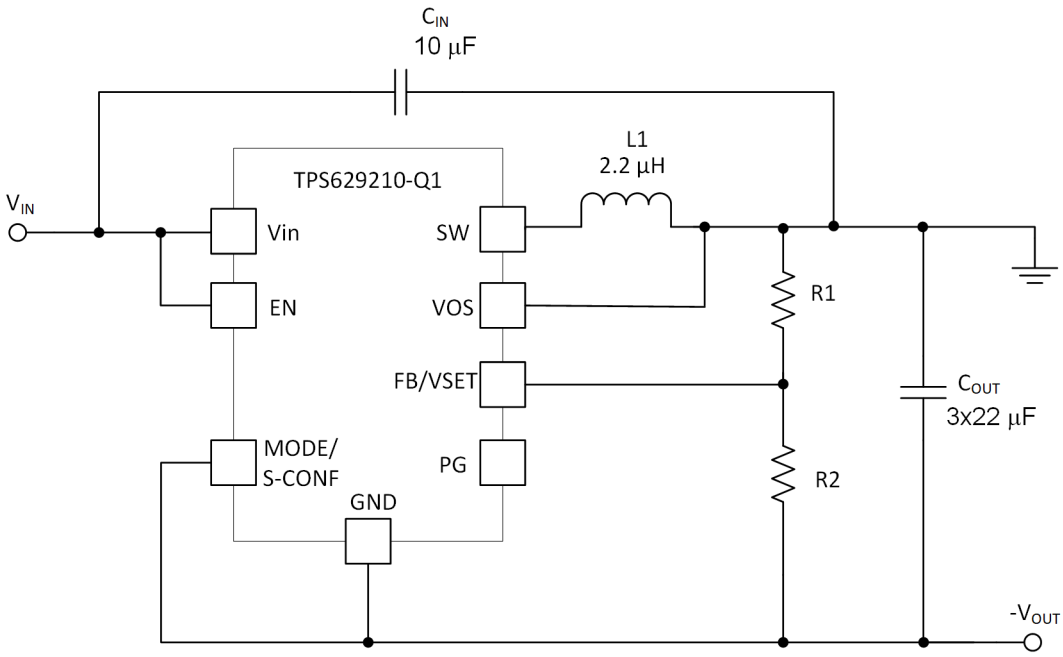


Figure 2-3. External Feedback with 2.5 MHz Switching Frequency and Auto PFM/PWM

2.3 Power Good Pin

The TPS629210-Q1 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG pin is an open-drain output that requires a pullup resistor. Because - V_{OUT} is the IC ground in this configuration, the PG pin is referenced to -V_{OUT} instead of ground, which means that the TPS629210-Q1 pulls PG to -V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PG pin, because in some applications the IC detecting the polarity of the PG pin might not be able to withstand negative voltages. The level shifter circuit shown in Figure 2-4 alleviates any difficulties associated with the offset PG pin voltages by eliminating the negative output signals of the PG pin. If the PG pin functionality is not needed, it can be left floating without this circuit. Note that to avoid violating its absolute maximum rating, the PG pin should not be driven more than 17 V above the negative output voltage (IC ground).

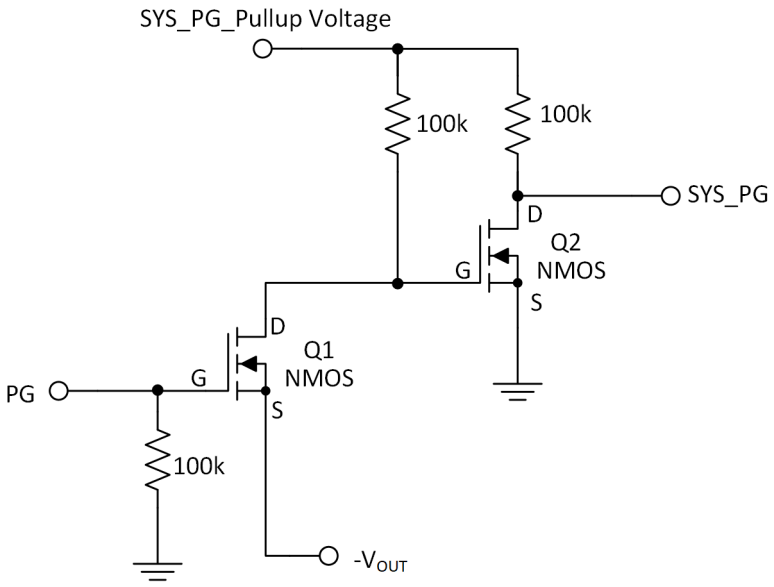


Figure 2-4. PG Pin Level Shifter

Connecting TPS629210-Q1 PG pin to the gate of Q1, when the PG pin is pulled low(-V_{OUT}), Q1 is off and Q2 is on because its V_{GS} sees SYS_PG_Pullup Voltage. SYS_PG is then pulled to ground.

When PG pin is pulled high(GND), the gate of Q1 is pulled to ground potential turning it on. This pulls the gate of Q2 below ground, turning it off. SYS_PG is then pulled up to its pullup voltage. Note that the pullup voltage must be at an appropriate logic level for the circuitry connected to the SYS_PG. A small size dual N Channel 20V(D-S) MOSFET Si1902CDL from Vishay is used in the design.

3 Design Considerations

The inductor and output capacitor need to be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor is different from the buck converter. See Selecting L and Cout for Stability for a discussion of stability.

3.1 Input Capacitor Selection

An input capacitor, C_{IN}, is required to provide a local bypass for the input voltage source. A low ESR input capacitor is best for input voltage filtering and minimizing interference with other circuits. For most applications, a 10-µF or 22-µF ceramic capacitor is recommended from V_{IN} to ground. The C_{IN} capacitor value can be increased without any limitation for better input voltage filtering.

For the inverting buck – boost configuration of the TPS629210-Q1, it is not recommended to install a capacitor from V_{IN} to - V_{OUT}. Such a capacitor, if installed, provides an AC path from V_{IN} to - V_{OUT}. When V_{IN} is applied to the circuit, this dV/dt across a capacitor from V_{IN} to - V_{OUT} creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the TPS629210-Q1 and is not recommended. Therefore, a capacitor from V_{IN} to - V_{OUT} is not needed or recommended. If such a capacitor (C_BYP) is present, then a Schottky diode should be installed on the output per Figure 3-1. Startup testing should be conducted to ensure that the SW and VOS pins are not driven more than 0.3 V below IC ground when V_{IN} is applied.

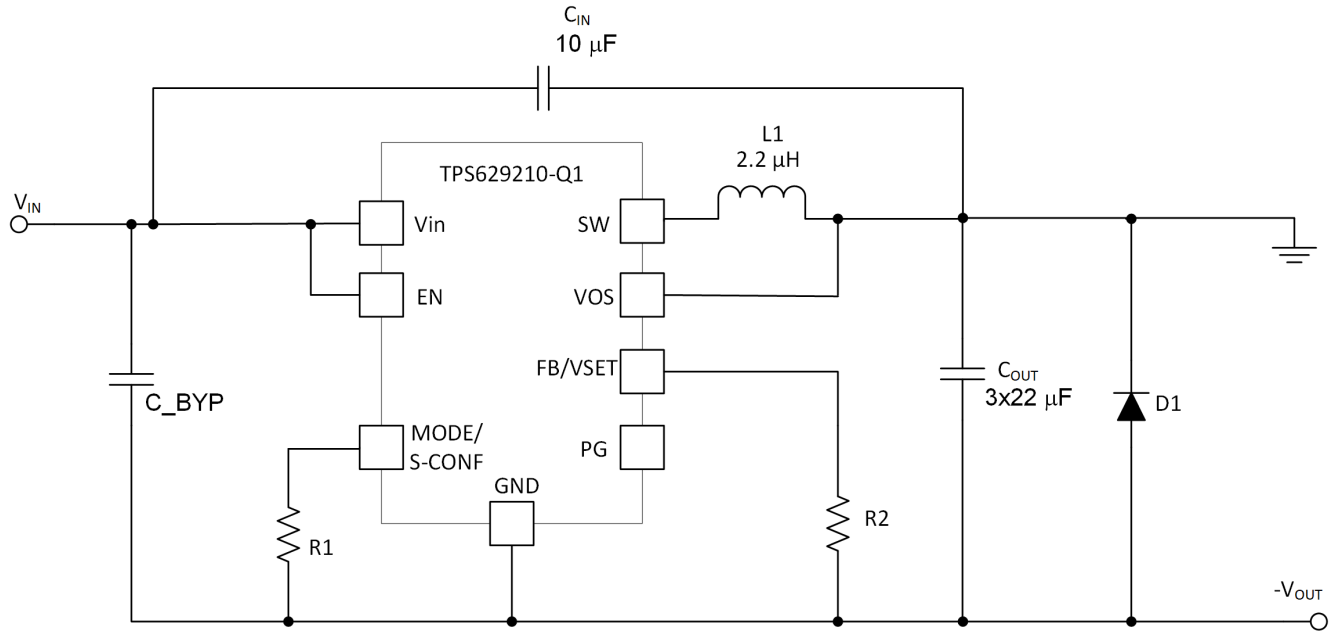


Figure 3-1. If Installing C_BYP, Installing Schottky D1 is Required

3.2 Output Inductor Selection

When selecting the inductor value for the inverting buck - boost topology, the equations provided in the Output Current Calculations section should be used instead of the ones provided in the data sheet. These equations help to select the right inductance by designing for a maximum inductor current ($I_{L(max)}$) for a given inductance. $I_{L(max)}$ should be kept below the minimum current limit value of TPS629210-Q1 (1.3 A) for a reliable design. The recommended output inductor for TPS629210-Q1 is in the range of 2.2uH to 3.3uH. See Selecting L and Cout for Stability for the stability impact of the inductor selection.

3.3 Stability Limits and Output Capacitor Selection

The switch node, inductor current, and the output voltage ripple during steady state are signals that need to be checked first for the stability of the system. Oscillations on the output voltage and the inductor current, and jitter on the switch node are good indicators of the instability of the system. Load transient response is another good test for stability, as described in the Simplifying Stability Checks application report.

The inverting buck - boost topology contains a right-half plane (RHP) zero which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. As a result the phase margin of the closed loop response is reduced which leading to potential instability and poor load transient response. Equation 9 estimates the frequency of the RHP zero. Where V_{OUT} is a negative value.

$$f_{(RHP)} = \frac{-\left(1 - D\right)^2 \times V_{OUT}}{\left(D \times L \times I_{OUT} \times 2 \times \pi\right)} \quad (9)$$

It is recommended to keep the loop crossover frequency to 1/10th of the RHP zero frequency. Doing this requires either decreasing the inductance to increase the RHP zero frequency or increasing the output capacitance to decrease the crossover frequency. Note that the RHP zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. A larger output capacitance is recommended for low input (< 12 V) voltage designs. How to Measure the Control Loop of DCS-Control™ Devices explains how to measure the control loop of a DCS-Control™ device.

The recommended minimum output capacitance for TPS629210-Q1 inverting buck-boost topology is 3x22 µF. The output capacitance used with inverting buck-boost is larger than would normally be used with a buck due to its right-half plane zero. More output capacitance pushes the crossover frequency of the control loop down to frequency lower enough so that the right-half plane zero is sufficiently higher for stability.

4 Layout Considerations

A proper layout is critical for the operation of inverting buck - boost topology. See Figure 4-1 for recommended layout for TPS629210-Q1 inverting buck - boost application.

- The input capacitor C1 should be placed as close as possible between the V_{IN} pin and GND.
- The output capacitors C2, C4, C5 should be placed as close as possible between $-V_{OUT}$ pin and GND.
- VOS trace should be routed/Kelvined to the positive terminal (GND) of output capacitors, not simply tied to the system GND plane.
- Sensitive nodes like FB/VSET and VOS need to be connected with short wires and not nearby high dv/dt signals(like SW). As they carry information about output voltage, they should be connected as close as possible to actual output voltage (at the pad of output capacitor). For this design, there is no feedback resistors required (float the FB/VSET pin) resulting in a -3.3V output voltage using the internal VSET.
- MODE/S-CONF pin resistor R3 should be kept close to IC and connect directly to its pin.

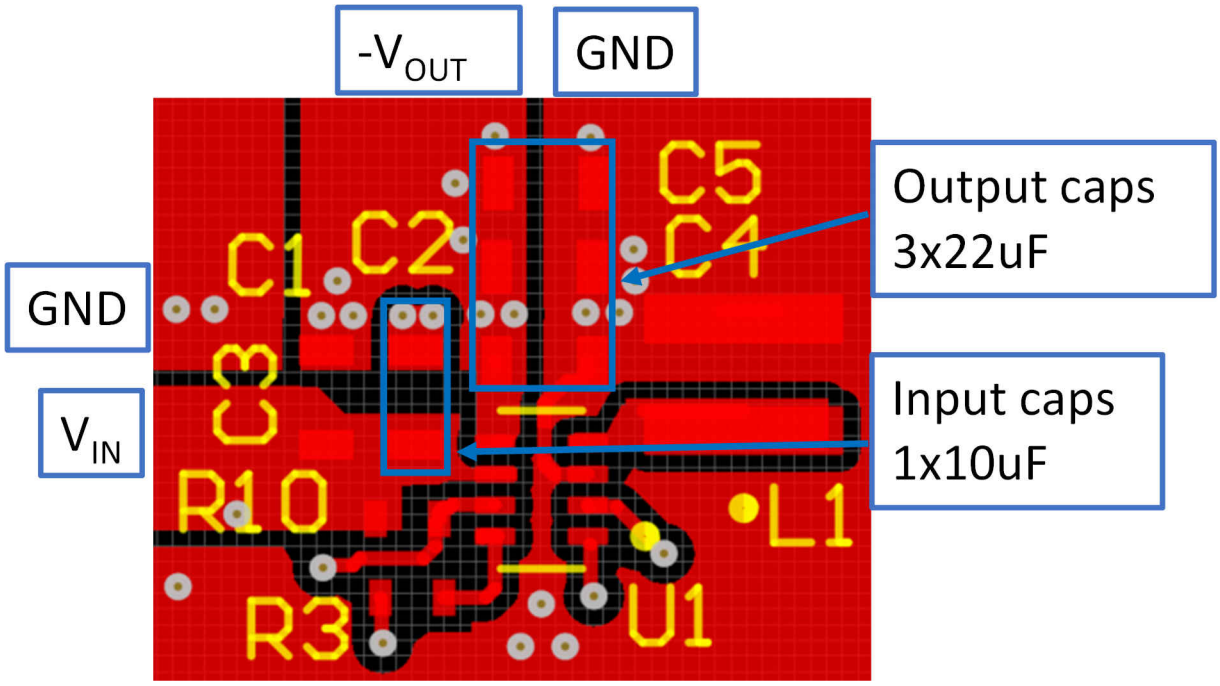


Figure 4-1. TPS629210-Q1 Inverting Buck – Boost Layout Example

5 How to Modify a Buck to Inverting Buck-Boost?

To achieve the inverting function, the output terminals are swapped such that V_{OUT} becomes GND and the GND terminal becomes -V_{OUT}. Everything was GND is now labeled - V_{OUT}. The modification shown in .Figure 5-1

- The reference designators are identical between buck and inverting buck boost, except for the input capacitors C1, C2 and C3 whose connections need to be changed
- Remove input capacitor C1, C2 and C3 from the EVM, but save them to re-install later
- Install 2 pcs 22 µF, 10V ceramic output capacitors at C6 and C7. Might add more to reduce output ripple and improve loop stability.
- Change the value of R1 and R2 to set the appropriate output voltage

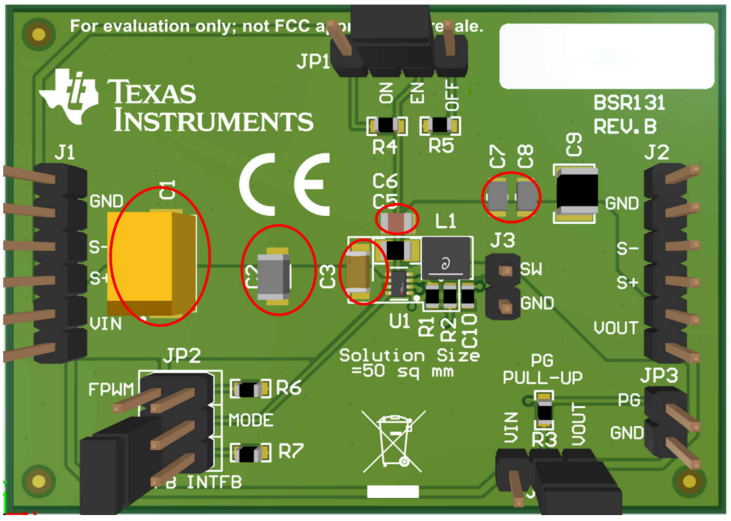


Figure 5-1. Buck EVM Before Modification

Installing the input capacitor C1, C2 and C3 guidance shown in Figure 5-2

- Because existing input GND pads of input capacitors C3 are not the correct electrical location on existing EVM. So put a electrical tape to cover that GND pad of C3 to avoid wrong connection.
- The existing pad for V_{IN} connection of C3 is used and a wire is added to complete the connection to GND, which is Vout on the PCB
- Re-install C1, C2 and C3 as highlighted in red square area
- Input supply can be applied between VIN and GND, which is V_{OUT} on the PCB
- Load can be applied between -V_{OUT} and GND

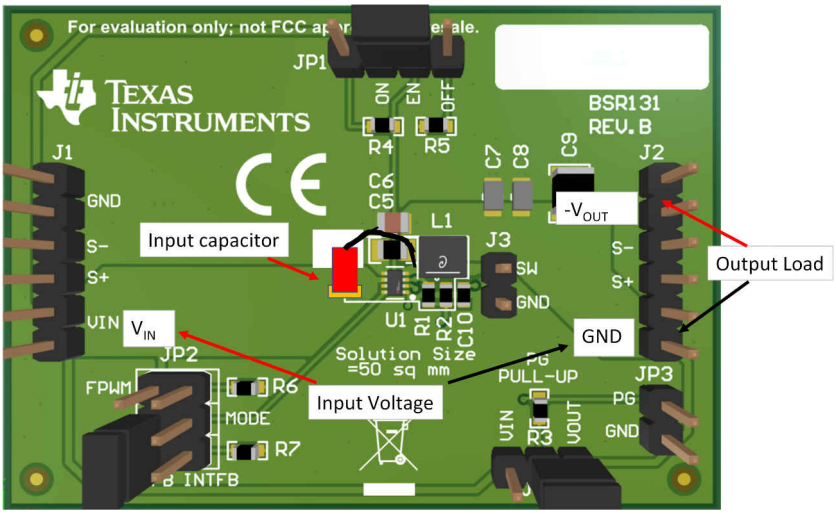


Figure 5-2. Inverting Buck-Boost EVM After Modification

6 Typical Performance and Waveforms

The application circuit shown in Figure 6-1 is used to generate the data for typical performance. L1 is a 2.2 µH inductor from Coilcraft, whereas a 2.2 µH XGL3530-222MEC is used. The output capacitors used 3x22 µF, 10 V, 0603, X5R ceramic capacitor. The input capacitor used 10 µF, 25V, 0603, X5R. Unless otherwise specified, V_{IN} = 12 V and V_{OUT} = –3.3 V, I_{OUT}=0 A to 0.76 A, 2.5 MHz, Auto PFM/PWM, internal feedback (VSET).

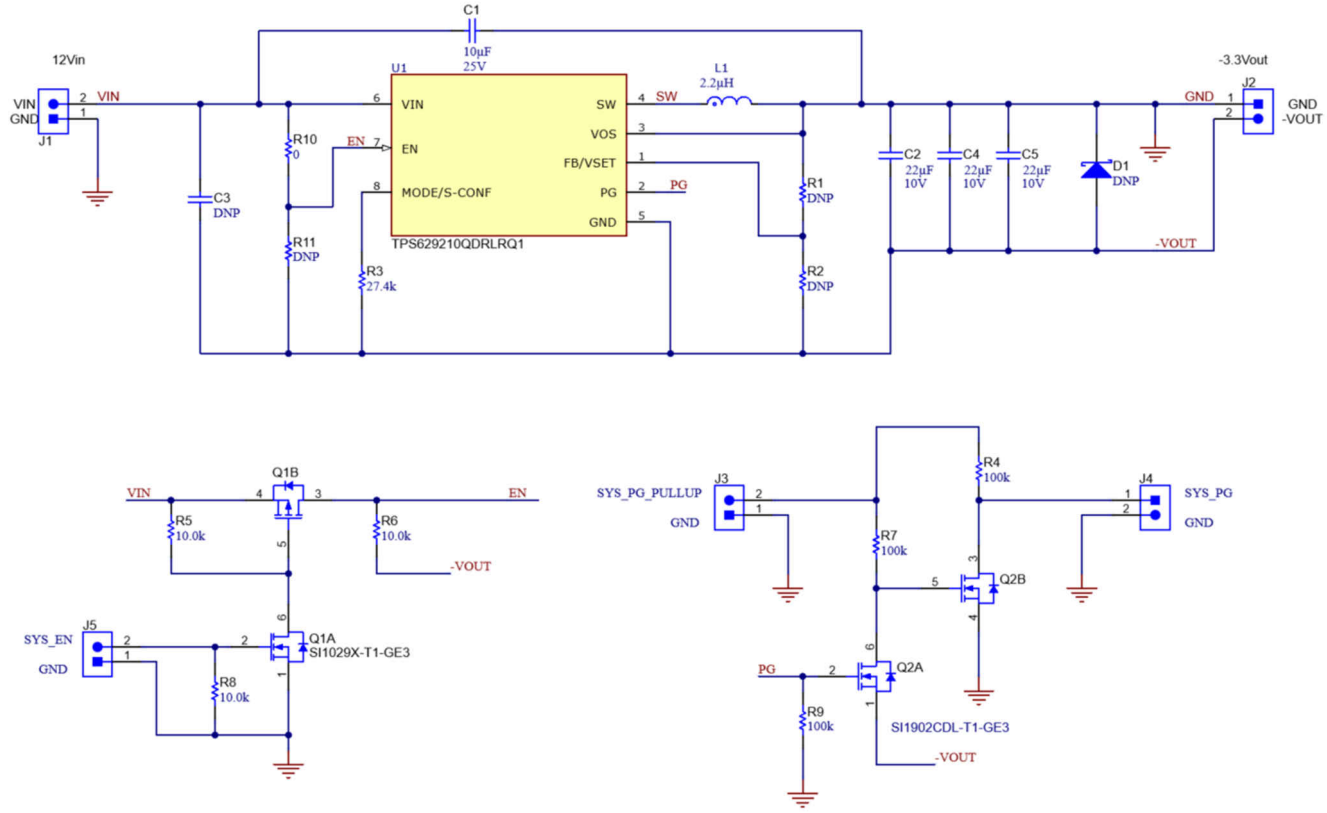


Figure 6-1. Schematic of Tested Circuit

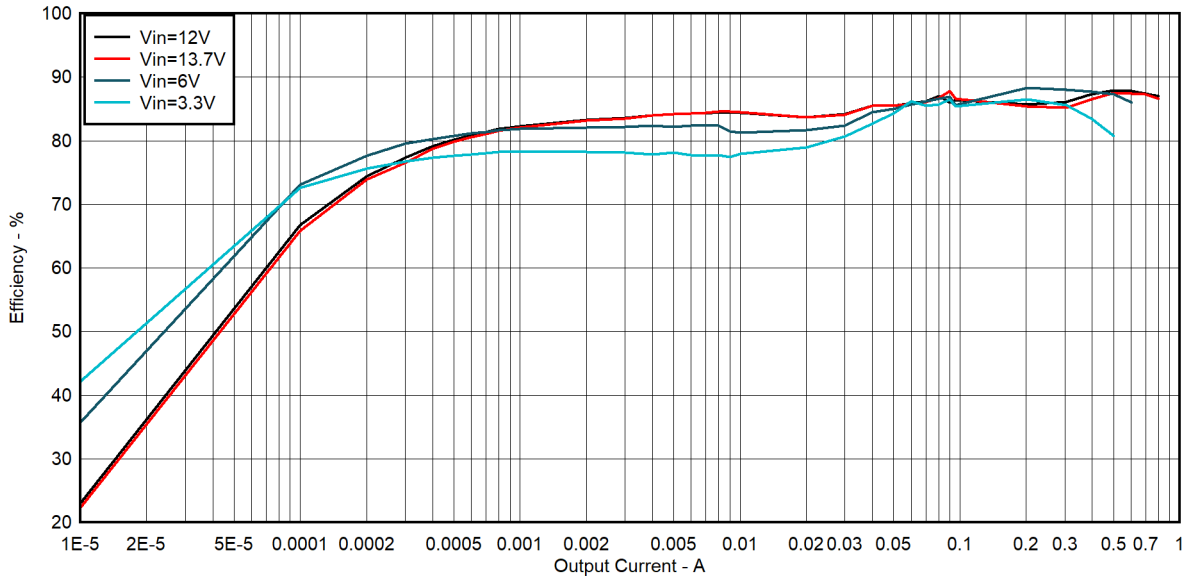


Figure 6-2. Efficiency with V_{OUT} = –3.3 V

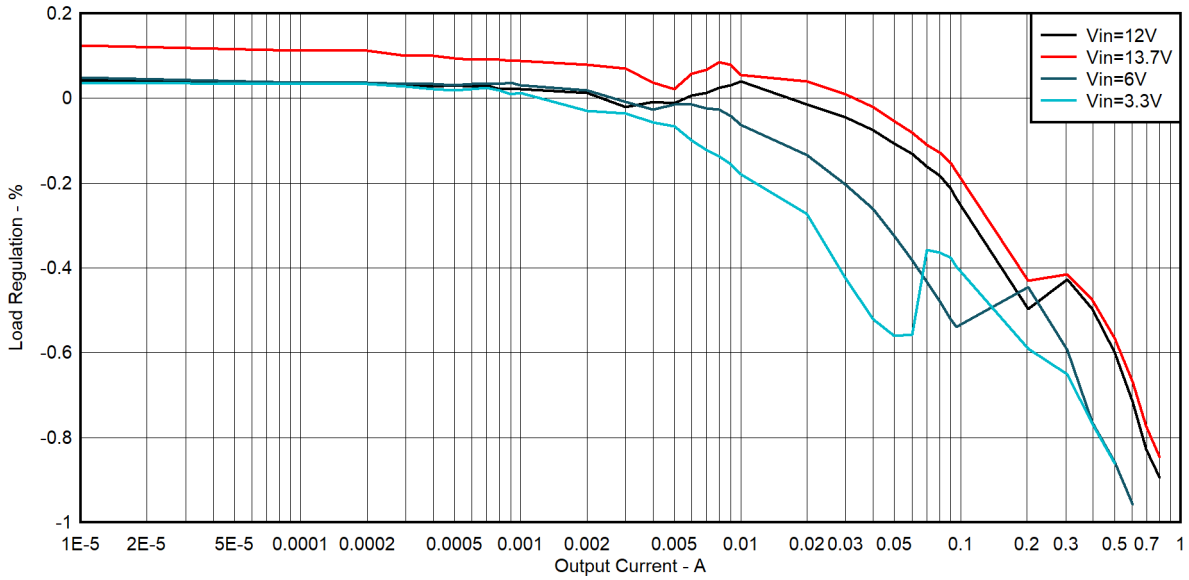


Figure 6-3. Load Regulation with V_{OUT} = –3.3 V

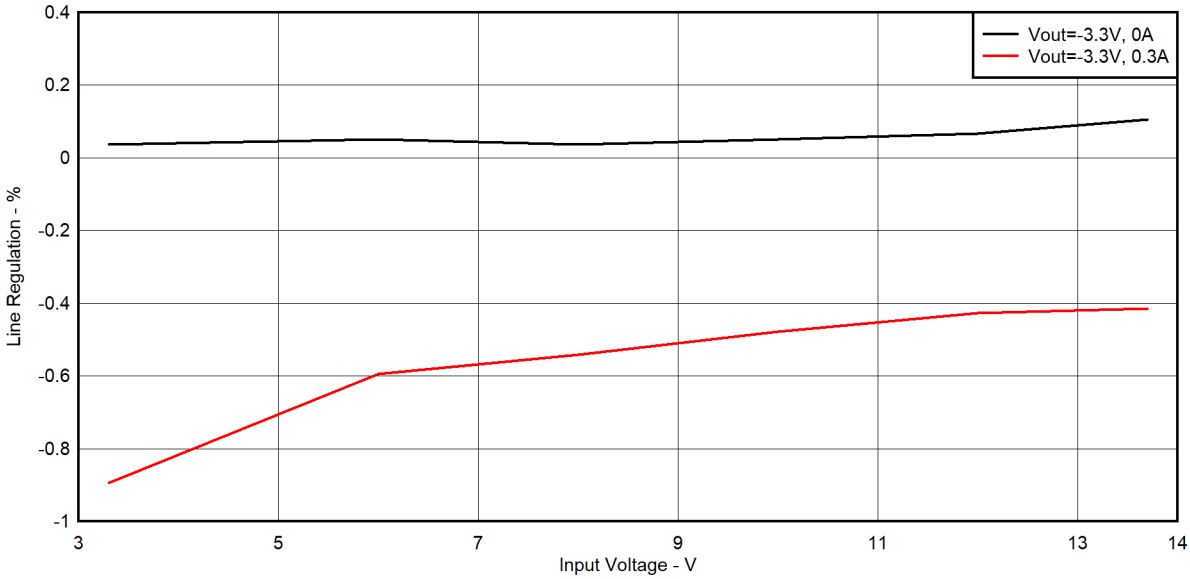


Figure 6-4. Line Regulation with V_{OUT} = –3.3 V , I_{OUT} = 0 A and 0.3 A

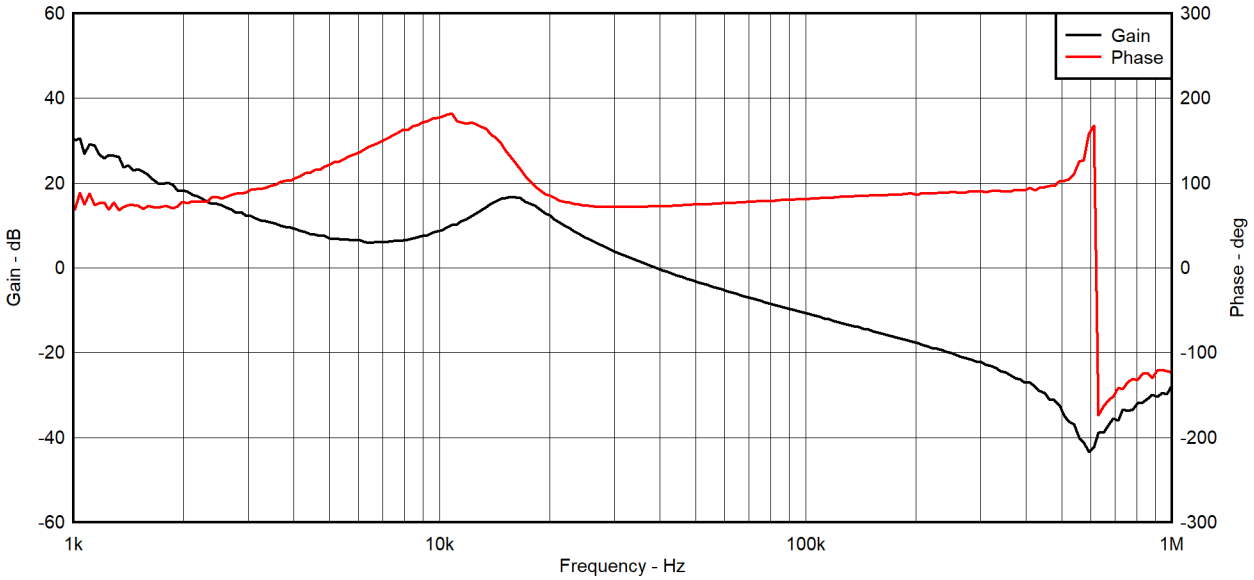


Figure 6-5. Loop Response with V_{IN} =12 V, V_{OUT} = –3.3 V, I_{OUT} = 0.5A

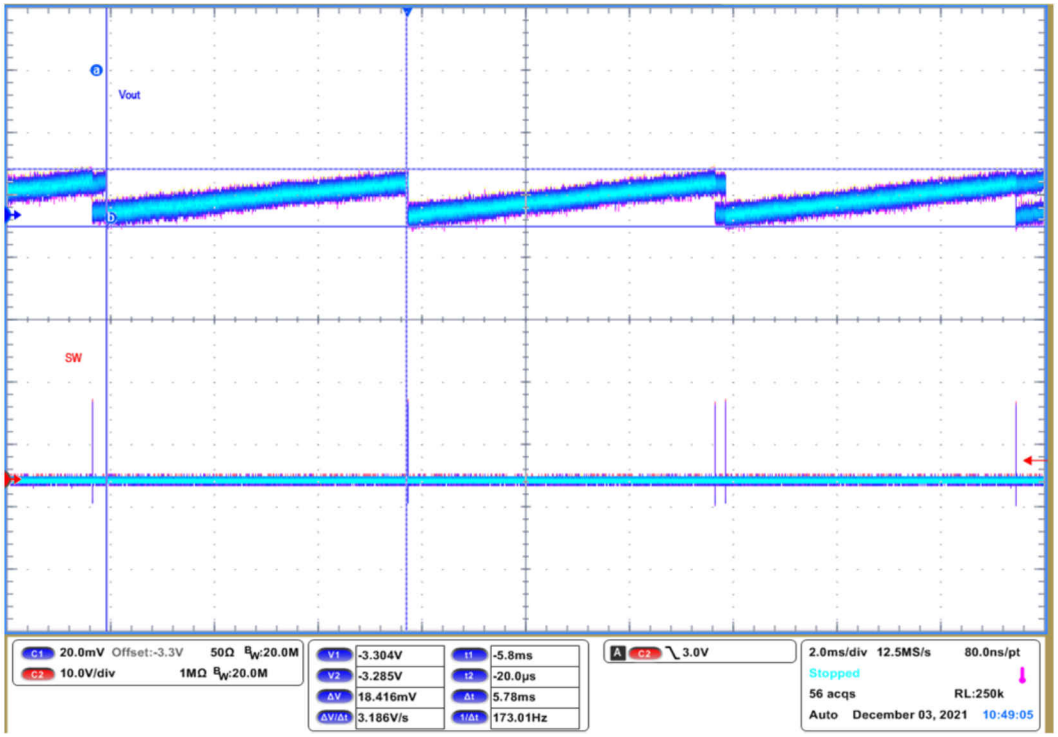


Figure 6-6. Output Voltage Ripple with V_{IN} = 12 V, V_{OUT} = -3.3 V, I_{OUT} = 0 A

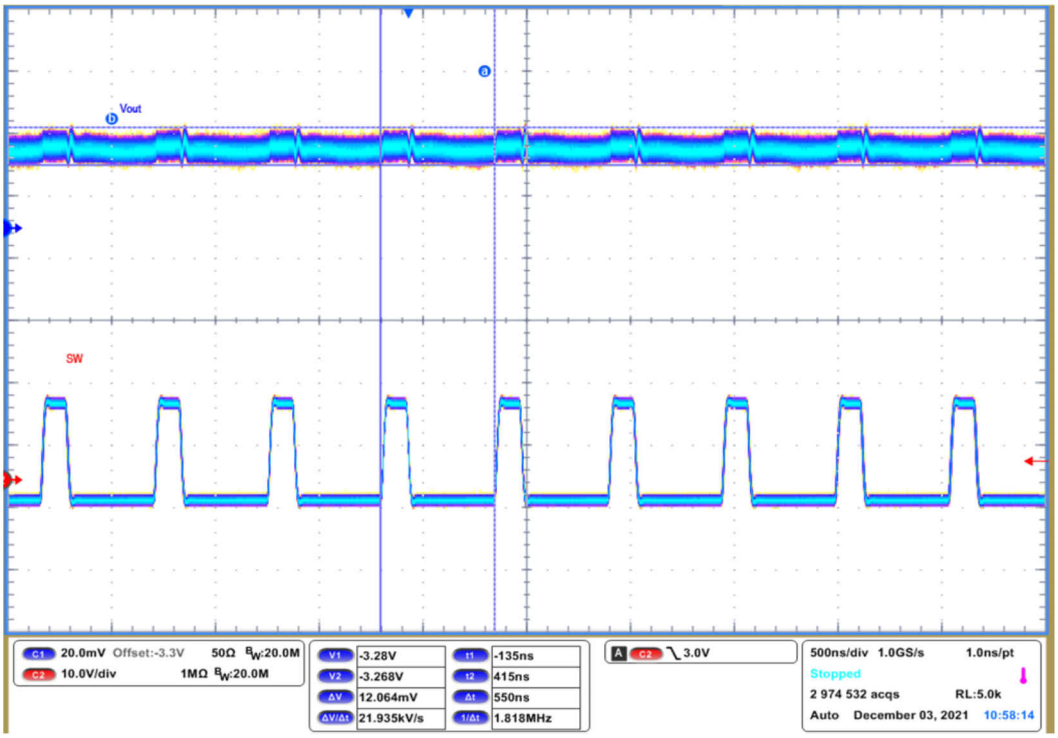


Figure 6-7. Output Voltage Ripple with V_{IN} = 12 V, V_{OUT} = -3.3 V, I_{OUT} = 0.5 A

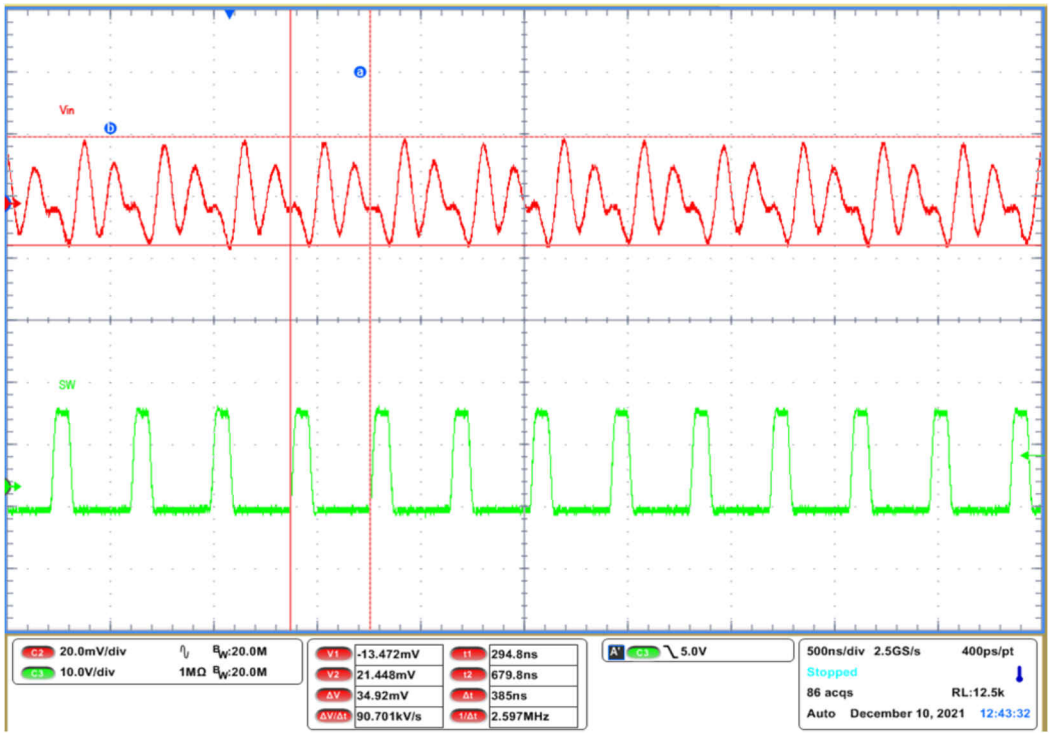


Figure 6-8. Input Voltage Ripple with V_{IN} = 12 V , V_{OUT} = -3.3 V, I_{OUT} = 0.5 A

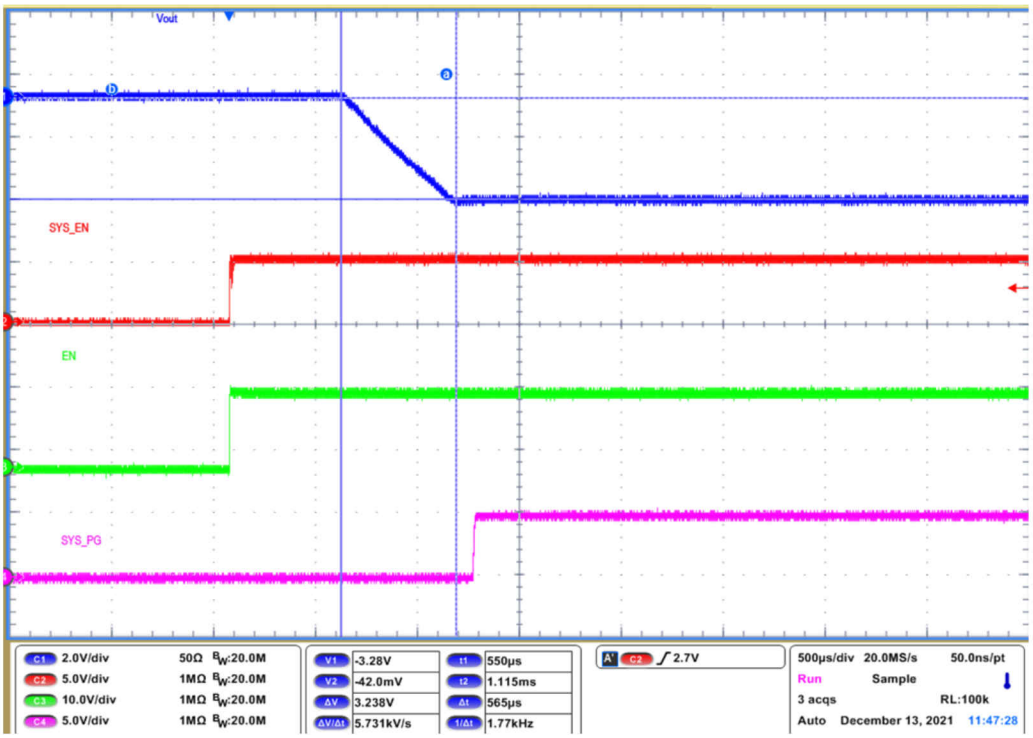


Figure 6-9. Enable Start up with V_{IN} = 12 V, V_{OUT} = -3.3 V, I_{OUT} = 0.5 A

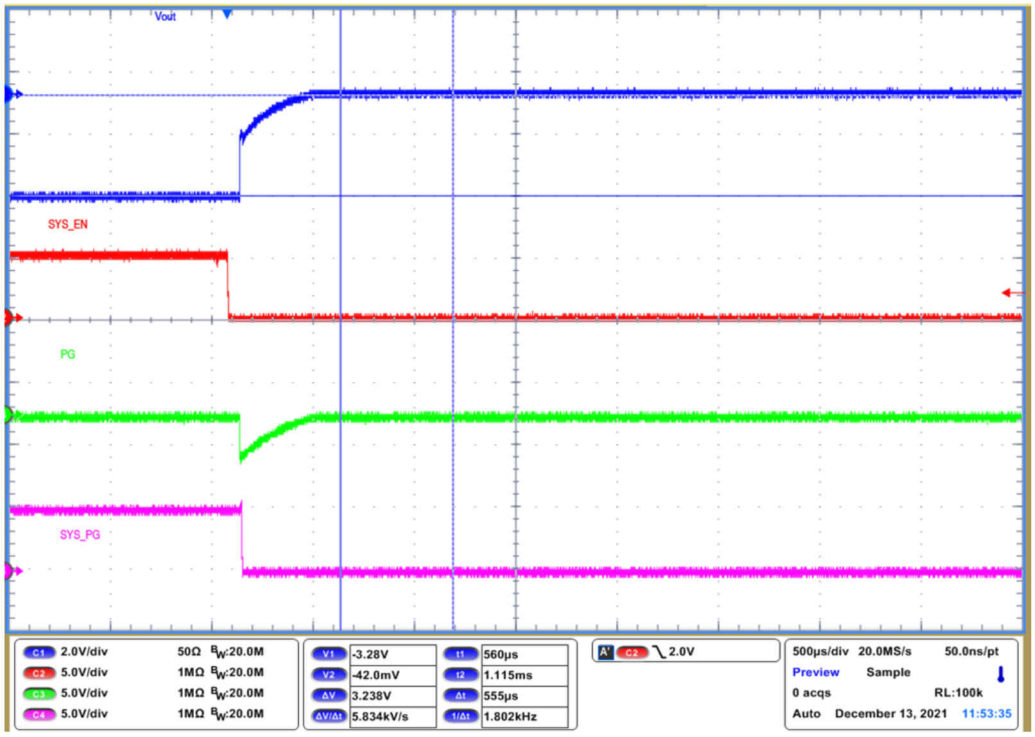


Figure 6-10. Enable shutdown with V_{IN}= 12 V, V_{OUT} = -3.3 V, I_{OUT} = 0.5 A

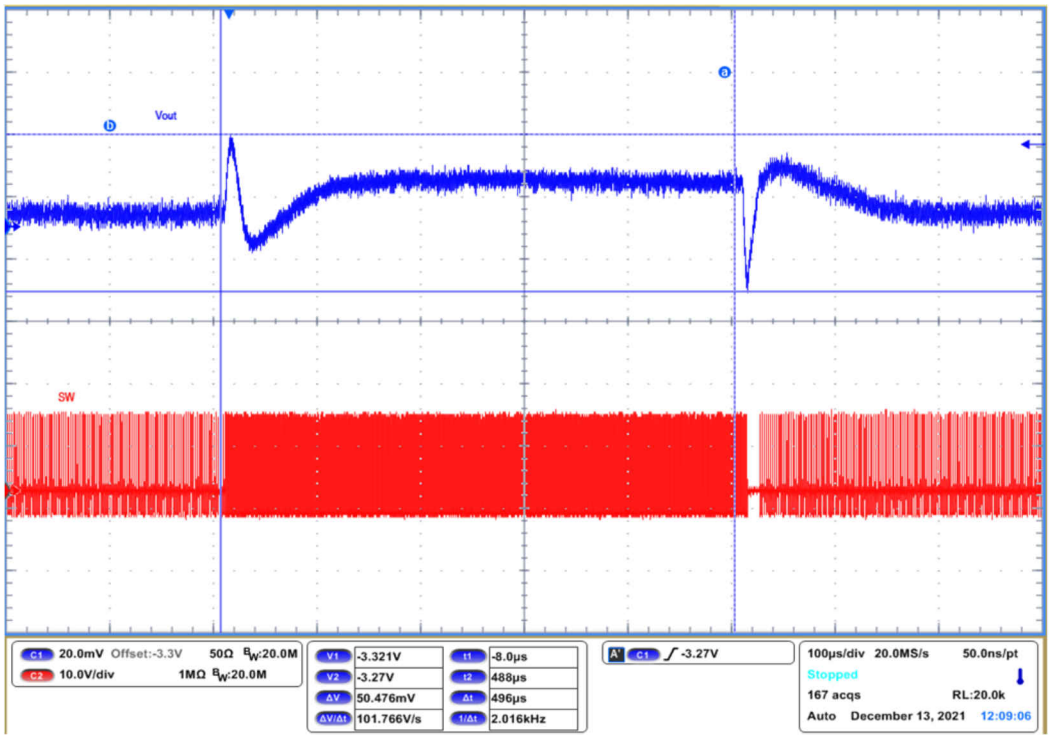


Figure 6-11. Load Transient with V_{IN} = 12 V, V_{OUT} = -3.3 V, I_{OUT} = 0.1 A to 0.6 A, Slew rate 1A/µs

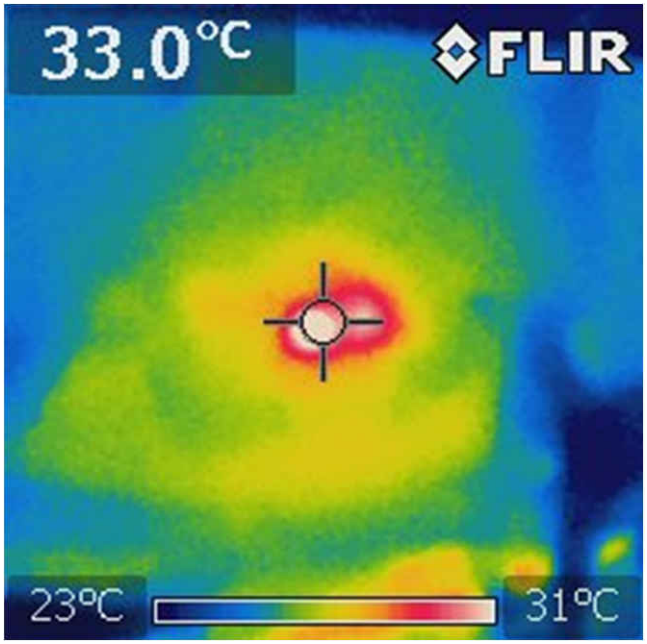


Figure 6-12. Thermal Performance with V_{IN} = 12 V, V_{OUT} =-3.3 V, I_{OUT} = 0.76 A, 10 mimutes soaking

7 Conclusion

The TPS629210-Q1 can be configured as an inverting buck boost converter to generate a negative output voltage. The inverting buck boost topology changes some system characteristics, such as input voltage range and maximum output current. This application report explains the inverting buck boost topology and how to select the external components with the changed system characteristics. Measured data from the example design is provided.

8 References

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