Application Brief

Why Radiation Hardness Matters for Point-of-Load Converters

Javier Valle, Adrian Helwig *Space Power*

Note

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Designing power-management systems for satellite payloads is becoming increasingly challenging because of the larger availability of space-qualified field programmable gate arrays (FPGAs) and their corresponding increase in processing capabilities. These processing capabilities come at the expense of the multiple rails required by the FPGA and a high-current, low-voltage core rail with very stringent voltage regulation requirements. Such requirements make earlier generation power-management designs less practical, since they cannot meet all of the size, weight, and radiation performance requirements of the satellite.

This application brief reviews a point-of-load (POL) power system architecture that highlights the relevance of radiation hardness performance, especially single-event effects, in meeting current FPGA voltage regulation requirements.

Spacecraft Electrical Power Systems Overview

Spacecraft electrical power systems (EPS) cover all aspects of power generation, energy storage, power distribution, and regulation – along with control. The EPS is divided into two subsystems, primary and secondary; an optimal combination of the two facilitates effective operation.

One part of the secondary power subsystem design process is the selection of appropriate POL converters, which can include both switching DC/DC regulators and low-dropout regulators. Switching regulators are the main focus of this article, as their higher efficiency makes them a popular choice for low-voltage, high-current FPGA power-supply core rails.

The manufacturing process of earlier generation space-grade FPGAs used larger structure geometries focused on single-event upset (SEU) mitigation, with hardening methods such as triplication of registers and dual interlocked storage memory cells. One advantage to this process was that the larger parasitic routing capacitances intrinsically filtered the single-event transients (SETs) inherent in radiation environments. The latest generation of FPGAs feature increased logic densities and smaller interconnects. As a result, SETs can be the dominant single-event effect (SEE) due to increased likelihood that the amount of electrical charge from an ion in space will affect sensitive nodes.

In modern satellites, the secondary power distribution unit must supply a wide variety of low voltages precisely and without fluctuations, even under severe load variations. Figure 1 is an example secondary power-distribution system.

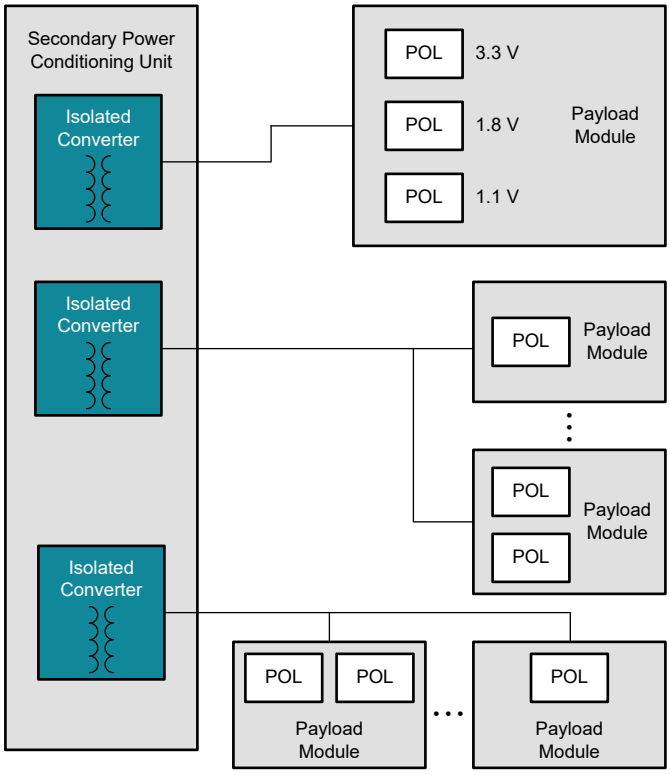

Figure 1. Secondary Power Distribution System

As shown, the modules use 3.3-V or 5-V distribution power rails to generate the supply voltages needed for the payload modules. These local voltages for these cards are commonly generated by compact and efficient DC/DC converters within the payload modules. The variety of supply voltages and current loads, along with increased power efficiency requirements, create a new design issue, making older, well established design approaches less practical and design goals more difficult to meet.

In addition, as shown in Figure 2, shrinking process nodes have resulted in core rails dropping to values below 1.0 V, requiring DC/DC converters to optimize performance for low-voltage regulation. Examples of this optimized performance include low-voltage and highly accurate internal references in response to advances in process nodes, adjustable slope compensation to better tailor the DC/DC converter for high-performance applications and the ability to parallel the converters to provide larger amounts of current for more system flexibility and reuse.

Simultaneously, with the growing complexity of satellite systems such as Earth observation programs with phased-array systems that use multiple FPGAs, selecting DC/DC converters with modern metal-oxide semiconductor field-effect transistor technology provides higher system efficiency. Higher system efficiency enables designers to downscale the solar array and battery weight and achieve one of the most important satellite design goals.

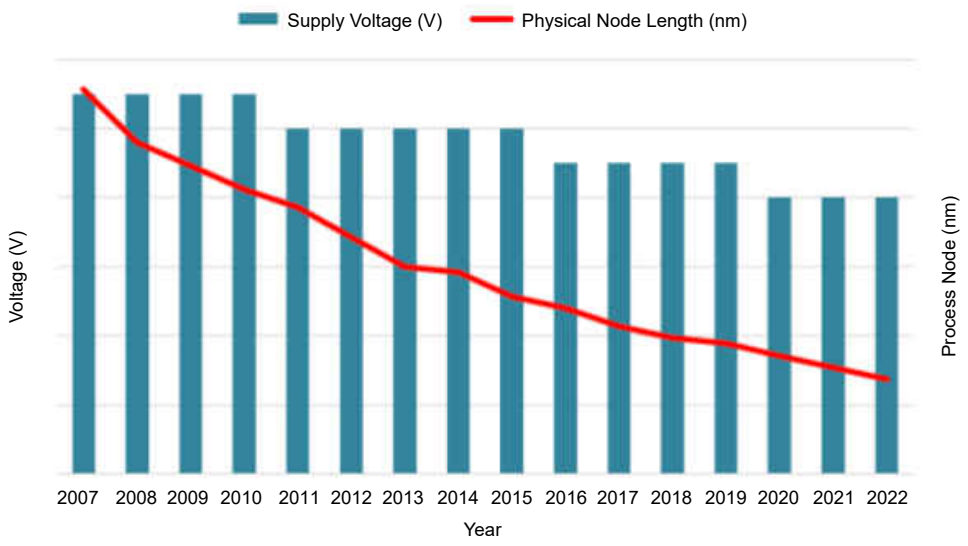

Figure 2. Process Node and Core Voltage Changes

Process node advancements in FPGA technology, along with the increase in processing capabilities, translates to tighter voltage regulation requirements.

Regulation tolerances for different FPGAs have changed as process nodes evolve. This evolution is drastically reducing margin and increasing the impact of SETs on POL switching regulators. Tightly regulating the core voltage ensures proper functionality, and locating the power source close to the new FPGA is now even more relevant to ensure an adequate voltage excursion caused by parasitic impedances.

POL converters can now be designed to precisely fit the requirements for reuse as a standard power interface for different payload modules. Although this standard power interface translates to significant cost and design time reductions, it is even more challenging because designers must consider different configurations (different input and output voltages at different output currents) of the POL converter during the design process. The process includes changing both power-stage components and the compensation network.

Therefore, it is important to select POL converters covering the required input and output voltage range that can also provide enough output current to the load.

Radiation Effects in Power Converters

On top of the stringent electrical requirements in modern power conditioning systems, designers need to consider radiation effects. In some cases, radiation effects requirements might not be as obvious as electrical requirements.

Radiation effects fall into two main categories: time dependent and random in time. Time-dependent effects are called dose effects and result in a parametric shift in the device, such as specifications falling outside of data sheet limits.

There are two categories of dose effects: total ionizing dose and neutron dose. Dose effects are typically, because of their time dependency, very well quantified and understood. As a result, designers can easily choose a space-grade power device that fits the time profile of a mission.

Random-in-time effects refer to SEEs. Given their random – and in some cases destructive – nature, it can be more challenging to understand SEEs and place them in context within a power conditioning system. There are two types of SEEs: destructive and nondestructive.

Destructive SEEs include single-event latch-up, single-event gate rupture and single-event burnout. The last two effects are particularly applicable to power field-effect transistors such as those used in the output stage of a DC/DC converter. Destructive SEEs, because of their destructive (pass or fail) nature, are also in some ways relatively easy to assess. As long as the manufacturer performs and properly documents the results for these

tests up to a specific effective linear energy transfer (LETeff), engineers can select a device suitable for the mission orbit.

Nondestructive SEEs include SETs, SEUs and single-event functional interrupts (SEFIs). The effects of nondestructive SEEs typically manifest as a glitch on the device output. The magnitude and behavior of the glitch depends on the LETeff as well as electrical testing conditions. Thus, nondestructive SEEs are a bit more convoluted than destructive SEEs.

SETs and SEFIs are effects typically associated with analog devices; SEUs apply to digital devices where a bit flip in a digital circuit occurs. Because most space power conditioning systems are analog-based, this brief focuses on SETs and SEFIs. These effects require detailed characterization to ensure that their behavior does not affect proper operation, nor potentially damage the load.

Depending on the type of load, the voltage regulation requirements might be stringent. As mentioned, high-performance, space-qualified FPGAs typically require a core voltage regulation accuracy of ±4%. This percentage includes electrical AC and DC regulation as well as aging and radiation effects typical of space applications. Therefore, DC/DC converters sensitive to radiation effects could suffer from variations in the output voltage larger than the accuracy requirement from the FPGA, triggering a power-on-reset of the FPGA if the output voltage drops (a negative SET), lost data and the need to reprogram the FPGA.

Conversely (and even more concerning), an increase in the output voltage (a positive SET) could violate the absolute maximum voltage rating of the FPGA and potentially damage the device. Large magnitude (> 4%) overshoots on the output of power devices are the most challenging because they can cause permanent damage (electrical overstress) in circuitry downstream.

Figure 3 shows an example of a SEFIs of the TPS50601A-SP, a space-grade 3-V to 7-V input, 6-A DC/DC converter. The SEFI occurs at LETeff = 86 MeV-cm^2/mg with a recovery time of about 4 ms.

In this example, there are no concerns about exceeding the rated voltage of the load, but rather that the load might stop operating – which could have system performance implications. At first glance, it may appear that the best solution is to choose a SEFI-free device up to the desired LETeff. However, the characterization of these effects is critical before such an assessment. The 62 overlapped events in Figure 3 show the repeatability of the SEFI.

After heavy ions characterization, event rates can be calculated to assess whether a device is suited for given applications. Texas Instruments calculated event rates for low-Earth orbit (LEO) applications such as the International Space Station and geosynchronous orbit (GEO) applications. The event rates indicate that the SEFI behavior shown in Figure 3 would occur every 700,000 years in LEO applications, or every 210,000 years in GEO applications.

For more details regarding the SEE performance of the TPS50601A-SP, see the full radiation report: *Single-Event Effects Test Report of the TPS50601A-SP Synchronous Step-Down Converter*.

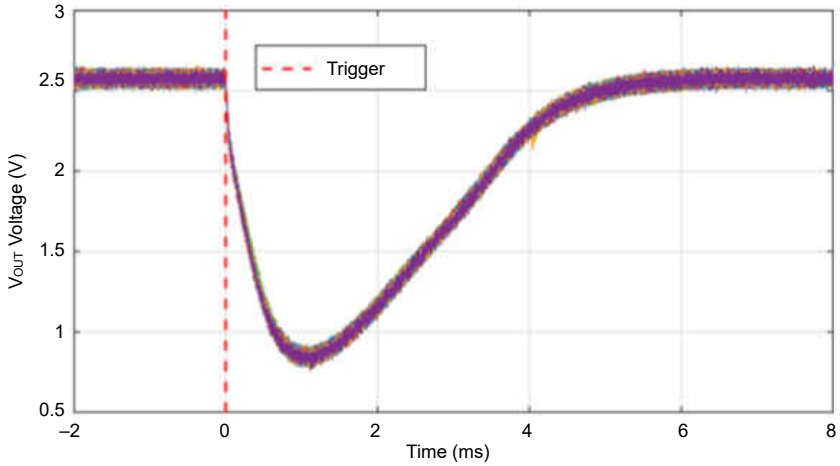

Figure 3. SEFI at LETeff = 86 MeV-cm^2/mg

Portfolio of Radiation-Hardened POL

To support the wide range of unique power rails that most FPGA payload designs require, the TPS7H4001-SP, a 3-V to 7-V input, 18-A DC/DC converter, has the capability to be paralleled to support up to 72 A of current. In addition, the TPS7H4002-SP, a 3-V to 5.5-V input, 3-A DC/DC converter, provides a compelling power density for the low current rails.

Increased Demand

Process nodes in semiconductor processes have decreased significantly, and supply voltages for digital cores are less than 1 V. Along with the increased processing capability in the digital cores, these changes translate to increased demand for supply currents and tight regulation requirements for power converters.

Such regulation requirements relate not only to the electrical performance of the POL converter but also to its performance under radiation effects. A radiation-sensitive DC/DC converter could have a serious impact on the downstream performance of a system and potentially damage the load. As such, proper SEE characterization of a DC/DC converter helps designers make the right POL converter choice based on event-rate calculations.

Resources

- Texas Instruments E2E™ Forums, *4 trends in space-grade power management in 2020*
- Texas Instruments E2E™ Forums, *Space-Enhanced Plastic gives designers a new solution for emerging low-earth-orbit commercial applications*
- Texas Instruments, *TI Space Products: Innovating your space solution with leading-edge Rad Hard (RHA) and QMLV products*

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265