User's Guide

28-V to 5-V, 10-A Flyback Converter Design With TPS7H5001-SP

Daniel Hartung *Space Power*

ABSTRACT

The flyback converter is a popular converter type used in satellites to take the 28-V bus to lower voltages such as 5-V. This design details how to use the TPS7H5001-SP controller to bring voltage down at up to 10 A of current both with and without synchronous rectification.

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Description

The TPS7H5001-SP controller brings the 28-V input down to a 5-V output at 10 A. The main converter was tested with synchronous rectification and efficiency was compared to the same converter without the synchronous rectification. Equations to find the values needed for the passives is reviewed along with the results from the 28-V rail. Passives are meant to reflect space-grade components, but may not have perfect analogs. The main transformer uses space-grade materials.

Features

- High efficiency using new radiation-hardened PWM controller
- Synchronous rectification using TPS7H5001-SP built-in outputs
- High-side current sensing using a current sense transformer
- Pulse-by-pulse current limiting with a current limit pin

Applications

- Command and data handling
- Satellite electric power system (EPS)
- Optical imaging payload
- Radar imaging payload
- Communications payload

1 System Overview

1.1 Block Diagram

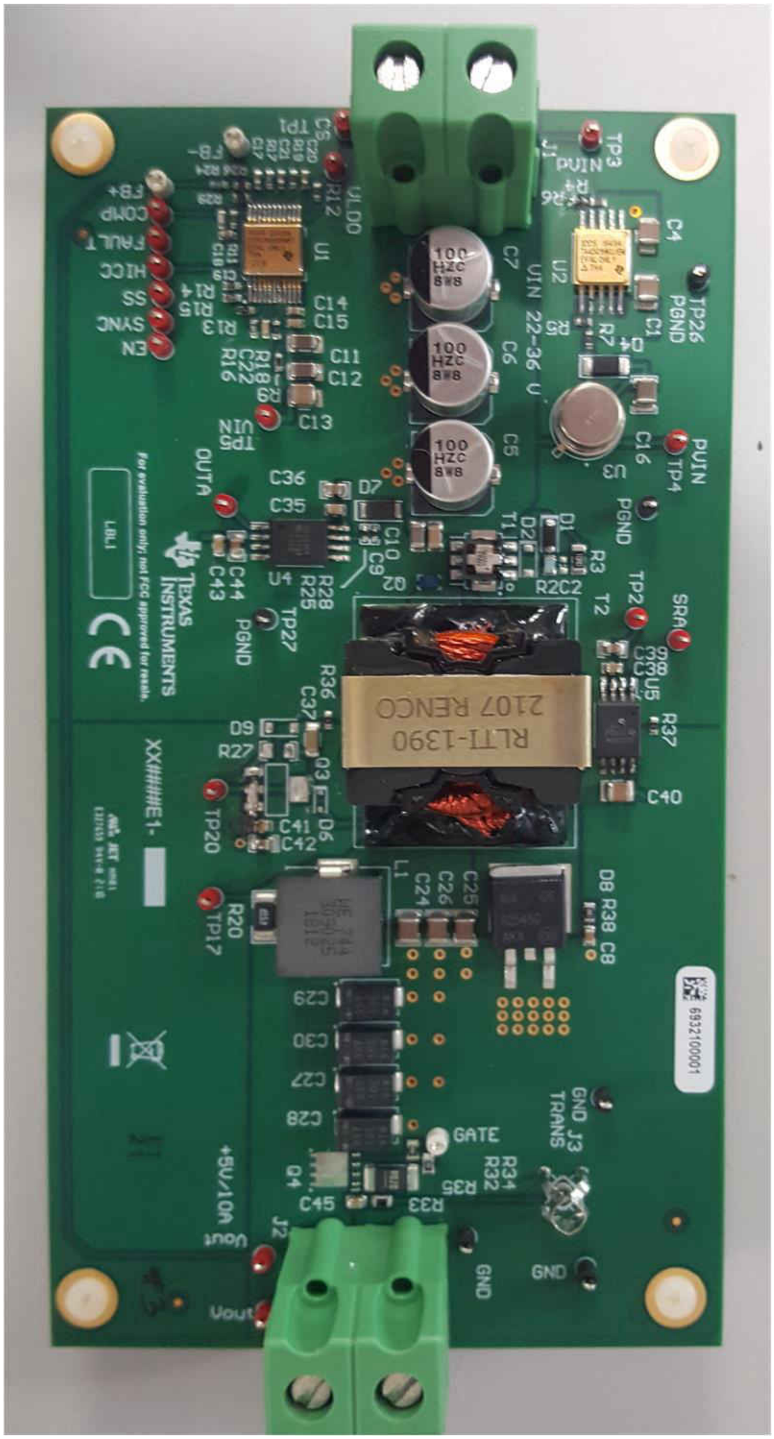

Figure 1-1. Design Board Picture

1.2 Design Considerations

The TPS7H5001-SP flyback board uses the TPS7H5001-SP and UCC5304 devices to create a synchronous buck converter to bring the 28-V battery voltage rail into a 5-V rail at 10 A for intermediate rails of space-grade power systems. The limiter of the output current in the design is the bottom-side GaN FET heat. Due to the roughly 150-mA peak current capability of the primary switching outputs of the TPS7H5001, the UCC5304 gate driver is used to amplify the current to provide the FETs of the synchronous buck with sufficient drive. These outputs are not dependent on the TPS7H5001-SP, and can be increased or decreased depending on the design. While isolated converters typically have isolated feedback incorporated into designs, this design capability is not focused on so the design of the other passives in the converter can be explained. Throughout the design process of the converter, equations were used to determine the starting values. Sometimes the value in an equation in this section does not exactly match what is shown in the schematic. Most of the time, this is due to rounding caused by values available in the lab.

1.3 System Design Theory

1.3.1 Switching Frequency

Choosing a switching frequency has a trade-off between efficiency, bandwidth, and size. Higher switching frequencies have larger bandwidth and a smaller size, but a lower efficiency than lower switching frequencies. A switching frequency of 500 kHz was chosen because space-grade materials for transformers can increase in size due to generated heat above this value. This makes it so the chosen frequency allows the converter to have as small of a magnetic field as possible. The timing resistor was then chosen to be 204 kΩ.

$$\mathrm{RT} = \frac{112{,}000}{f_{\mathrm{SW}}(\mathrm{kHz})} - 19.7 = \frac{112{,}000}{500\ \mathrm{kHz}} - 19.7 = 204.3\ \mathrm{k\Omega} \tag{1}$$

1.3.2 Transformer

The transformer of the design consists of two major values, turns ratio and primary side inductance. Equation 2 provides the turns ratio as a function of duty cycle. If the turns ratio is put in the maximum duty cycle of the converter, the calculations provide a maximum turns ratio. The TPS7H5001-SP design targeted a duty cycle of 33%. This allows for room in both directions for the duty cycle to change due to transients as well as keep it above the minimum on-time. Equation 2 and Equation 3 calculates the turns ratio of the transformer.

$$\mathrm{N_{ps}} = \frac{\mathrm{V_{in}} \times \mathrm{D}}{(\mathrm{V_{out}} + \mathrm{V_{Diode}}) \times (1 - \mathrm{D})} \tag{2}$$

$$\mathrm{N_{ps}} = \frac{28\ \mathrm{V} \times 0.33}{(5\ \mathrm{V} + 0.5\ \mathrm{V}) \times (1 - 0.33)} = 2.5 \tag{3}$$

Often the turns ratio slightly changes in the design due to how the transformer is manufactured. In this case, an axillary winding was planned, but not used. That factor plus the need to have a whole value of turns caused the turns ratio to be 8:3. Using a turns ratio of 3:1 is recommended, if the axillary winding is not needed, because while the duty cycle changes, there is less of a parasitic spike on the switch node since there are less turns on the primary side.

The primary inductance of the transformer is found from picking an appropriate ripple current. A higher inductance often means reduced current ripple, thus lower EMI and noise, but a higher inductance also increases physical size and limits the bandwidth of the design. A lower inductance does the opposite, increasing current ripple, lowering EMI, lowering noise, decreasing physical size, and increasing the limited bandwidth of the design. The percent ripple current can be anywhere from 20% to 80% depending on the design. Use Equation 4 and Equation 5 to find the primary inductance from the percentage ripple current.

$$\mathrm{L_{PRI}} = \frac{\mathrm{V_{in}}^2 \times \mathrm{D}^2}{\mathrm{V_{out}} \times \mathrm{I_{out}} \times \mathrm{f_{osc}} \times \%_{\mathrm{Ripple}}} \tag{4}$$

$$\frac{(28\ \mathrm{V})^2 \times 0.33^2}{5\ \mathrm{V} \times 10\ \mathrm{A} \times 500\ \mathrm{kHz} \times 0.4} = 8.54\ \mu\mathrm{H} \tag{5}$$

There are quite a few physical limitations when making transformers, so often this inductance changes slightly. For the TPS7H5001-SP design, us a primary inductance of μH. This corresponds to a percent ripple of around 0.38. The peak and primary currents of the transformer are also generally useful for figuring out the physical structure of the transformer, as listed in Equation 6 through Equation 13.

$$I_{Ripple} = \frac{V_{out} \times I_{out} \times \%_{Ripple}}{V_{in} \times D} \tag{6}$$

$$I_{Ripple} = \frac{5\ \ V \times 10\ \ A \times 0.38}{28\ \ V \times 0.33} = 2.06\ \ A \tag{7}$$

$$I_{PriPeak} = \frac{V_{out} \times I_{out}}{V_{in} \times D \times \eta} + \frac{I_{Ripple}}{2} \tag{8}$$

$$I_{PriPeak} = \frac{5\ \ V \times 10\ \ A}{28\ \ V \times 0.33 \times 0.8} + \frac{2.06}{2} = 7.79\ \ A \tag{9}$$

$$I_{PriRMS} = \sqrt{D \times \left(\frac{V_{out} \times I_{out}}{V_{in} \times D}\right)^2 + \frac{I_{Ripple}{}^2}{3}} \tag{10}$$

$$I_{PriRMS} = \sqrt{0.33 \times \left(\frac{5\ \ V \times 10\ \ A}{28\ \ V \times 0.33}\right)^2 + \frac{(2.06\ \ A)^2}{3}} = 3.33\ \ A \tag{11}$$

$$I_{SecRMS} = \sqrt{\left(1 - D\right) \times I_{out}{}^2 + \frac{\left(I_{Ripple} \times N_{ps}\right)^2}{3}} \tag{12}$$

$$I_{SecRMS} = \sqrt{0.67 \times \left(10\ \ A\right)^2 + \frac{(2.06\ \ A \times 2.67)^2}{3}} = 8.78\ \ A \tag{13}$$

1.3.3 RCD and Diode Clamp

Using a resistor and capacitor are commonly used for the clamp for flybacks, the design philosophy for how to pick resistor and capacitor values is covered. The resistor and capacitor is generally a value that is found through testing, but starting values can be obtained. To figure out the resistor and capacitor needed for the RCD clamp, first pick how much the node is allowed to overshoot. Use Equation 14 to find the voltage of the clamp.

$$V_{clamp} = K_{clamp} \times N_{ps} \times \left(V_{out} + V_{Diode}\right) \tag{14}$$

K_{clamp} is recommended to be 1.5, because this value allows for only around 50% overshoot. Knowing the parasitic inductance of the transformer and how much the snubber voltage is allowed to change over the switching cycle, allows the user to determine the starting values for the resistor and capacitor using Equation 15 and Equation 16.

$$R_{clamp} = \frac{V_{clamp}{}^2}{\frac{1}{2} \times L_{leakage} \times I_{PriPeak}{}^2 \times \frac{V_{clamp}}{V_{clamp} - N_{ps} \times \left(V_{out} + V_{Diode}\right)} \times f_{osc}} \tag{15}$$

$$C_{clamp} = \frac{V_{clamp}}{\Delta V_{clamp} \times V_{clamp} \times R_{clamp} \times f_{osc}} \tag{16}$$

A starting value of 10% is generally used for ΔV_{clamp}. Testing determined that a resistor value of 1 kΩ and a capacitor value 15 nF was required.

1.3.4 Output Diode and MOSFET

The voltage stress by the converter on the diode or MOSFET on the secondary side is found with Equation 17 and Equation 18.

$$V_{SecStress} = V_{out} + \frac{V_{in}}{N_{ps}} \tag{17}$$

$$V_{SecStress} = 5\ \ V + \frac{28\ \ V}{2.67} = 15V \tag{18}$$

Any diode selected needs a voltage rating of well above this value because it does not include parasitic spikes in the equation. The UC1843-SP diode was picked to have a voltage rating of 45 V.

1.3.5 Output Filter and Capacitance

For most designs, a ripple voltage is picked and the output capacitance is figured out from that value. The TPS7H5001-SP design started similar to that using Equation 19 through Equation 22.

$$C_{out} > \frac{I_{out} \times D}{V_{Ripple} \times f_{osc}} \tag{19}$$

$$C_{out} > \frac{10\ \ A \times 0.33}{50\ \ mV \times 500\ \ kHz} = 133\ \ \mu F \tag{20}$$

$$C_{out} > \frac{\Delta I_{step}}{2\pi \times \Delta V_{out} \times f_{co}} \tag{21}$$

$$C_{out} > \frac{10\ \ A}{2\pi \times 0.15\ \ V \times 10.0\ \ kHz} = 1\ \ mF \tag{22}$$

A value of around 1145 µF was chosen to keep output voltage ripple low. Note that the output voltage ripple in the design was further decreased by adding an output filter and by adding an inductor after a small portion of the output capacitance. Six ceramic capacitors were picked to be placed before the output filter and then the large tantalum capacitors with some small ceramics were added to be part of the output filter. The initial ceramics help with the initial current ripple, but have a very large output voltage ripple. This voltage ripple is attenuated by the inductor and capacitor combination placed between the ceramic capacitors and the output. Equation 23 through Equation 28 allow for finding the amount of attenuation that comes from a specific output filter inductance. An inductance of 500 nH was chosen to attenuate the output voltage ripple.

$$F_{resonant} = \frac{1}{2\pi \times \sqrt{L_{Filter} \times C_{oBulk}}} \tag{23}$$

$$F_{resonant} = \frac{1}{2\pi \times \sqrt{0.5\ \ nH \times 1127\ \ \mu F}} = 6.7\ \ kHz \tag{24}$$

$$F_{Zero} = \frac{1}{2\pi \times C_{oBulk} \times ESR_{oBulk}} \tag{25}$$

$$F_{Zero} = \frac{1}{2\pi \times 1127\ \ \mu F \times 0.009\ \ \Omega} = 15.69\ \ kHz \tag{26}$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{f_{osc}}{f_{resonant}}\right) - 20 \times \log_{10}\left(\frac{f_{osc}}{f_{zero}}\right) \tag{27}$$

$$Attenuation_{fsw} = 40 \times \log_{10}\left(\frac{200\ \ kHz}{6.7\ \ kHz}\right) - 20 \times \log_{10}\left(\frac{200\ \ kHz}{15.69\ \ kHz}\right) \quad = 36.88\ \ dB \tag{28}$$

Sometimes the output filter can cause peaking at high frequencies, this can be damped by adding a resistor in parallel with the inductor. For the UC1843A-SP design, 0.5 Ω was used as a very conservative value. Calculate the resistance needed to damp the peaking using Equation 29 through Equation 32.

$$\omega_o = \sqrt{\frac{2(C_{oCerm} + C_{oBulk})}{L_{Filter} \times C_{oCerm} \times C_{oBulk}}} \tag{29}$$

$$\omega_o = \sqrt{\frac{2(19\ \ \mu F + 1127\ \ \mu F)}{500\ \ nH \times 19\ \ \mu F \times 1127\ \ \mu F}} = 463\ \ kHz \tag{30}$$

$$R_{Filter} = \frac{R_o \times L_{Filter} \times \left(C_{oCerm} + C_{oBulk}\right) - \frac{L_{Filter}}{\omega_o}}{\frac{R_o \times (C_{oCerm} + C_{oBulk})}{\omega_o} - L_{Filter} \times C_{oCerm}} \tag{31}$$

$$R_{Filter} = \frac{0.5 \times 500\ \ nH \times \left(19\ \ \mu F + 1127\ \ \mu F\right) - \frac{500\ \ nH}{463\ \ kHz}}{\frac{0.5 \times (19\ \ \mu F + 1127\ \ \mu F)}{463\ \ kHz} - 500\ \ nH \times 19\ \ \mu F} = 0.232\ \ \Omega \tag{32}$$

1.3.6 Compensation

The poles and zeros of a flyback converter are calculated with Equation 33 through Equation 38.

$$f_{ZESR} = \frac{1 + D}{2\pi \times C_{out} \times R_{ESR}} \tag{33}$$

$$f_{ZESR} = \frac{1 + 0.33}{2\pi \times 1146\ \ \mu F \times 0.009\ \ \Omega} = 20.52\ \ kHz \tag{34}$$

$$f_P = \frac{1}{2\pi \times C_{out} \times R_o} \tag{35}$$

$$f_P = \frac{1}{2\pi \times 1146\ \ \mu F \times 0.5} = 278\ \ Hz \tag{36}$$

$$f_{RHPZ} = \frac{R_{out} \times (1 - D)^2}{2\pi \times \frac{L_{PRI}}{N_{ps}^2} \times D} \tag{37}$$

$$f_{RHPZ} = \frac{0.5 \times (1 - 0.33)^2}{2\pi \times \frac{9\ \ \mu H}{2.67^2} \times 0.33} = 86\ \ kHz \tag{38}$$

Type IIB compensation was selected to compensate the poles and zeros of the flyback converter. Since the right half-plane zero (RHPZ) of the flyback converter is unable to be compensated, the crossover frequency of the converter needs to be between one fourth to a whole decade below the RHPZ of the converter. Type IIB compensation has 1 pole and 1 zero to help compensate the converter. Place the pole from the compensation by the RHPZ of the converter and place the zero from compensation a decade before the expected crossover frequency. Using these guidelines, the compensation values for the converter were picked for the converter. For the non-isolated portion of the board this means choosing the value of the compensation resistors and capacitors along these guidelines. This allows for the gain to be controlled in the system without changing the poles and zeros of the system. Adding an isolated feedback loop often changes how the compensation is done. Optimization is needed for compensation values, and those values can be validated through testing.

1.3.7 Controller Passives

The sense resistor is used to sense the ripple current from the transformer as well as shutdown the switching cycle if the peak current of the converter is allowed to get too high. The voltage threshold of the CS pin is around 1 V and the gain of the current sense transformer is 100 due to the 1:100 turns ratio, thus the equation to find the sense resistor from the peak current is shown in Equation 39 and Equation 40.

$$R_{cs} = \frac{V_{CS\ Threshold} \times G_{CSTransformer}}{I_{limit}} \tag{39}$$

$$R_{cs} = \frac{1V \times 100V}{10A} = 10.0\Omega \tag{40}$$

I_{limit} needs to be greater than $I_{PriPeak}$.

The output voltage of the power converter is set by using a resister divider from the converter to the VSENSE pin. For a selected value of 10 kΩ, the value is found using Equation 41.

$$\text{Rbottom} = \frac{V_{ref}}{\text{Vout} - V_{ref}} \times \text{Rtop} = \frac{0.613\ \text{V}}{5\ \text{V} - 0.613\ \text{V}} \times 10\ \text{k}\Omega = 1.37\ \text{k}\Omega \quad (41)$$

The TPS7H5001-SP allows programming of two independent dead times. This allows for the dead times to be optimized to prevent shoot-through between the primary and synchronous switches while attaining the best possible converter efficiency. Use Equation 42 to determine the values of and for a desired dead time.

$$R_{PS} = R_{SP} = 1.207 \times \text{DT} - 8.858 = 1.207 \times 24\ \text{ns} - 8.858 = 20.11\ \text{k}\Omega \quad (42)$$

Using a capacitor between the soft start (SS) pin and AVSS, the soft start of the device is programmed. Equation 43 shows the calculation of the SS capacitor:

$$\text{Css} = \frac{t_{SS} \times I_{SS}}{V_{ref}} = \frac{7\ \text{ms} \times 2.7\ \mu\text{A}}{0.613\ \text{V}} = 30.8\ \text{nF} \quad (43)$$

Leading edge blank time is utilized to remove any transient noise from the current-sensing loop after the primary switching outputs, OUTA or OUTB, go high. The leading-edge blank time was selected to be 100 ns. Equation 44 shows the calculation to program the LEB resistor for a chosen LEB time.

$$R_{LEB} = 1.212 \times \text{LEB} - 9.484 = 1.212 \times 50\ \text{ns} - 9.484 = 51\ \text{k}\Omega \quad (44)$$

2 Test Results

2.1 Testing and Results

2.1.1 Test Setup

Table 2-1. Test Parameters

PARAMETER	SPECIFICATIONS
Input Power Supply	28 VDC
Output Voltage	5 VDC
Output Current	0 to 10 A
Operating Temperature	25°C
Switching Frequency of UC1843A-SP	200 kHz
Peak Input Current Limit	10 A
Bandwidth	About 10 kHz
Phase Margin	About 75°

2.1.2 Test Results

2.1.2.1 Efficiency

The efficiency measurement represented in Figure 2-1 was taken after the board was run for 20 minutes at full output load. The test setup for non-synchronous measurement was taken by disabling the GaNFETs used as nonsynchronous rectifiers. Both measurements were taken with the same board.

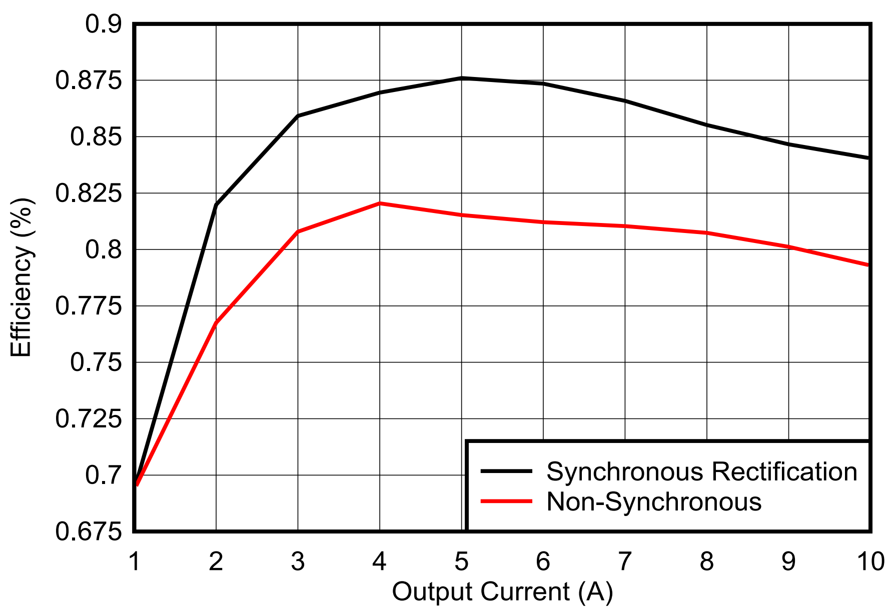

Figure 2-1. Efficiency vs Output Current

2.1.2.2 Frequency Response

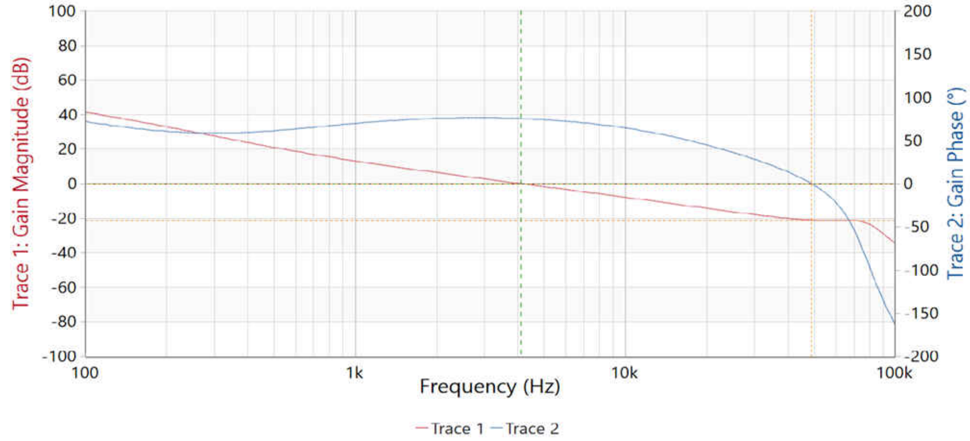

Figure 2-2. 28-V_{IN} Frequency Response

Frequency response was taken with 10-A output current.

Table 2-2. Frequency Response Characteristics

PARAMETER	VALUE
Crossover Frequency	4.12 kHz
Phase Margin	75.4°
Phase Crossover	49.1 kHz
Gain Margin	–21.0 dB

2.1.2.3 Thermal Characteristics

Thermal measurement was done with 28 V_{in} after 20 minutes of running with full load on the output. The hot spot on top side is GaNFET and the transformer. The hot spot on the bottom side is the resistors for the RCD clamp.

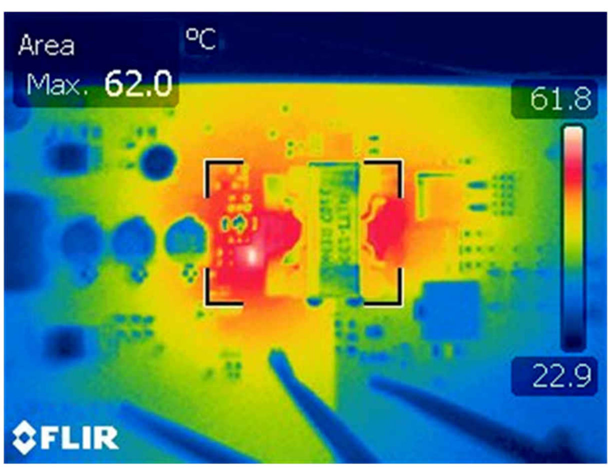

Figure 2-3. Top Board Thermal Characteristics for 28 V_{IN}

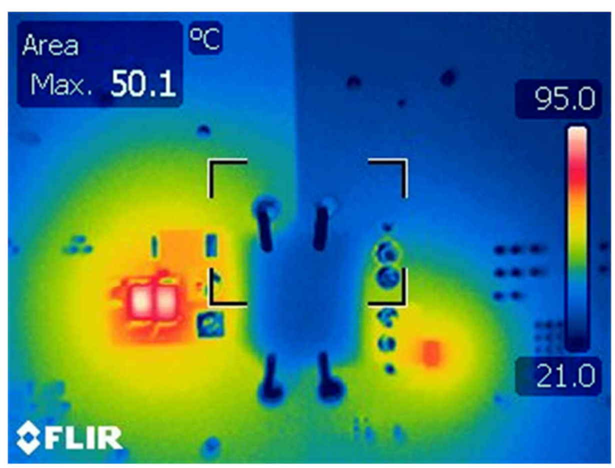

Figure 2-4. Bottom Board Thermal Characteristics for 28 V_{IN}

2.1.2.4 Output Voltage Ripple

Figure 2-5 shows the output voltage ripple waveform.

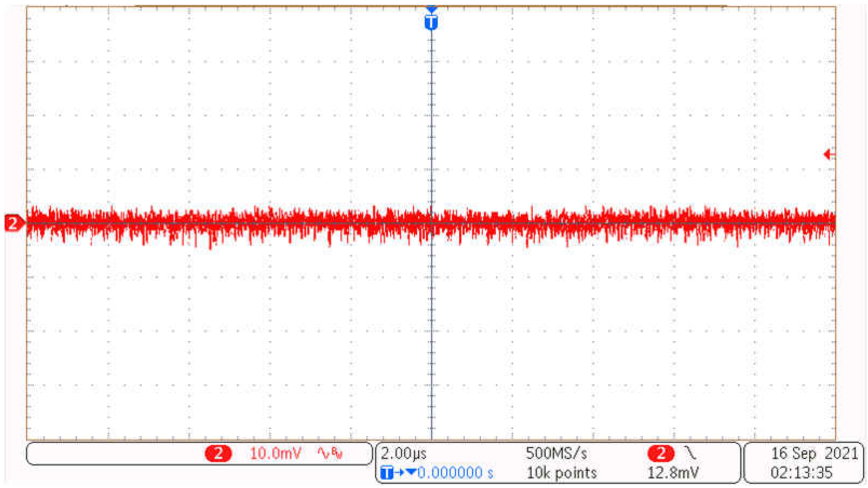

Figure 2-5. Output Voltage Ripple

2.1.2.5 Load Step

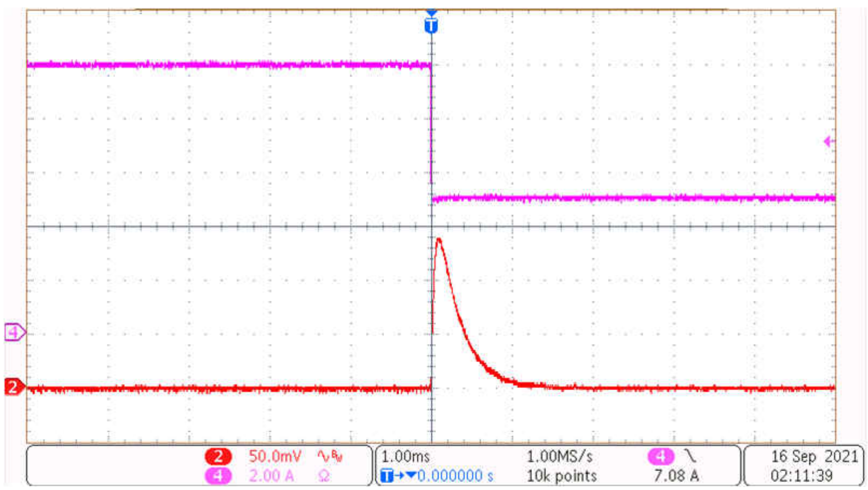

Figure 2-6. 10-A Load Step Down

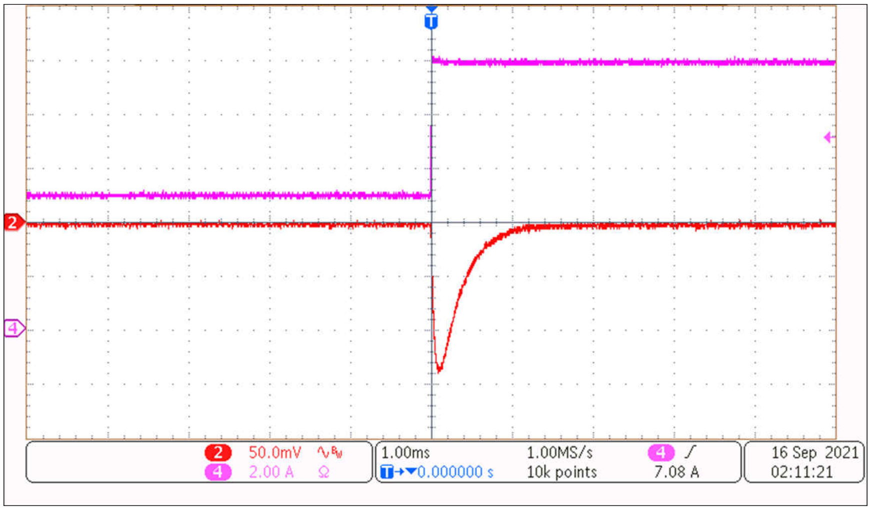

Figure 2-7. 10-A Load Step Up

2.1.2.6 Start-Up

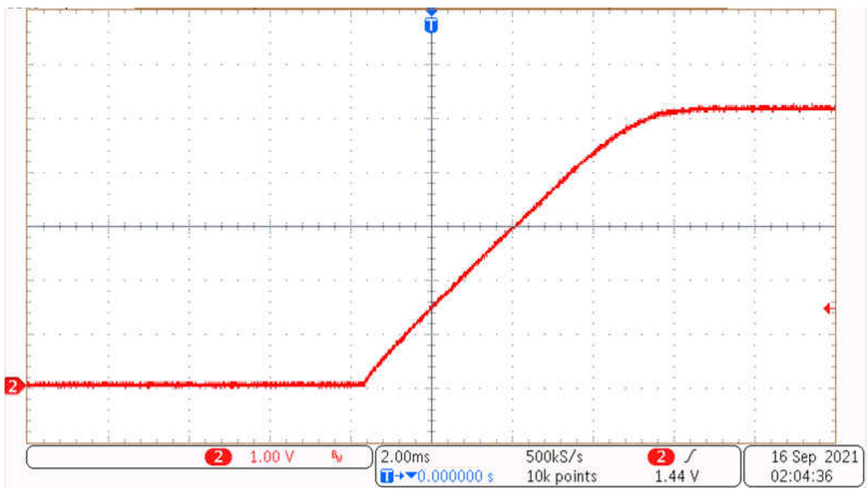

Figure 2-8. Start-Up With Fully Loaded Output

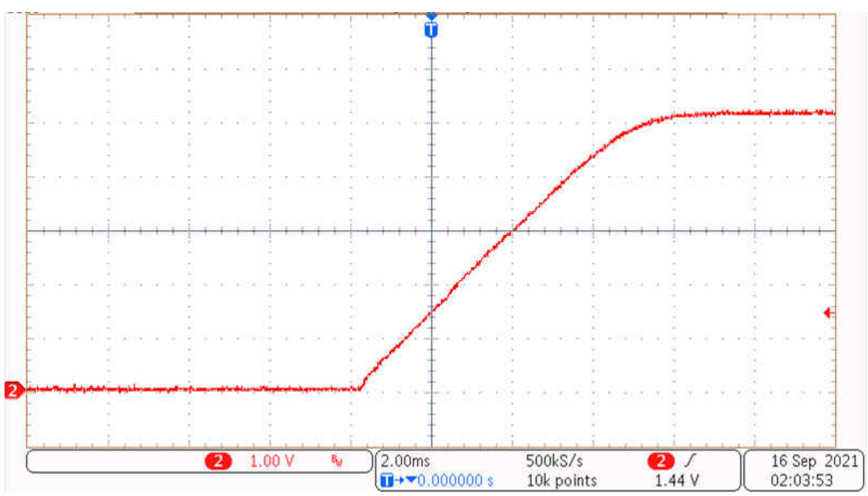

Figure 2-9. Start-Up With No Load on Output

2.1.2.7 Shutdown

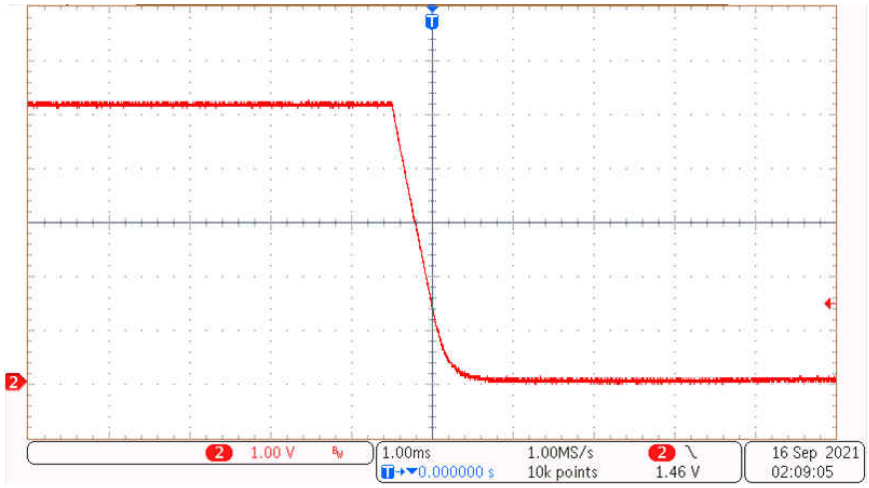

Figure 2-10. Shutdown With Fully Loaded Output

2.1.2.8 Component Stresses

For the test in Figure 2-11 and Figure 2-12, 28 V was applied to the input and 10 A was drawn from the output. For the output FET and diode stress, the voltage was measured with respect to ground so the output voltage must be added to show the true stress on the output diode.

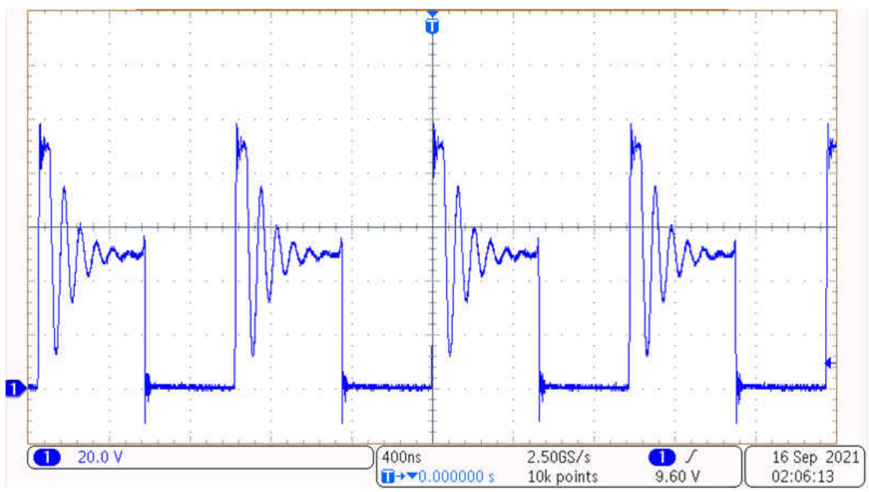

Figure 2-11. Voltage Stress on Main Switching MOSFET

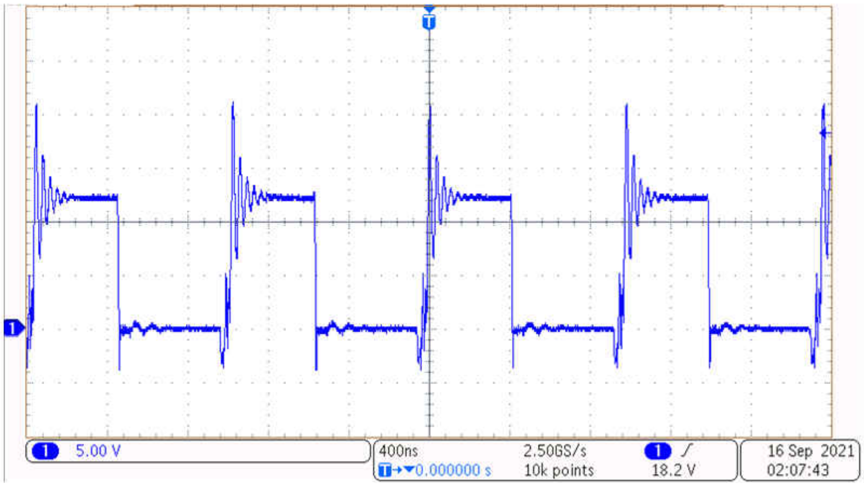

Figure 2-12. Output FET and Diode Stress

3 Design Files

3.1 Schematics

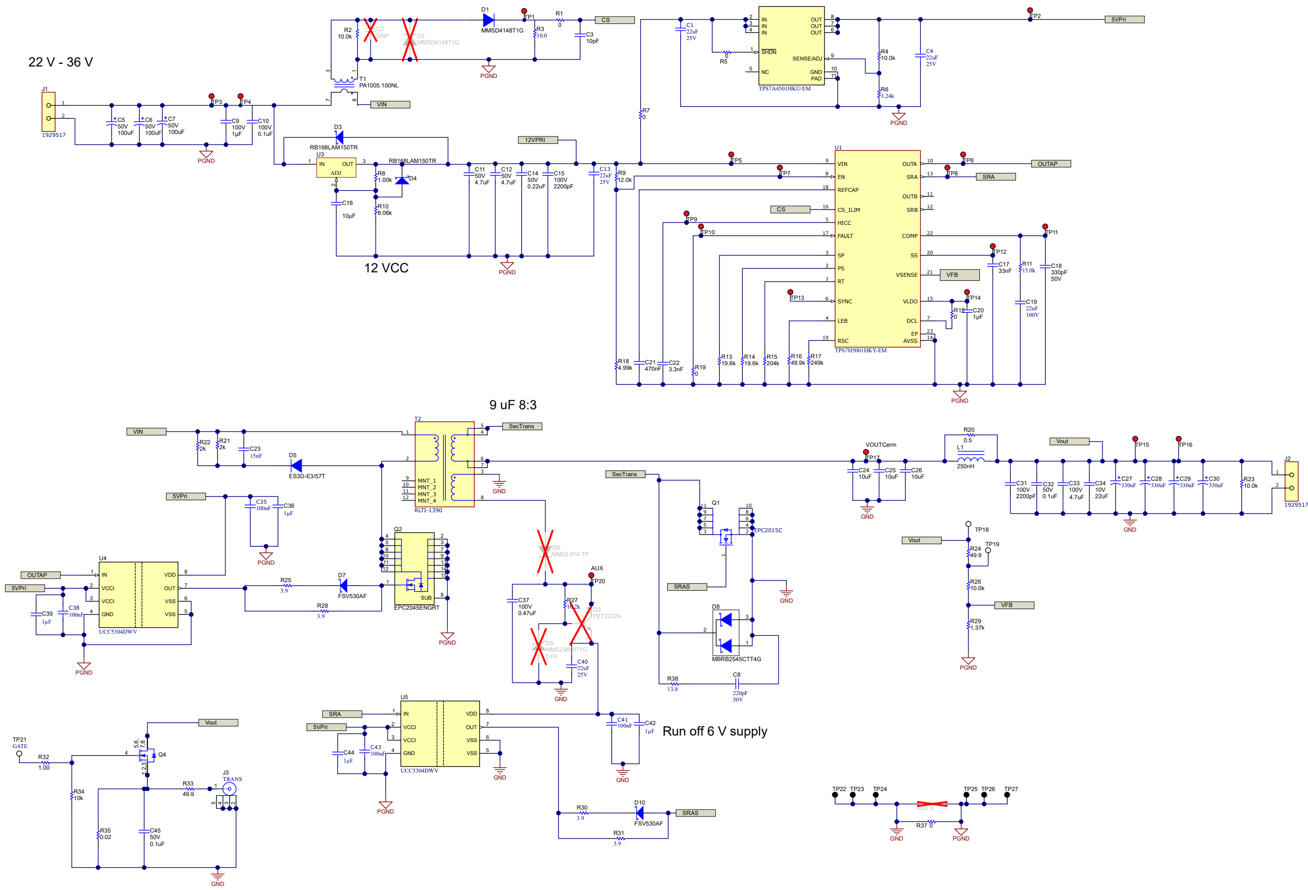

Figure 3-1. Main Schematic

3.2 Bill of Materials

Designator	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		XX####	Any
C1, C4, C13, C40	4	22 µF	22 µF ±20% 25-V Ceramic Capacitor X7R 1210 (3225 Metric)	1210	GRM32ER71E226ME15K	Murata
C3	1	10 pF	CAP, CERM, 10 pF, 10 V, ±10%, X7R, 0603	0603	0603ZC100KAT2A	AVX
C5, C6, C7	3	100 µF	CAP, Polymer Hybrid, 100 uF, 50 V, ±20%, 28 ohm, 10x10 SMD	10x10	EEHZC1H101P	Panasonic
C8	1	220 pF	CAP, CERM, 220 pF, 50 V, ±10%, X7R, 0805	0805	C0805C221K5RACTU	Kemet
C9	1	1 µF	CAP, CERM, 1 µF, 100 V,±10%, X7R, 1206	1206	CC1206KKX7R0BB105	Yageo America
C10	1	0.1 µF	CAP, CERM, 0.1 µF, 100 V, ±10%, X7R, 1206	1206	12061C104KAT2A	AVX
C11, C12	2		4.7 µF ±10% 50-V Ceramic Capacitor X7R 1206 (3216 Metric)	1206	885012208094	Wurth Electronics
C14	1	0.22 µF	CAP, CERM, 0.22 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E3X7R1H224K080AB	TDK
C15	1	2200 pF	CAP, CERM, 2200 pF, 100 V, ±5%, X7R, 0603	0603	06031C222JAT2A	AVX
C16	1	10 µF	CAP, CERM, 10 µF, 63 V,±20%, X7R, 1210	1210	GRM32ER71J106MA12L	MuRata
C17	1	0.033 µF	CAP, CERM, 0.033 µF, 25 V, ±5%, X7R, 0603	0603	C0603C333J3RACTU	Kemet
C18	1	330 pF	CAP, CERM, 330 pF, 50 V, ±10%, X7R, 0603	0603	C0603C331K5RACTU	Kemet
C19	1	0.022 µF	CAP, CERM, 0.022 µF, 100 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E2X7R2A223K080AA	TDK
C20	1	1 µF	CAP, CERM, 1 µF, 25 V,±10%, X7R, AEC-Q200 Grade 1, 0603	0603	CGA3E1X7R1E105K080AD	TDK
C21	1	0.47 µF	CAP, CERM, 0.47 µF, 50 V, ±10%, X7R, 0603	0603	C1608X7R1H474K080AC	TDK
C22	1	3300 pF	CAP, CERM, 3300 pF, 100 V, ±5%, X7R, 0603	0603	06031C332JAT2A	AVX
C23	1	330 pF	CAP, CERM, 330 pF, 630 V, ±5%, C0G/NP0, 1206	1206	GRM31A5C2J331JW01D	MuRata
C24, C25, C26	3	10 µF	CAP, CERM, 10 µF, 50 V, ±10%, X7R, 1210	1210	GRM32ER71H106KA12L	MuRata
C27, C28, C29, C30	4	330 µF	CAP, Tantalum Polymer, 330 µF, 10 V, ±20%, 0.006 ohm, 7343-43 SMD	7343-43	T530X337M010ATE006	Kemet
C31	1	2200 pF	CAP, CERM, 2200 pF, 100 V, ±10%, X7R, 0805	0805	08051C222KAT2A	AVX
C32	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 1210	1210	C1210C104K5RACTU	Kemet
C33	1	4.7 µF	CAP, CERM, 4.7 µF, 100 V, ±10%, X7S, AEC-Q200 Grade 1, 1210	1210	CGA6M3X7S2A475K200AB	TDK
C34	1	22 µF	CAP, CERM, 22 µF, 10 V, ±10%, X7R, 1210	1210	GRM32ER71A226ME20L	MuRata
C35, C38, C41, C43	4		0.1 µF ±10% 50 V Ceramic Capacitor X7R 0805 (2012 Metric)	0805	GCE21BR71H104KA01L	Murata
C36, C39, C42, C44	4	1 µF	CAP, CERM, 1 µF, 50 V,±10%, X7R, 0805	0805	GJ821BR71H105KA12L	MuRata

Designator	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C37	1	0.47 µF	CAP, CERM, 0.47 µF, 100 V, ±10%, X7R, 1206	1206	C3216X7R2A474K160AA	TDK
C45	1	0.1 µF	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0805	0805	C0805C104K5RACTU	Kemet
D1	1	100 V	Diode, Switching, 100 V, 0.2 A, SOD-123	SOD-123	MMSD4148T1G	ON Semiconductor
D3, D4	2	150 V	Diode, Schottky, 150 V, 1 A, SOD-128	SOD-128	RB168LAM150TR	Rohm
D5	1	200 V	Diode, Ultrafast, 200 V, 3 A, SMC	SMC	ES3D-E3/57T	Vishay-Semiconductor
D6	1	100 V	Diode, Switching, 100 V, 0.2 A, SOD-323	SOD-323	MMDL914-TP	Micro Commercial Components
D7, D10	2	30 V	Diode, Schottky, 30 V, 5 A, AEC-Q101, SMAF	SMAF	FSV530AF	Fairchild Semiconductor
D8	1	45 V	Diode, Schottky, 45 V, 30 A, DDPAK	DDPAK	MBRB2545CTT4G	ON Semiconductor
D9	1	5.6V	Diode, Zener, 5.6 V, 500 mW, SOD-123	SOD-123	MMSZ4690T1G	ON Semiconductor
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 × 1/4, Nylon, Philips pan head	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2	2		Fixed Terminal Blocks MKDSP 10 HV/ 2-10	HDR2	1929517	Phoenix Contact
J3	1		Compact Probe Tip Circuit Board Test Points, TH, 25 per	TH Scope Probe	131-5031-00	Tektronix
L1	1	250 nH	Inductor, Shielded Drum Core, Ferrite, 250 nH, 50 A, 0.000165 ohm, SMD	12.5x13mm	744309025	Wurth Elektronik
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
Q1	1		N-Channel 40 V 53 A (T_A) Surface Mount Die	POWER_MOSFET_N_CH_4 MM105_1MM635	EPC2015C	EPC
Q2	1	100 V	MOSFET, N-CH, 100 V, 16 A, 2.5 × 1.5 mm	2.5 × 1.5 mm	EPC2045ENGRT	EPC
Q3	1	40 V	Transistor, NPN, 40 V, 1 A, SOT-223	SOT-223	PZT2222A	Fairchild Semiconductor
Q4	1	25 V	MOSFET, N-CH, 25 V, 113 A, DQH0008A (VSON-CLIP-8)	DQH0008A	CSD16408Q5	Texas Instruments
R1, R5, R7, R12, R19, R36, R37	7	0	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R2	1	10.0 k	RES, 10.0 k, 1%, 0.2 W, 0805	0805	MCU08050C1002FP500	Vishay/Beyschlag
R3	1	10.0	RES, 10.0, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW120610R0FKEA	Vishay-Dale
R4, R13, R14, R23, R26	5	10.0k	RES, 10.0 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD0710KL	Yageo America
R6	1	3.24k	RES, 3.24 k, 1%, 0.1 W, 0603	0603	RC0603FR-073K24L	Yageo
R8	1	1.00k	RES, 1.00 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1001V	Panasonic
R9	1	12.0k	RES, 12.0 k, 1%, 0.1 W, 0603	0603	RC0603FR-0712KL	Yageo
R10	1	8.06k	RES, 8.06 k, 1%, 0.1 W, 0603	0603	RC0603FR-078K06L	Yageo

Designator	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R11	1	15.0k	RES, 15.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060315K0FKEA	Vishay-Dale
R15	1	90.9k	RES, 90.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0790K9L	Yageo
R16	1	49.9k	RES, 49.9 k, 1%, 0.1 W, 0603	0603	RC0603FR-0749K9L	Yageo
R17	1	249k	RES, 249 k, 1%, 0.1 W, 0603	0603	RC0603FR-07249KL	Yageo
R18	1	4.99k	RES, 4.99 k, 1%, 0.1 W, 0603	0603	RC0603FR-074K99L	Yageo
R20	1	0.5	RES, 0.5, 1%, 1 W, 2010	2010	CSRN2010FKR500	Stackpole Electronics Inc
R21, R22	2	100k	RES, 100 k, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	CRCW2512100KFKEG	Vishay-Dale
R24	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	RC0603FR-0749R9L	Yageo America
R25, R28, R30, R31	4	3.9	RES, 3.9, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023R90JNED	Vishay-Dale
R27	1	10.2k	RES, 10.2 k, 1%, 0.25 W, AEC-Q200 Grade 0, 1206	1206	CRCW120610K2FKEA	Vishay-Dale
R29	1	1.37k	RES, 1.37 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K37L	Yageo
R32	1	1.00	RES, 1.00, 1%, 0.125 W, 0805	0805	RC0805FR-071RL	Yageo America
R33	1	49.9	RES, 49.9, 0.1%, 0.125 W, 0805	0805	RT0805BRD0749R9L	Yageo America
R34	1	10k	RES, 10 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080510K0JNEA	Vishay-Dale
R35	1	0.02	RES, 0.02, 1%, 1 W, AEC-Q200 Grade 0, 2512	2512	LRMAM2512-R02FT4	TT Electronics/IRC
R38	1	13.0	RES, 13.0, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805	CRCW080513R0FKEA	Vishay-Dale
T1	1		SMT Current Sense Tranformer	P82xx	PA1005.100NL	Pulse Engineering
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP20	18		Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP18, TP19, TP21	3		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP22, TP23, TP24, TP25, TP26, TP27	6		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U2	1		Wide Vin Low-Dropout Voltage Regulator, HKU0010A (CFP-10)	HKU0010A	TPS7A4501HKU/EM	Texas Instruments
U3	1		3-Terminal Adjustable Regulator, 3-pin TO-39	NDT0003A		Texas Instruments
U4, U5	2		4-A/6-A, Single-Channel Reinforced Isolation Gate Driver with High Noise Immunity, DWV0008A (SOIC-8)	DWV0008A	UCC5304DWV	Texas Instruments

Designator	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C2	0	0.01 µF	CAP, CERM, 0.01 µF, 50 V,±10%, X7R, 0603	0603	885012206089	Wurth Elektronik
D2	0	100 V	Diode, Switching, 100 V, 0.2 A, SOD-123	SOD-123	MMSD4148T1G	ON Semiconductor
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
T2	0		Flyback Transformer, Pri 9.3 mΩ, Sec 21/1.64 mΩ, 500VAC	PTH_XFRMR_1IN30_1IN15	RLTI-1390	Renco Electronics
U1	0		Radiation-Hardness-Assured Si and GaN Dual Output Controller	CFP22	TPS7H5001HKY-EM	Texas Instruments

3.3 Assembly Drawings

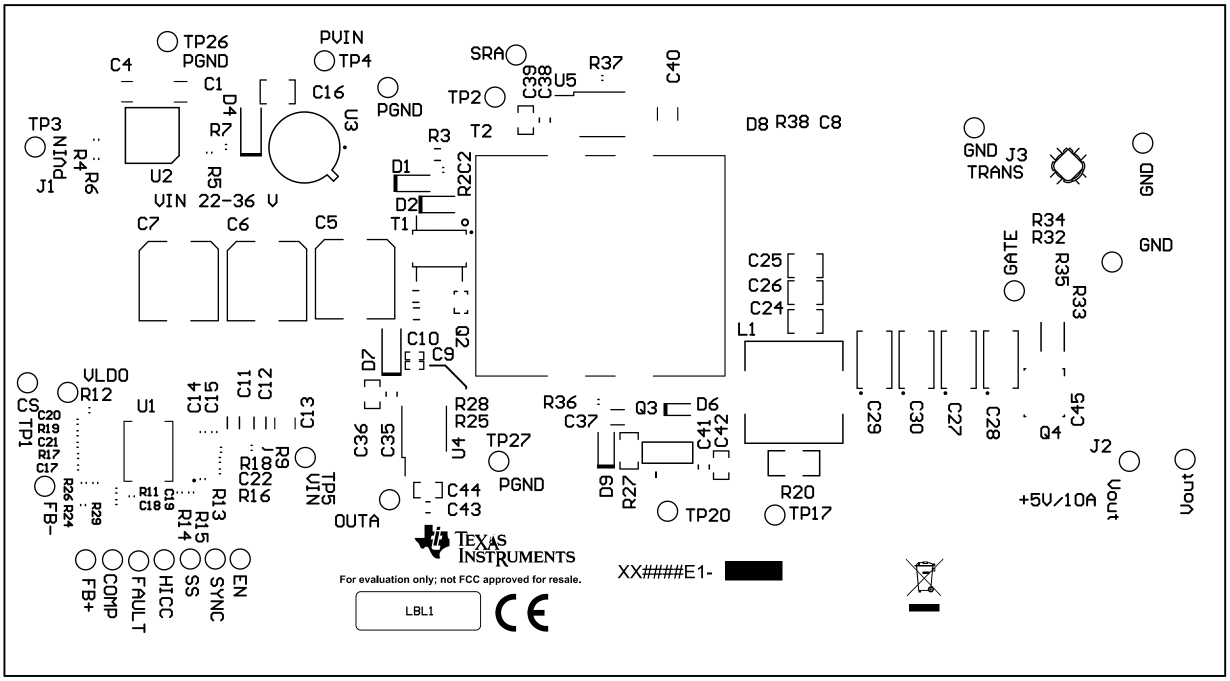

Figure 3-2. Top Overlay

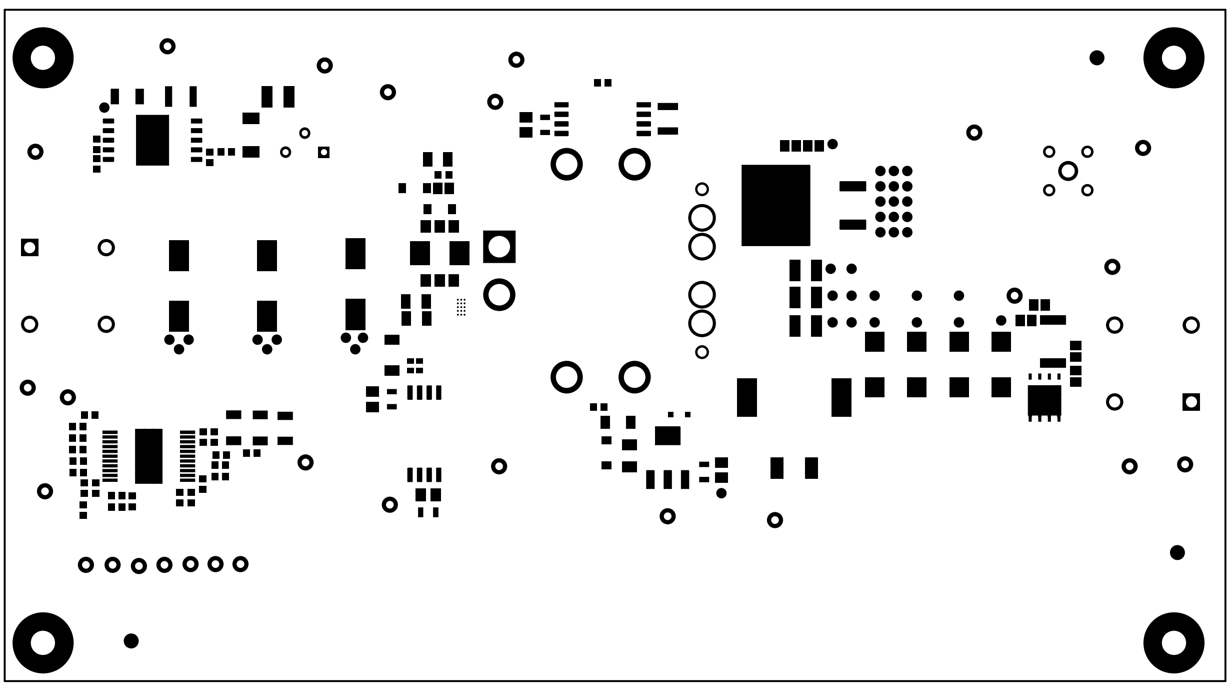

Figure 3-3. Top Solder

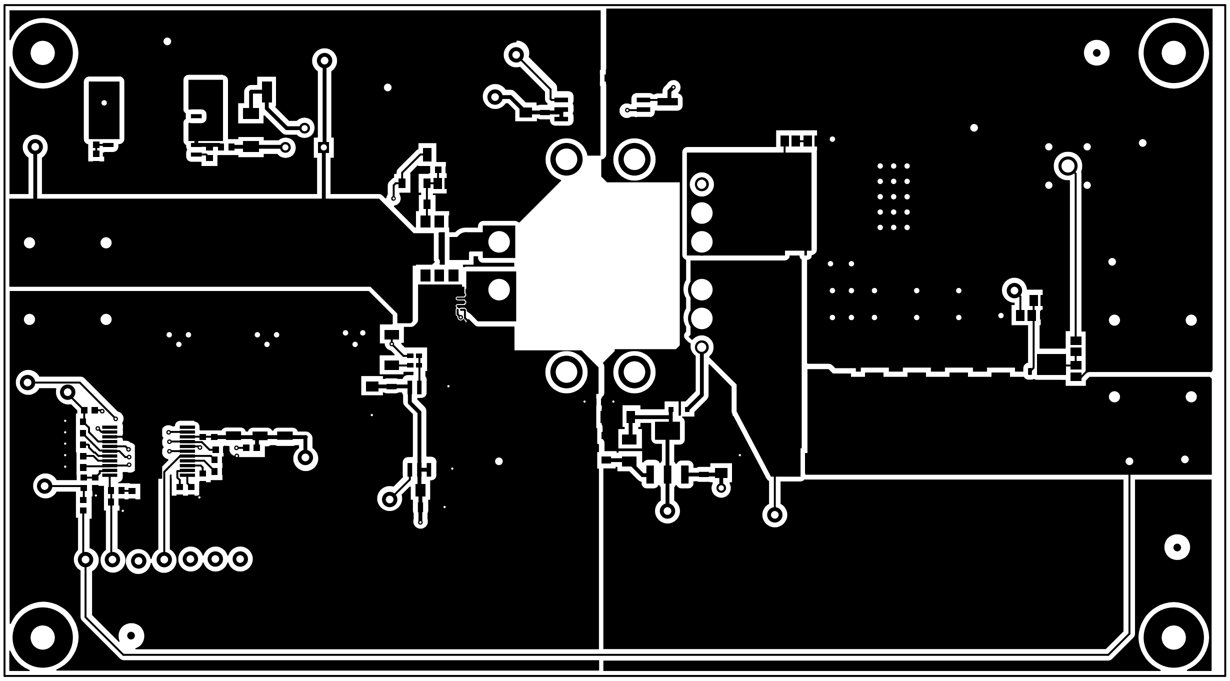

Figure 3-4. Top Layer

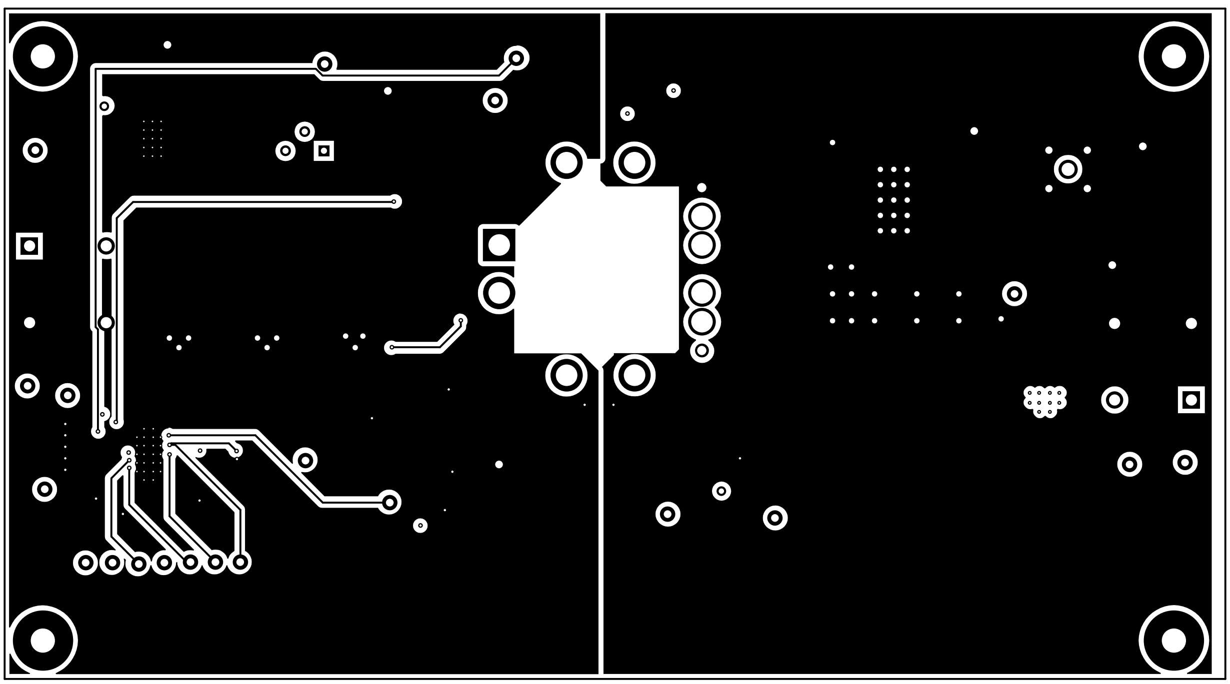

Figure 3-5. Signal Layer One

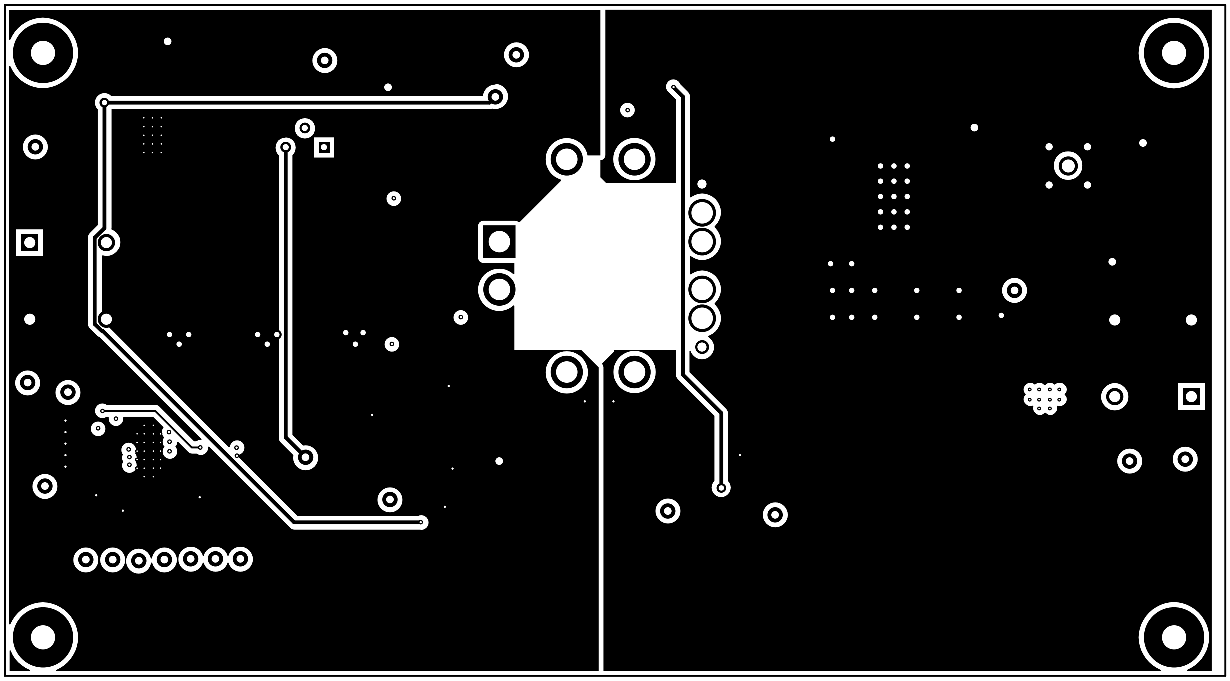

Figure 3-6. Signal Layer Two

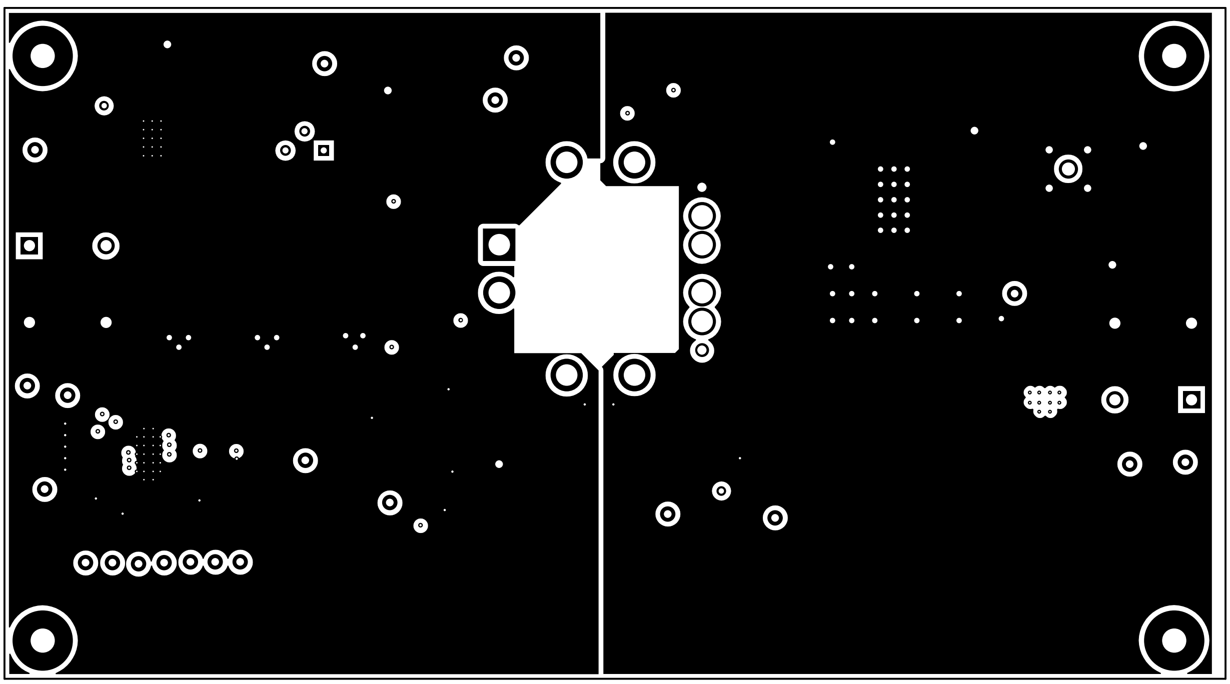

Figure 3-7. Signal Layer Three

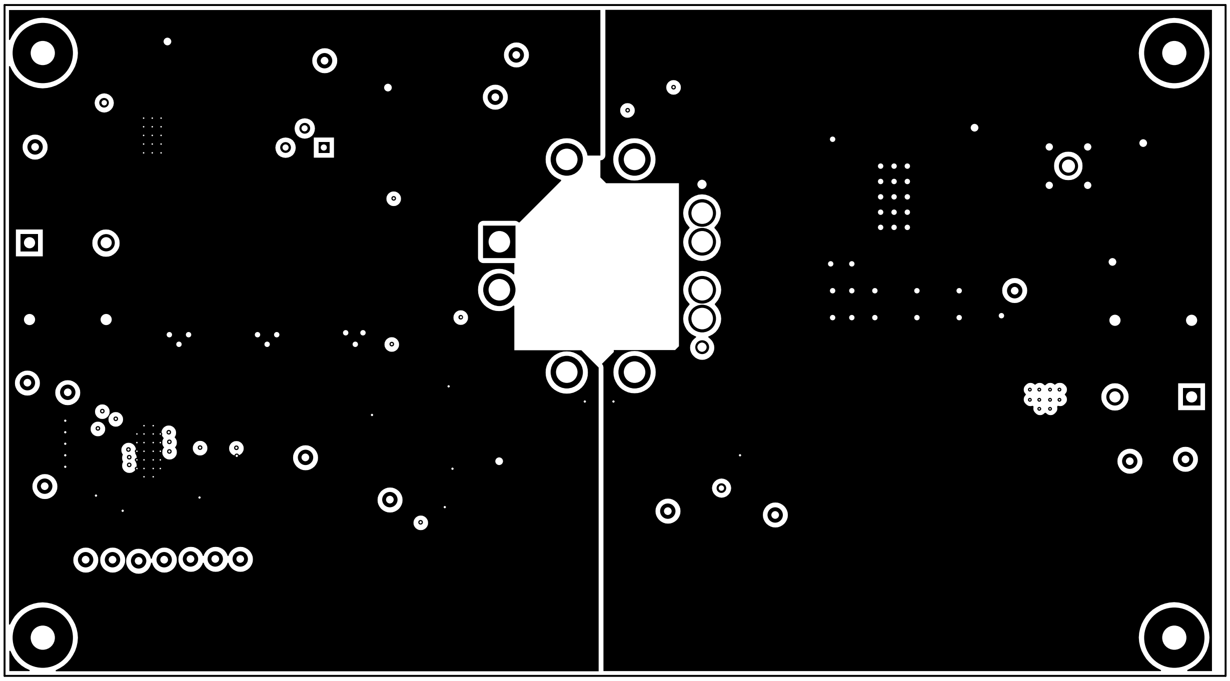

Figure 3-8. Signal Layer Four

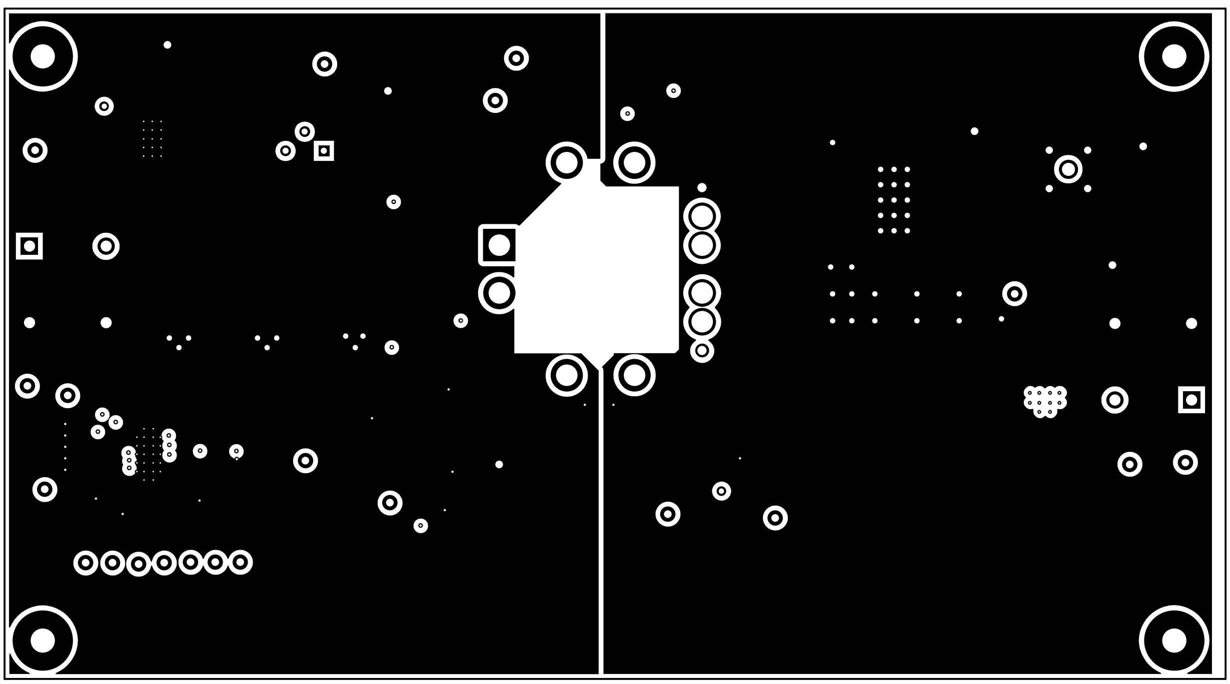

Figure 3-9. Signal Layer Five

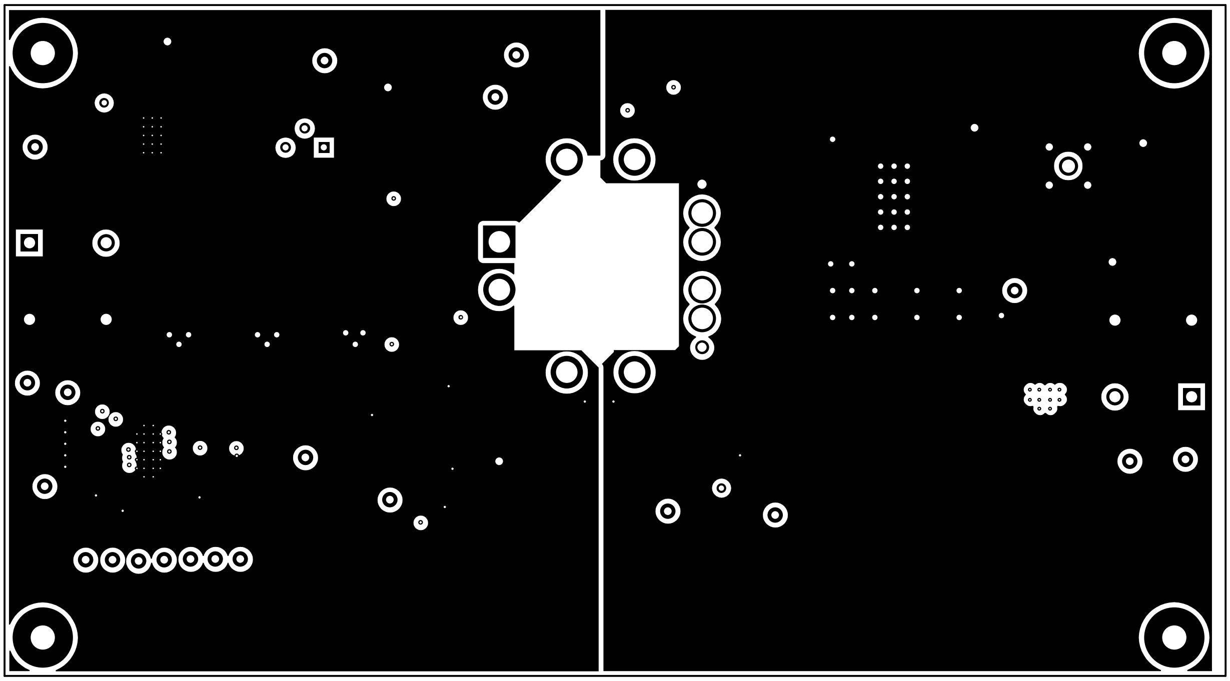

Figure 3-10. Signal Layer Six

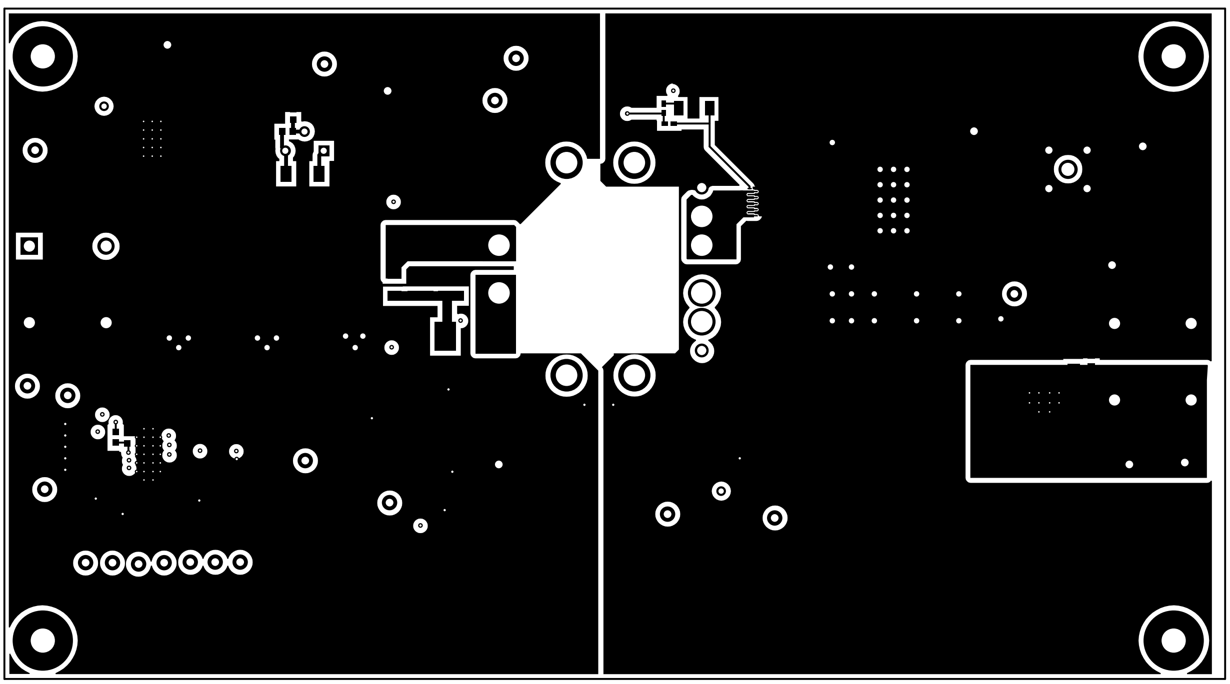

Figure 3-11. Bottom Layer

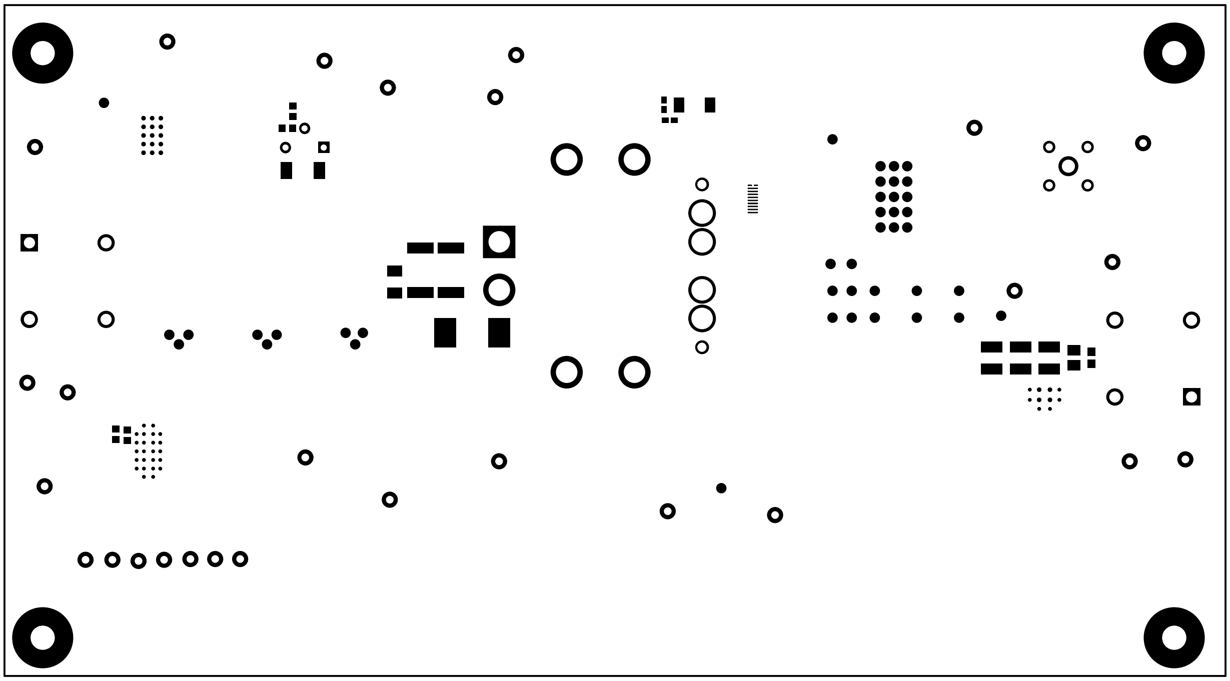

Figure 3-12. Bottom Solder

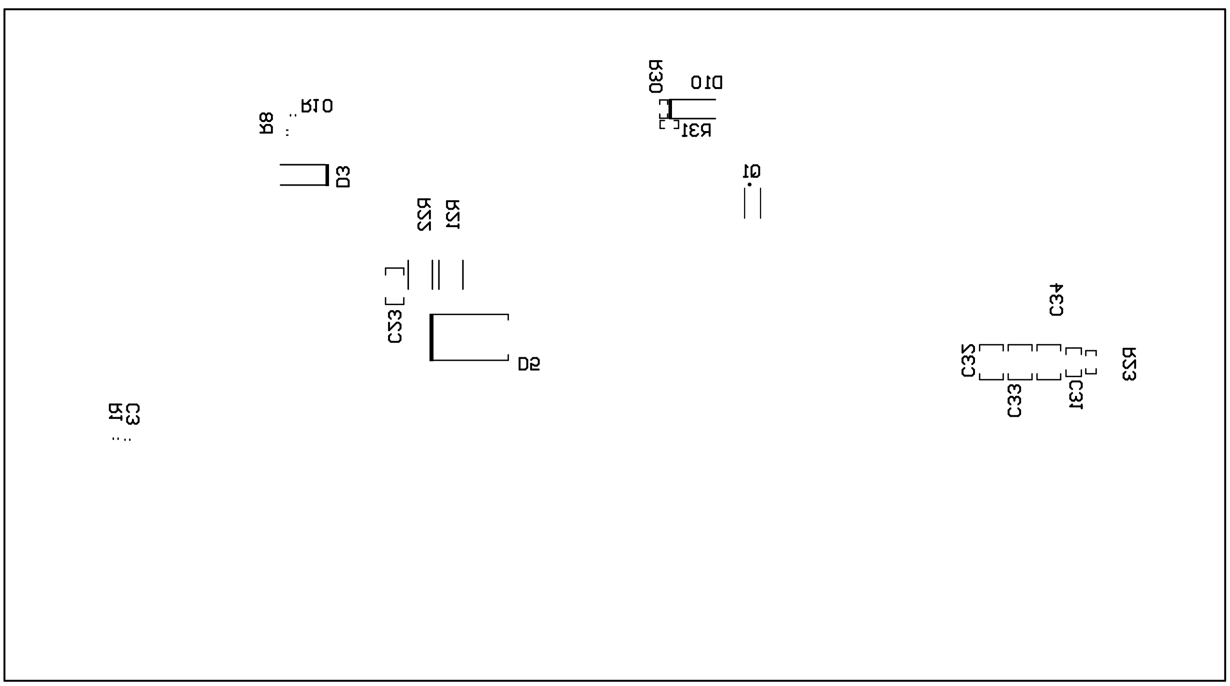

Figure 3-13. Bottom Solder

3.3 Assembly Drawings

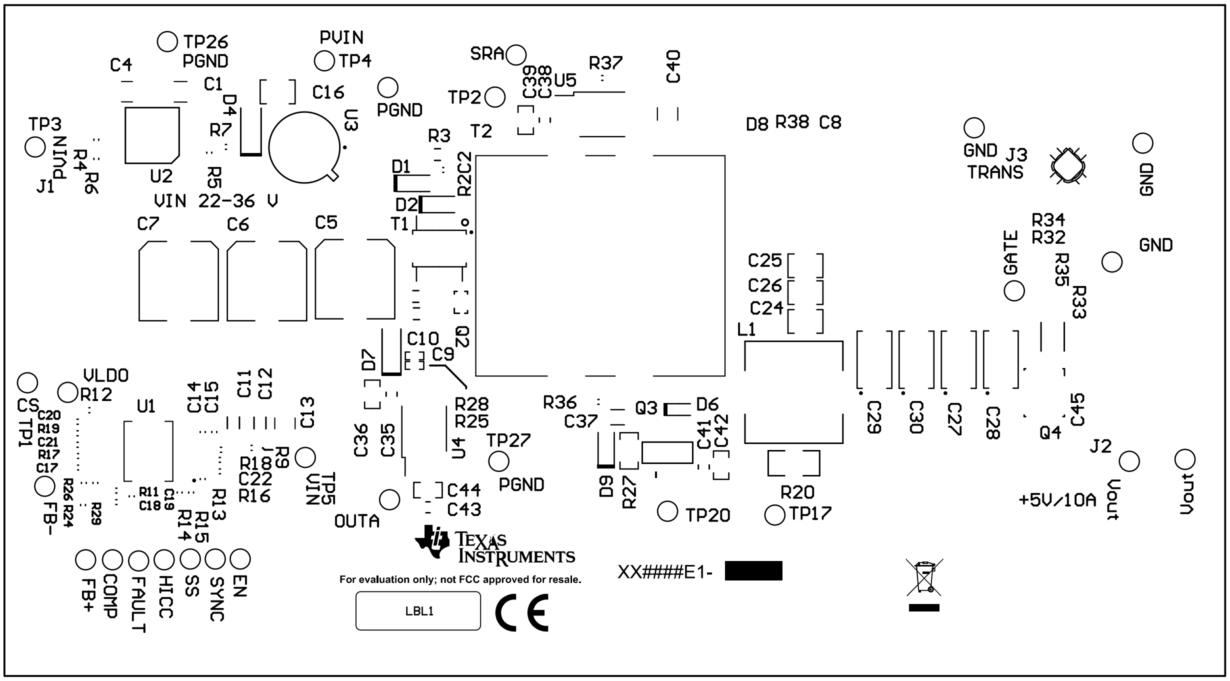

Figure 3-2. Top Overlay

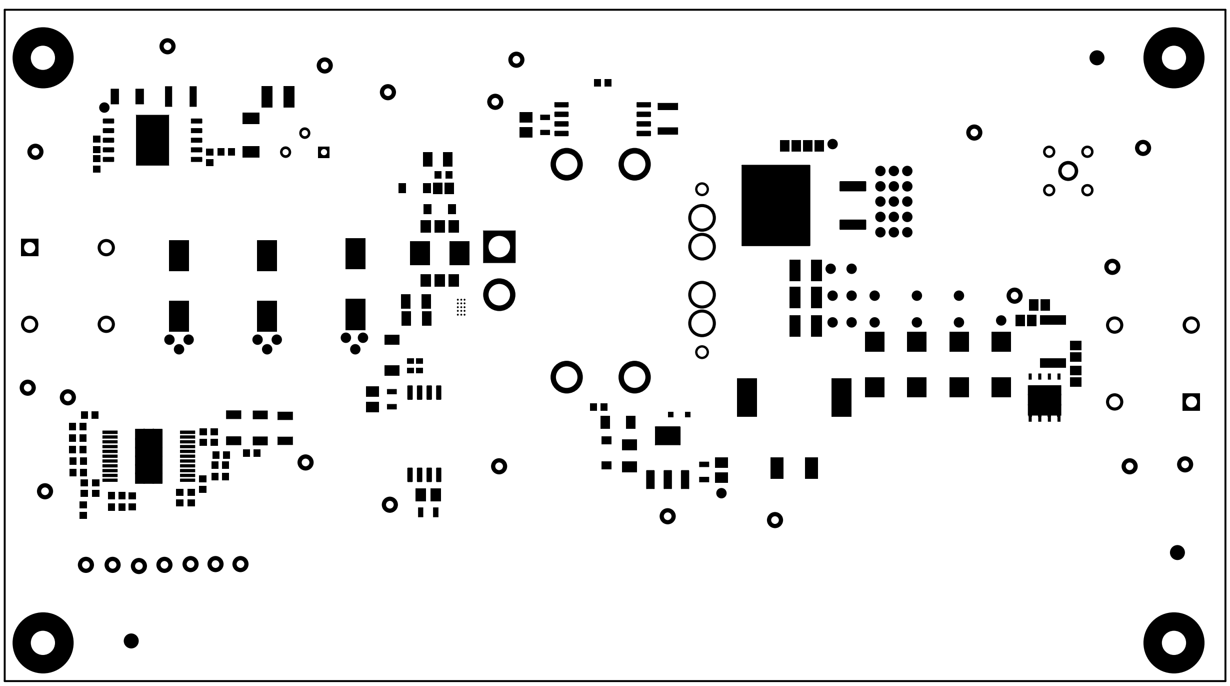

Figure 3-3. Top Solder

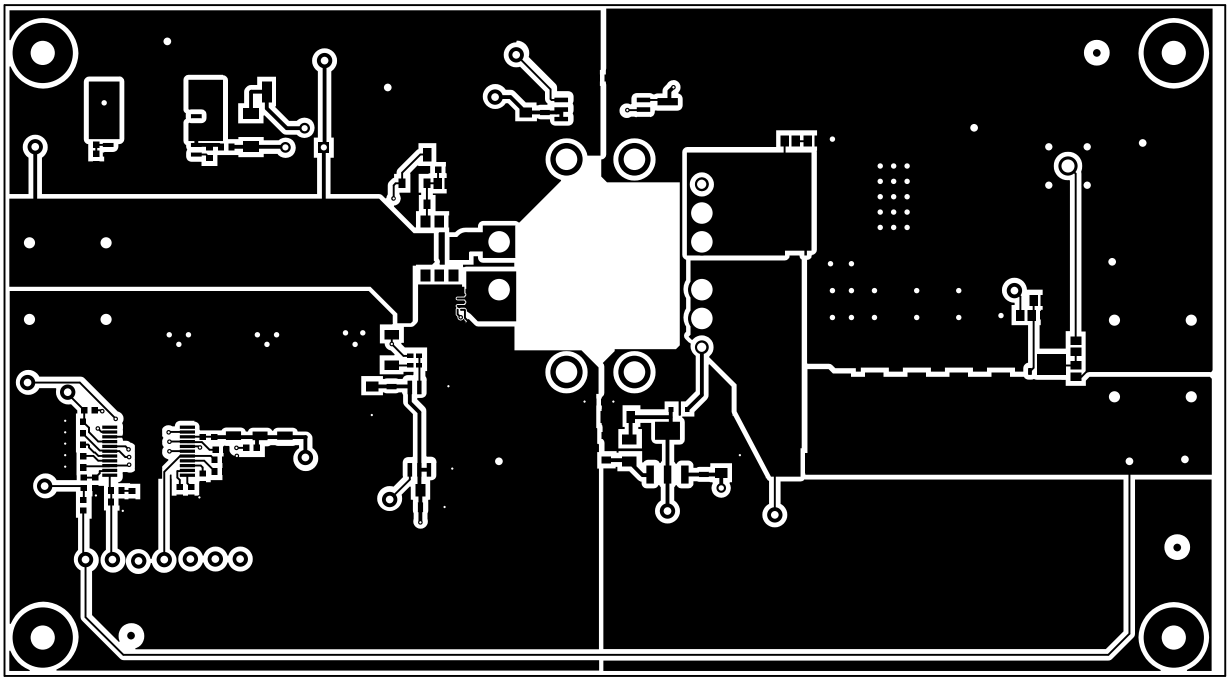

Figure 3-4. Top Layer

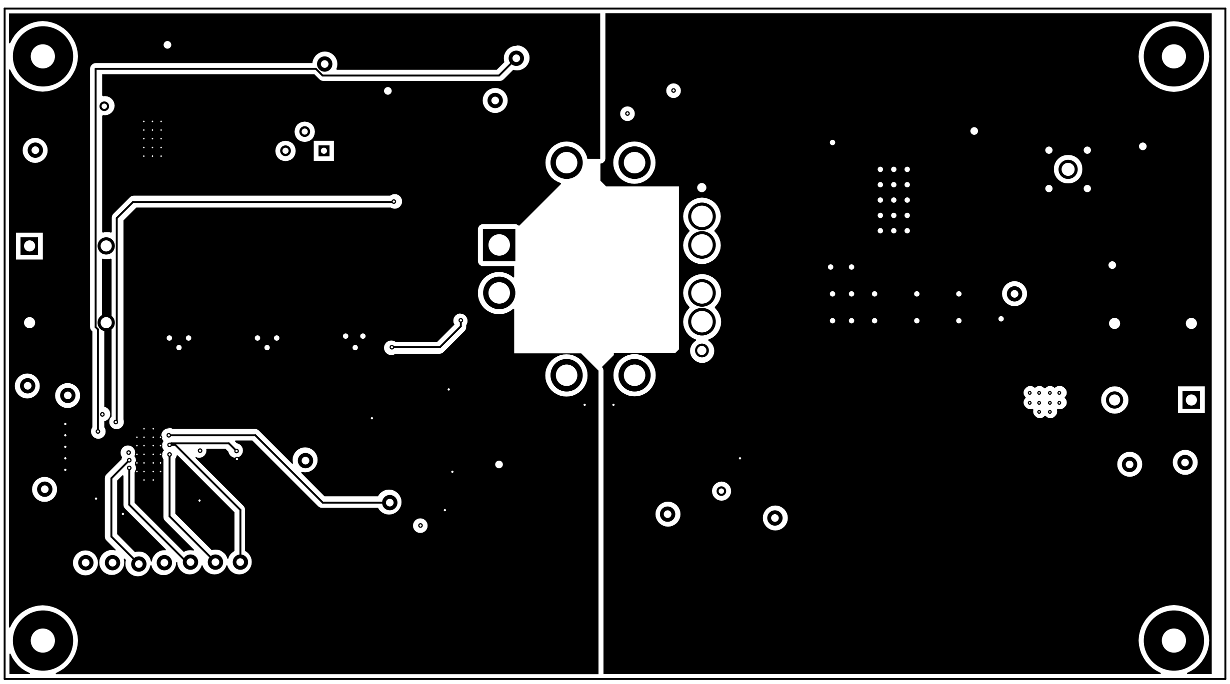

Figure 3-5. Signal Layer One

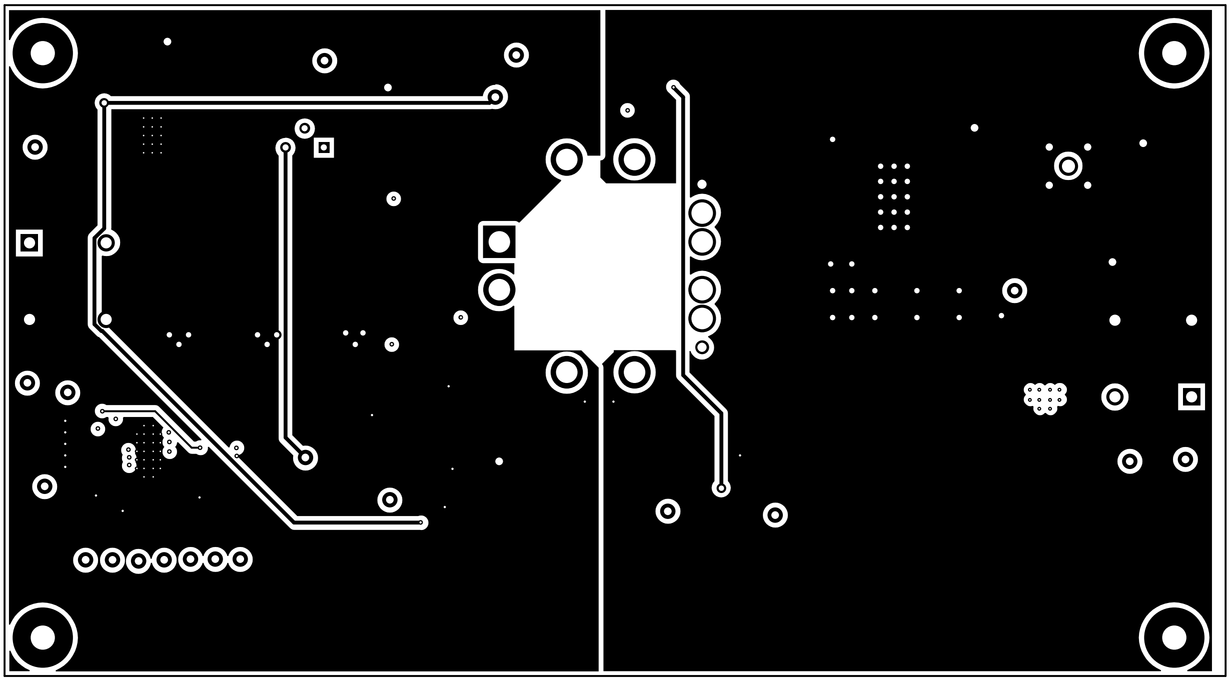

Figure 3-6. Signal Layer Two

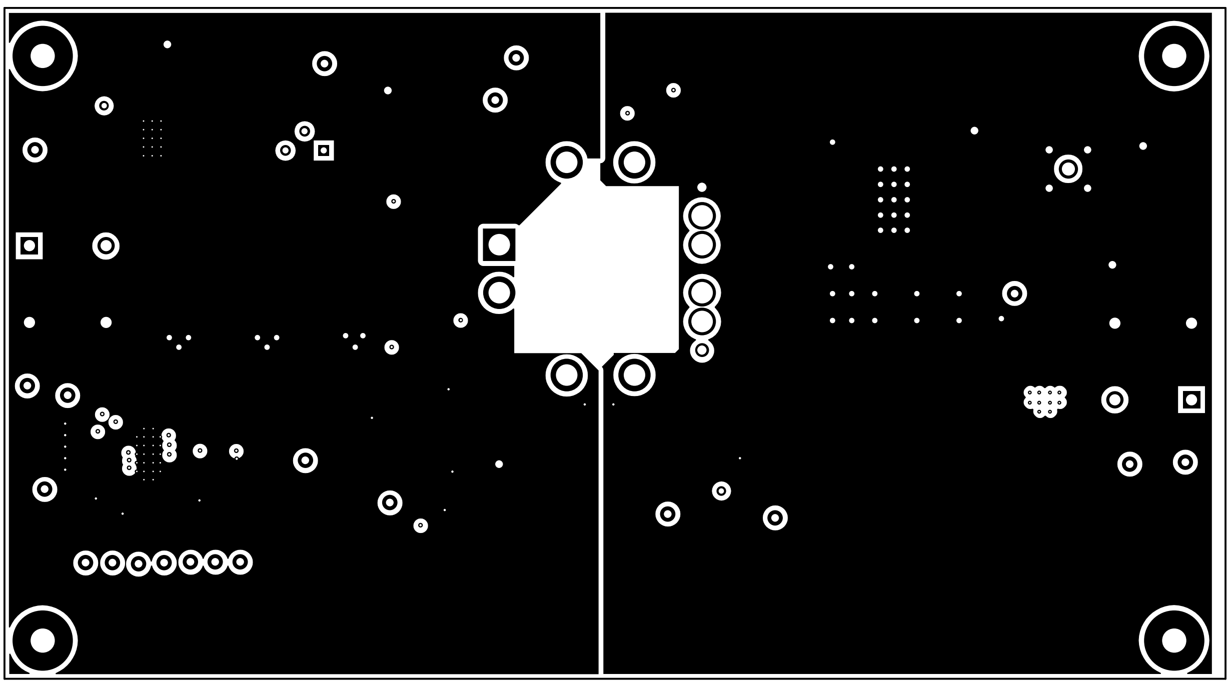

Figure 3-7. Signal Layer Three

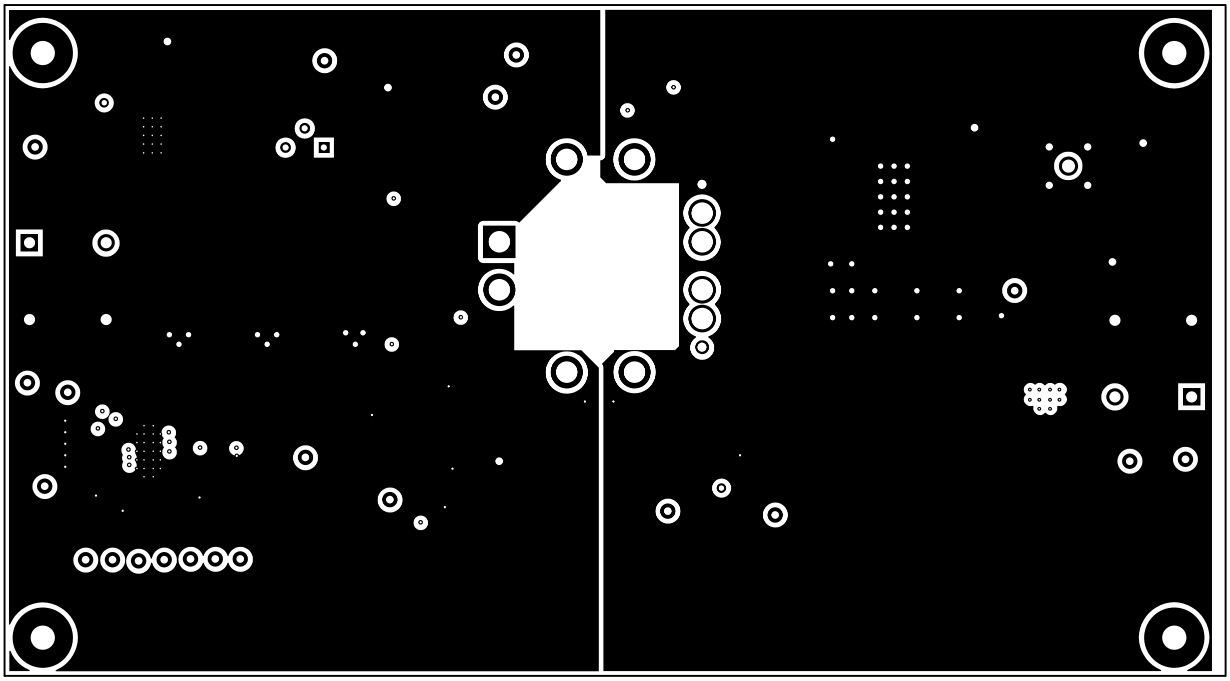

Figure 3-8. Signal Layer Four

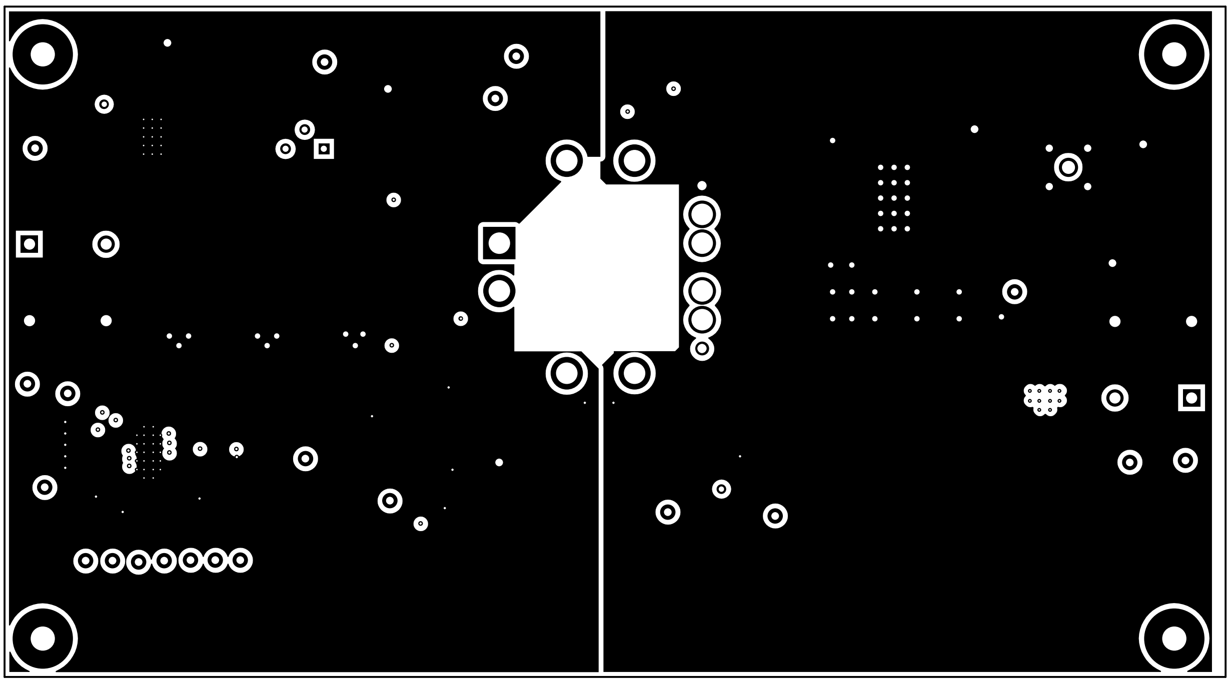

Figure 3-9. Signal Layer Five

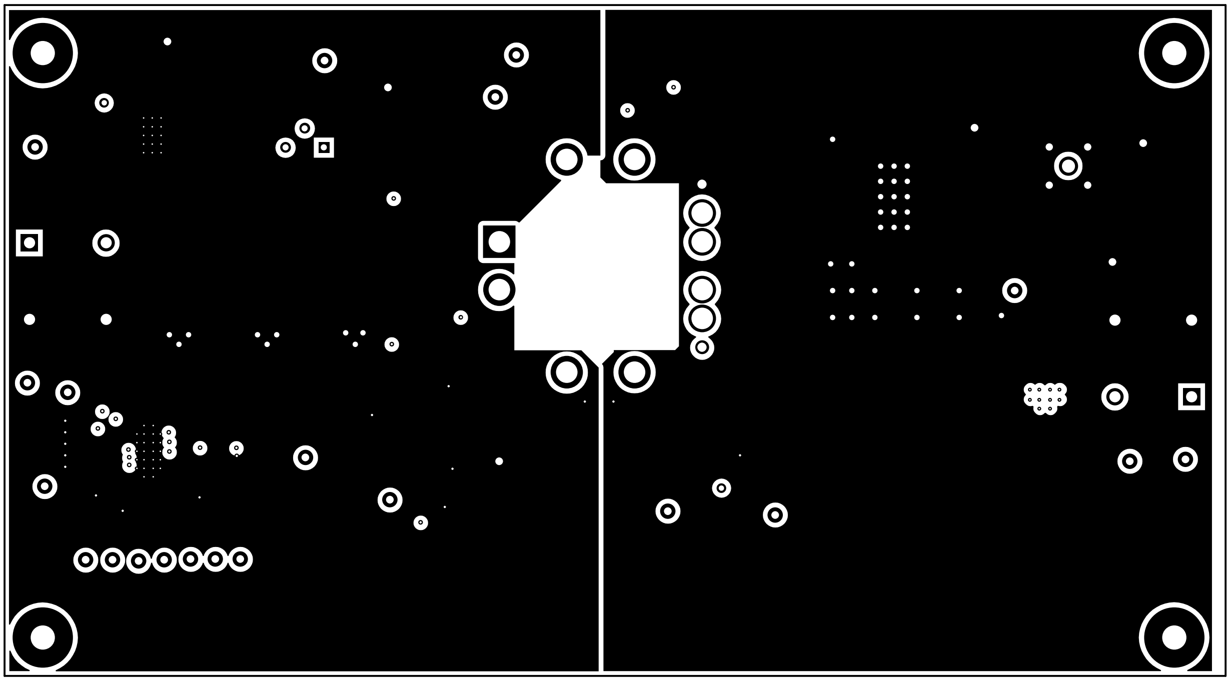

Figure 3-10. Signal Layer Six

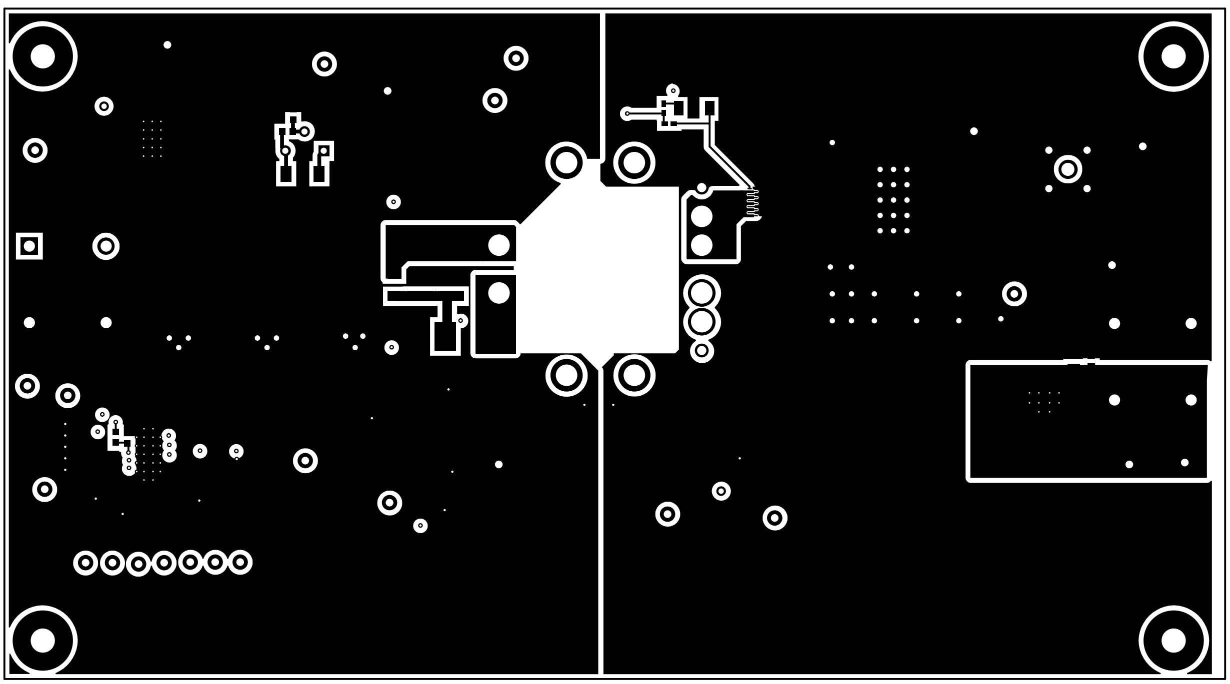

Figure 3-11. Bottom Layer

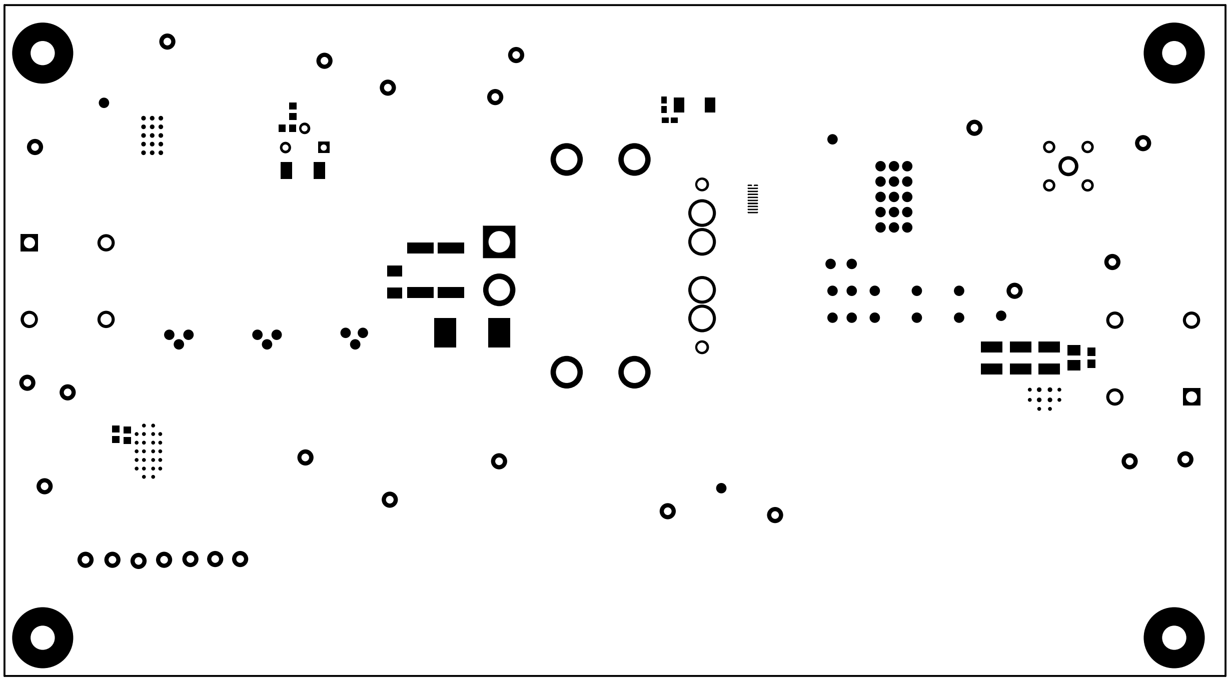

Figure 3-12. Bottom Solder

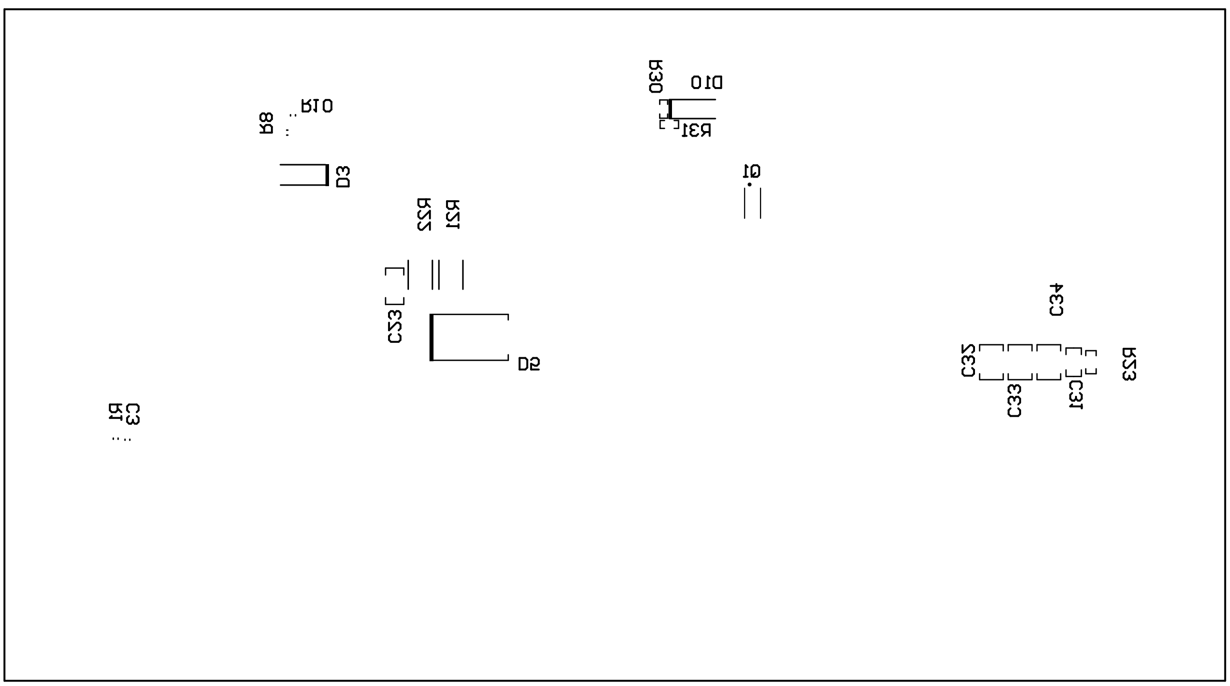

Figure 3-13. Bottom Solder

4 Related Documentation

1. Texas Instruments, *Using The DRV3204EVM To Evaluate The DRV3203-Q1 data sheet*