Application Report

System Design Considerations for High-Power Motor Driver Applications

Cole Macias *Brushless DC*

ABSTRACT

Motor applications that sustain higher power ratings introduce design considerations that are not required in lower power applications. By looking at the anatomy of the power stage we can develop troubleshooting guidelines, a library of external circuits, TI driver product features, or layout techniques to combat the volatile nature of higher power systems.

Table of Contents

List of Figures

1 Introduction to High-Power Motor Applications

High power motor applications can range anywhere from lower voltage systems that result in hundreds of watts, such as a 12-V automotive power seats, to multiple kilowatt systems, such as 60-V and 100-A power tools. Typically, these systems use shunt-based current sensing, and non-isolated gate drivers that control large power MOSFETs. While these applications can be powered from a battery or gridded AC power converted to DC, they all have the common goals to be robust and protected against high current and high voltage events that result from shoot-through, short-circuit, overcurrent, MOSFET reverse recovery, or PCB parasitic inductance behavior.

For example, power tools have high power ratings for industrial and household purposes, such as drilling, grinding, cutting, polishing, driving fasteners, and more. Requirements include:

- Small form factor, as tools are often hand-held
- High efficiency, as tools are often battery operated
- High current, as tools must produce high torque to overcome large loads
- High reliability, as safety is a primary concern if the tool fails
- Good thermal performance, as high power densities without proper dissipation cause systems to overheat

When designing high power systems, these requirements produce tradeoffs and conflict with each other. In the case of power tools, high current, efficiency, and thermal performance can be an increased with a larger board size which conflicts with the need to be small and hand-held.

This makes high power design very important. Like in the case of Electromagnetic Interference (EMI), designing for high power applications is a process of making decisions and planning to mitigate problems that may or may not occur.

1.1 Effects of a Poorly-Designed High-Power Motor Driver System

Surprisingly, poor high-power design does not always result in an electrical fire or smoke. The results are a spectrum. In the case of the electrical fire, the results may be instantaneous, and the first time the motor spins is also the last time the motor spins due to catastrophic board damage. This indicates that something is fundamentally faulty with the design, or some aspects of normal operation are amplified. As a result, some aspect of the design can be reduced or mitigated, controlling the source of damage and reducing its negative effects on the system to bring probability of damage to a negligible level.

In other cases, the motor will spin and damage might occur when commanded to deliver more current, or stop rotating. A change in operation stresses the system beyond what it is capable. In more difficult cases, the motor will spin at the same current or speed for a hundred hours but fail minutes before the test concludes. This could mean that a special use case might cause the design to fail, or regular operation might result in damage to the design over time until a permanent and observed failure occurs.

Understanding the differences in the spectrum allows the designer to understand what kind of change is needed to fix or prevent damage. Just like the spectrum of damage, the spectrum of changes could vary from replacing a component on the bill of materials to a complete redesign of the schematic and layout.

1.2 Example of the High-Power Design Process

This example covers a hypothetical and uses the principles of high-power design to improve a high-power motor driver application. Note, this example serves to show that how the process is utilized and rest of the application note explains the theory that eventually results in the process used.

Consider the following example:

- In a 48-V system running at 20 A using the DRV835x, the system works as expected
- When increasing the current to 30 A, which is the target current, the system is consistently damaged
- This happens for all systems brought above the 30 A current level

Examining the givens, there is a fundamental problem with the system. In this context, the functions of the gate drive circuit must be verified as the next step in troubleshooting.

After going through the troubleshooting steps, the notable observations are:

- The nFAULT signal is exerted only after trying to switch the low side and looking at the criteria, a VGS fault occurred on the low side which means that the gate voltage is not rising to the expected voltage when the input low-side gate signal is switched
- Using a DMM, an impedance test on the low-side gate-to-source shows a couple of couple of ohms which indicates a short and damage
- The damage occurs primarily on a singular phase but some other phases have received damage depending on the system tested

The short between gate-to-source seems to indicate that voltage inductive spiking is the problem as an absolute maximum limit could have been exceeded. This is further supported by the lack of damage at a lower current level. In addition, if there is damage is primarily on a singular phase then this might indicate that the layout is not optimized and might be contributing to the problem.

With a goal to reduce the voltage spiking:

- The gate drive sink and source current were reduced in an attempt to limit the spiking by lowering the IDRIVE.
  - This allowed the system to survive at 30-A but the resulting rise and fall time of the VDS signal, and gates, were too slow for the application. If the rise and fall time were acceptable, then the issue would have been solved here.
- By using an oscilloscope probe on the low-side gate and source voltages at 20 A, the waveforms show there is negative voltage spiking on the low-side source that is close but does not exceed the absolute maximum limits defined in the *DRV835x 100-V Three-Phase Smart Gate Driver* data sheet.
  - This leads the assumption that these spikes get worse as the current increases and eventually exceed the absolute maximum ratings

With some indicators that negative spiking on the low-side source and gate is the problem, some solutions include:

- Add high-side source to low-side capacitors
- Add gate-to-GND diodes
- Increase bulk capacitance
- Analyze the layout around the phase that receives damage and improving it, notably GND and the sense resistor path

Evaluate the options that may fix the problem. To avoid a redesign of the board, its best to look for a change on the bill of materials or populate components that were previously depopulated.

- Because the footprints for the high-side drain to low-side source capacitors were present, but not populated, adding a capacitor fixed the problem without having to do a redesign and without lowering the gate drive current.

This application note breaks down the process into a development of troubleshooting guidelines, a library of external circuits, TI driver product features, or layout techniques to combat the volatile nature of higher power systems.

2 Examining a High-Power Motor Drive System at a High Level

2.1 Anatomy of the Motor Drive Power Stage and How to Troubleshoot

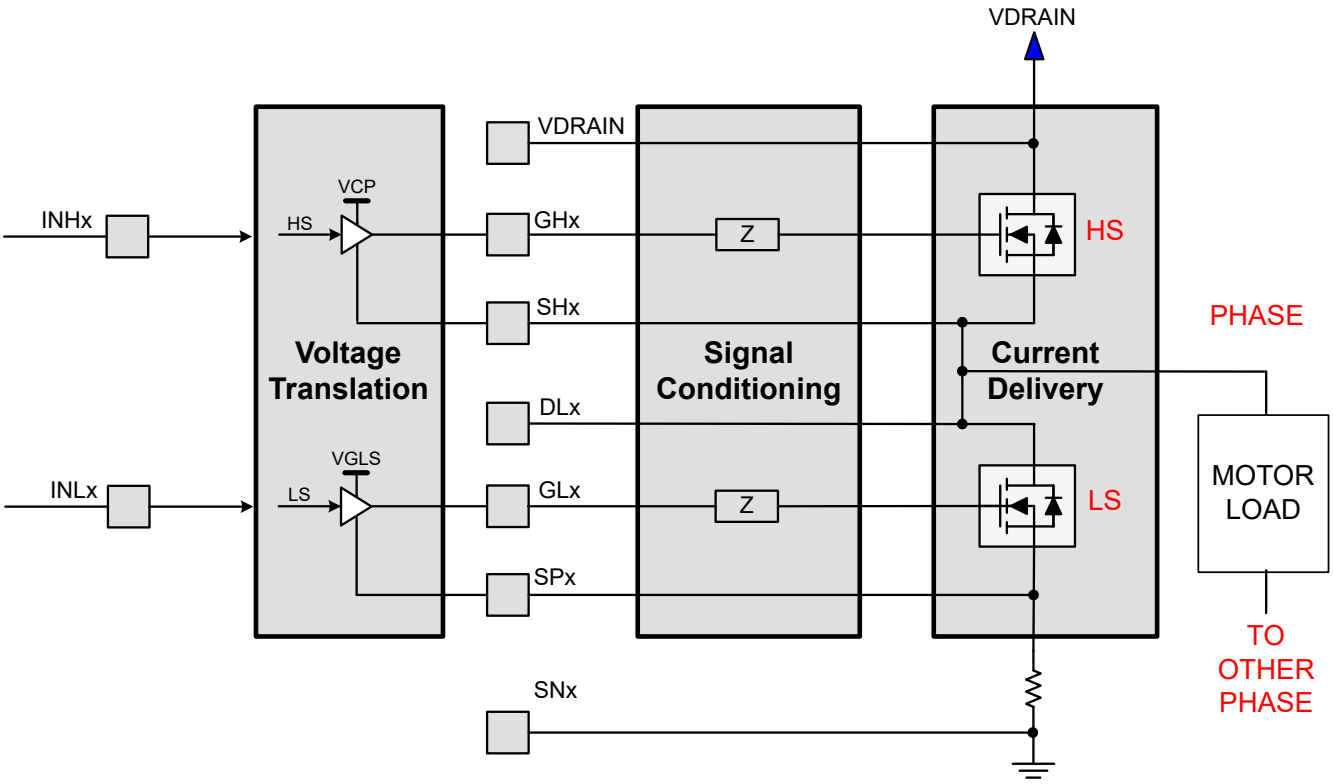

Figure 2-1. High-Level Power Stage

Before developing troubleshooting guidelines, a library of external circuits, TI driver product features, or layout techniques, the typical gate driver system and its sub-functions must be understood.

Starting on the right side of Figure 2-1, one function of the motor driver power stage, otherwise known as inverter, phase, or half bridge, is to deliver current to the motor. Broken into its simplest parts, current flows from VDRAIN through the high-side FET and into the motor, assuming the low-side FET is off. Alternatively, if the low-side FET is on, and the high-side FET is off, current flows from the motor and through the low-side FET to GND. In the context of kilowatt motor drive application, up to hundreds of amps can flow through these FETs.

Moving to the left side of Figure 2-1, another function of the power stage is to translate the digital logic PWM input signals (for example, INHx and INLx) to signals at a higher analog voltage level, such as 24 V or 48 V. In this way, one part of the power stage is voltage translation from digital level signals to analog level signals. In addition, it is usually part of the functions of the motor driver to produce the voltage rails from the supplied motor driver supply voltage to translate the analog voltage levels. These analog voltages can be higher than VDRAIN, or the highest input voltage in the system. As such, linear regulators, charge pumps, or bootstrap architectures are used to achieve these voltages (for example, VCP and VGLS).

In the middle of Figure 2-1, another secondary function of the power stage is to condition or control the signals at the gates of the FET. Because MOSFETs can act as switches, resistors, or current sources depending on the gate voltage in relation to the drain and source voltages, all voltages of the FET must be controlled and monitored. Protection, signal conditioning techniques, and specialized circuits all fall under this function.

In summary, three functions of the motor drive power stage are:

- Delivering current to the motor
- Voltage translation from digital voltage levels to motor voltage level
- Gate signal conditioning or protection

2.2 Troubleshooting a High-Power System

The first step in the troubleshooting process is to understand where the damage occurred. Check the functions of the power stage to evaluate if any function no longer works as intended after damage has occurred.

For the case of delivering current to the motor, take a Digital Multimeter (DMM) and perform an impedance check between drain and source of the FETs, or VDRAIN and SHx shown in Figure 2-1. The drain-to-source path is expected to be high impedance (that is, kΩ) when unpowered so low impedance indicates damage to the FETs and current delivery path. For more troublesome troubleshooting, use an oscilloscope to probe the gate voltage, drain voltage, and source voltage at the FET during a transition to check for stability and the amount of ringing on the signals.

In the case of voltage translation, take a DMM and perform an impedance check between the gate signals and the gate voltage supplies, such as VGLS, VCP, or GND as shown in Figure 2-1. These paths are expected to be high impedance with a capacitive load. Low impedance signifies damage (that is, ones of ohms). For more in-depth troubleshooting, use an oscilloscope voltage probe to check the stability of the voltage supplies during operation.

For the case of conditioning or protecting gate signals, take a DMM or LRC meter and do an impedance check on the components in the path to ensure the passive components were not damaged. Simply comparing the read value with the expected value listed in the schematic is an easy way to check for damage.

It is important to note that most motor drivers integrate these functions into one device or piece of silicon. As a result, most of these integrated gate drivers are able to monitor and check these functions and notify the designer with some sort of FAULT, WARNING, LOCK GPIO signal, or read-able register. If the nFAULT signal is asserted, it is critical to understand why the nFAULT signal is asserted and which fault is triggered. Criteria for every fault is usually provided in the data sheet. More importantly, if the nFAULT signal can be reset, the signal can be monitored with an oscilloscope voltage probe and used as a falling-edge trigger to capture other signals, such as the FET gate, source, or drain voltages.

In summary, the steps are:

- Use a DMM to check impedance between all terminals of the FETs
- Use an oscilloscope to probe gate, drain, and source voltages to check for stability and ringing
- Use a DMM to check impedance between the gate and gate voltage supplies
- Use an oscilloscope to probe gate supply voltages for stability
- Use a DMM or LCR to confirm passive component values in power stage
- Understand the cause for any FAULT signals asserted

Fortunately, high-power design does not primarily need to be an experiment that takes place after something has gone wrong. As previously mentioned, there are actions that can be taken to mitigate potential problems.

These actions may result in a different board architecture or different operation of gate driver leading to more components or board area. As such, there are tradeoffs between implementing every possible action, and considering the most important requirements of the real system - this is the art of high-power design.

3 High-Power Design Through MOSFETs and MOSFET Gate Current (IDRIVE)

3.1 MOSFET Gate Current

As previously mentioned, the MOSFET drain and gate current is the backbone of power delivery to the motor. To deliver current and turn the FET on, charge must build up on the intrinsic gate capacitors of the MOSFET. This process is explained in more detail in the *Fundamentals of MOSFET and IGBT Gate Driver Circuits* and *Understanding Smart Gate Drive* application notes.

As a result, link the rate of electrical charge, or current, at the gate-to-the rise in drain-to-source voltage of the FET, as shown in the ideal first-order Equation 1:

$$SR_{DS} = \frac{I_{DRIVE} \times V_{DS}}{Q_{gd}} \quad (1)$$

Where:

- SR_{DS} = slew rate of the drain to source voltage, in seconds
- I_{DRIVE} = current sourced to or sunk out of the gate, in amps
- V_{DS} = voltage difference between the MOSFET drain voltage and source, in volts
- Q_{gd} = inherent gate-to-drain charge for the MOSFET, in coulombs

According to Equation 1, a high I_{DRIVE} and a small Q_{gd} results in a very fast slew rate, as VDRAIN is usually fixed in a system unless the system supply voltage is specifically designed to change. Since a high slew rate results in lower switching losses in the MOSFETs it can seem at first beneficial to make the slew rate as high as possible. However, most designers try to use a higher slew rate without realizing that there are adverse effects of using a slew rate that is too high for the design.

3.1.1 How Gate Current Causes Damage

Unfortunately, there are adverse effects of a high slew rate in a high-power system. The inherent capacitive coupling of the MOSFET, and the effects of parasitic LC resonance increase as more current flows through the FETs and the VDS voltage transitions more quickly.

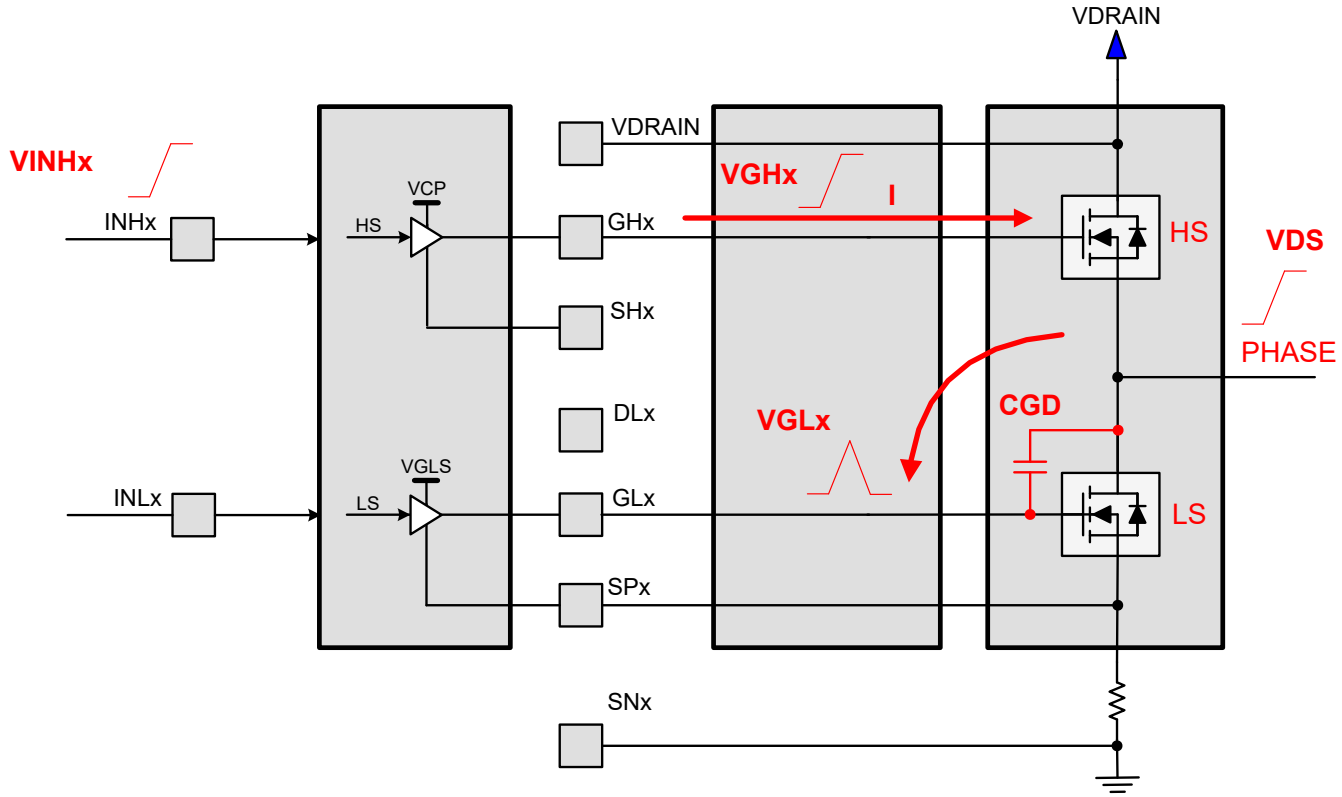

Figure 3-1. Inductive Spiking and Coupling From Switching on MOSFET

As shown in Figure 3-1, the high-frequency component of the rising edge of the gate signal—and more importantly, the rising VDS signal going through the Miller region—causes current to flow onto the intrinsic capacitors of the other FET. This signal couples through the inherent gate-to-drain or gate-to-source capacitor because capacitors have lower impedance at higher frequencies. If these coupled signals are high enough, they can exceed absolute maximum ratings of the motor driver or turn on the low- and high-side FETs within one phase to cause a shoot-through condition as current bypasses the motor and flows through the direct path from VDRAIN to GND.

MOSFETs have a limit of maximum slew rate before they turn on due to CGD coupling. This means that if the slew rate is too high—**even if the gate is shorted directly to the source**—the MOSFET turns on. When considering the gate driver pulldown strength and parasitic inductance on the gate path, this reduces the maximum slew rate possible before causing unintentional turn-on.

Simply put, higher gate current means more coupling, and less gate current means less coupling.

To reiterate:

- Too much gate current leads to damage
- Decreasing the current prevents damage
- Choosing the right gate drive current (I_{DRIVE}) for the system is essential.

Now that the effects of too much gate current are understood, methods to adjust the gate current must be developed and calculation of a gate current for a given system must be derived.

3.1.2 Gate Resistors and Smart Gate Drive Technology

While gate current or I_{DRIVE} plays a huge role in the switching characteristics of FET, methods for adjusting the gate current are required.

3.1.2.1 Gate Resistors

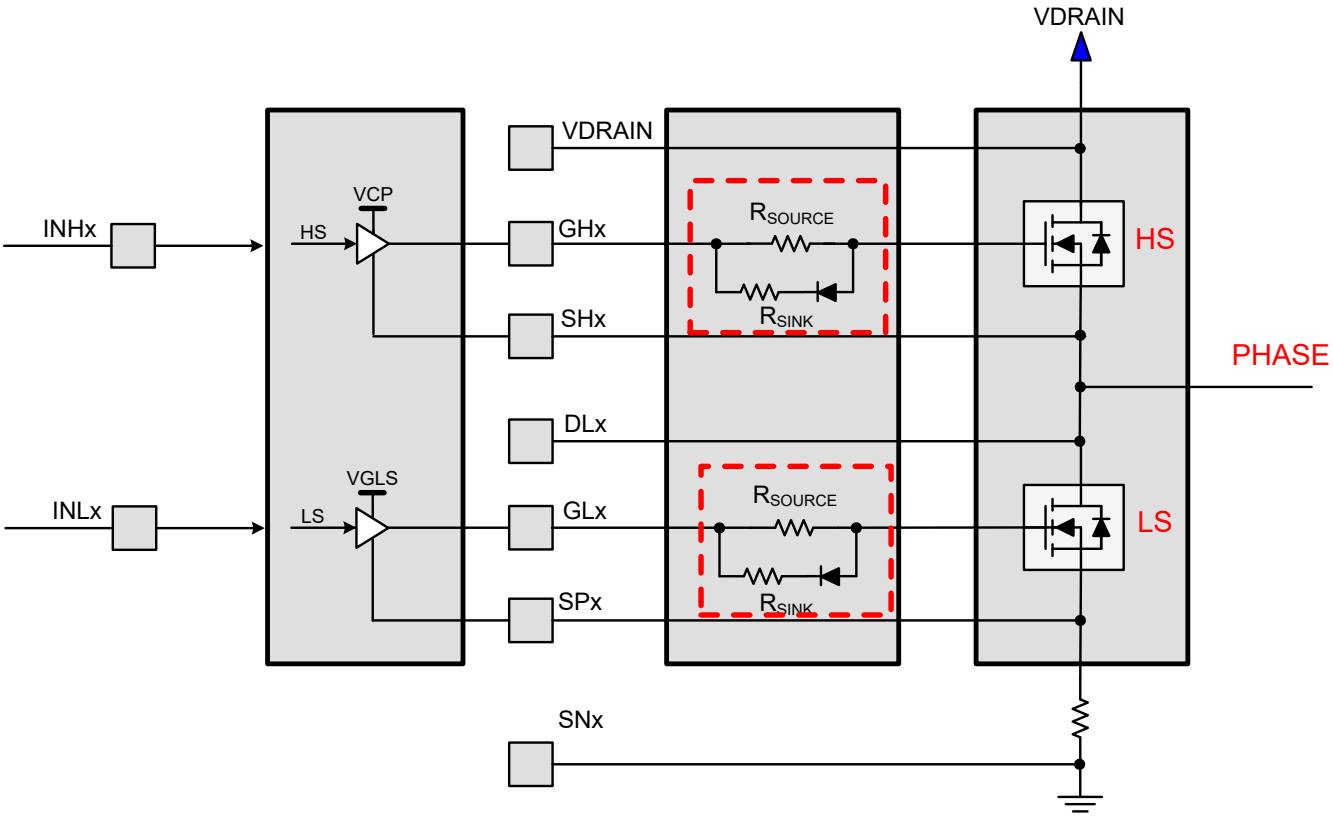

Figure 3-2. Sink and Source Resistors When Gate Current is Fixed

In most gate driver devices, the source and sink, or pullup and pulldown, gate-drive current values are found in the data sheet. In some devices, this value is fixed internally, and the output current capability is much larger than the calculated IDRIVE for a given FET.

Add an external series gate resistor to control the slew rate of the applied gate voltage and reduce the peak current applied to the gate of the FET. This is similar to a RC filter: R is the gate resistor, and C is the inherent capacitance of the MOSFET. For further control, place another gate resistor and diode in parallel – if the designer wants to control sink and source separately. This is shown in Figure 3-2.

The MOSFET parameters, system voltage, and board parasitics all affect the final slew rate, so selecting an optimal gate resistor value is an iterative process. This process is explained in the *External Gate Resistor Design Guide for Gate Drivers* tech note.

There is a helpful principle that is beneficial to help determine the best resistance to use for a gate resistor: less resistance equals more current with a faster slew rate, and more resistance equals less current with a slower slew rate.

3.1.2.2 Smart Gate Drive and Internally-Controlled Sink and Source Gate Currents

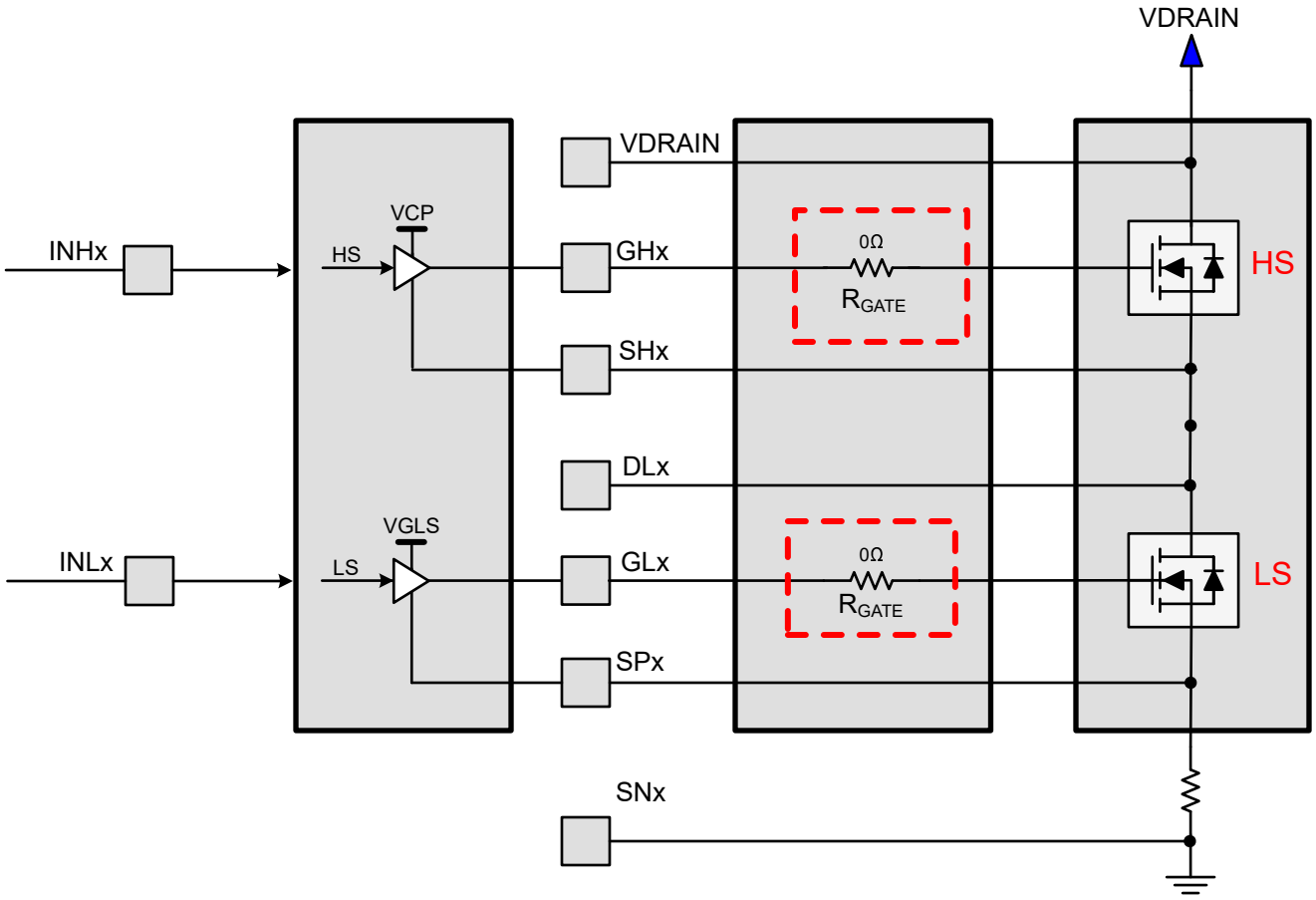

Figure 3-3. Gate Resistor Placeholder When Sink and Source Current are Controlled, for Example, Smart Gate Drive

Several TI gate drivers contain technology called Smart Gate Drive which is used to control the current delivered to the FET. The designer simply needs to pick the source and sink current through changing bits in a register or configuring an external resistor on a designated pin as described in Figure 3-2. More information is found in the *Understanding Smart Gate Drive* application note.

With that being said, it is still a good practice to put a series 0-Ω resistor between the gate of the FET and the gate drive pin of the device as the designer might need to make a sink or source current between two settings or lower than the lowest setting. This resistor can also be used as an easy-to-access test point for voltage measurements. This is shown in Section 3.1.2.2.

3.1.2.3 Summary for Gate Resistors and Smart Gate Drive Technology

- Both the gate resistor and the Smart Gate Drive technology adjust the gate sink and source current
- Choose a gate resistor that is equal to the reactance of the source inductance for critically damped performance and choose a gate resistor that is up to twice the reactance of the source inductance for underdamped performance as described in the *External Gate Resistor Design Guide for Gate Drivers* tech note
- Alternatively, the resistors can also be chosen by using general calculations, observing the VGS waveform, and adjusting the value higher or lower for slower or faster slew rates, respectively
- The Smart Gate Drive source or sink current can be calculated for a given FET, as described in Section 3.1.3
- The process for choosing the gate resistor or IDRIVE is iterative and experimental
- If the source and sink current can be controlled within the device, for example, Smart Gate Drive, it is still a good practice to add a 0-Ω resistor in series with the gate of the FET and replace with a non-zero resistor if further adjustment is required

3.1.3 Example Gate Current Calculation for a Given FET

For this example, the DRV835x family of devices is used and paired with the CSD19536KTT power MOSFETs, which are used in the 54-V, 1.5-kW, > 99% efficient, 70 × 69 mm^2 power stage reference design for 3-phase BLDC motors: TIDA-010056.

The steps for estimating the approximate gate current generally are:

1. Find the FET part number and the associated data sheet
2. Locate the Q_{gd}value in the data sheet
3. The typical Q_{gd} is acceptable but always be aware of the minimum or maximum tolerance of the Q_{gd}
4. Estimate needed VDS rise and fall time. For many high-power systems, rise and fall times between 100 ns to 300 ns are a good starting point as a general guideline.
5. Alternatively, the designer can rearrange Equation 2 to get the equation in terms of gate drive current (I_{DRIVE}) instead of VDS slew rate (SR_{DS}) where 25 V/µs to 100 V/µs is acceptable as general input:

$$I_{DRIVE} = \frac{Q_{gd}}{t_{RiseFall}} \tag{2}$$

Where:

- I_{DRIVE} = current sourced to or sunk out of the gate, in amps
- $t_{RiseFall}$ = equivalent rise or fall time for the VDS (not VGS), in seconds
- Q_{gd} = inherent gate-to-drain charge of the MOSFET, in coulombs

For the case of the CSD19536KTT, Q_{gd} = 17 nC and we can use the general guidelines to put 100 ns into the rise and fall time of Equation 3. Note, some designers like to make the fall time two times faster than the rise time.

$$I_{DRIVE} = \frac{\left(17 \times 10^{-9}\right)}{\left(100 \times 10^{-9}\right)} \tag{3}$$

$$I_{DRIVE} = 170\ mA \tag{4}$$

The DRV835x family does not have an I_{DRIVE} setting of exactly 170 mA, but it does have lower options of 150 mA or 100 mA for source current and 100 mA for sink current. Source refers to the current taken from the gate voltage supply and pushed into the FET, which corresponds with the rise time; and sink refers to the rate at which charge is pulled from the gate of the FET and pushed to the source of the FET, which corresponds with the fall time.

In the case where the rise and fall time is 300 ns, the same equation can be used:

$$I_{DRIVE} = \frac{\left(17 \times 10^{-9}\right)}{\left(300 \times 10^{-9}\right)} \tag{5}$$

$$I_{DRIVE} = 56\ mA \tag{6}$$

Using the DRV835x family again, choose 50 mA for the source current but the smallest sink current is 100 mA. This is a perfect example for replacing the 0-Ω gate resistor with a nonzero value to get the equivalent gate sink current below the lowest setting. If not planning to have the 0-Ω gate resistor, traces must be cut and the board redesigned to get the desired performance.

Remember, we are merely using a starting gate drive current that was calculated with a safe general guideline. This is a first order equation and does not exactly match what is seen in the real system, but the goal is to get within a reasonable starting point. This is why we round down if the device does not have an exact selection, to make the equivalent rise or fall time to be longer than the calculated value. Designers are expected to increase or decrease this number after testing.

4 High-Power Design Through External Components

Plenty of theory and simulation supporting evidence for this section is found in the *Understanding and Mitigating Motor Driver Board Parasitics through Simulation* article. It is highly recommended to supplement the theory discussed here with the article.

Many of the sections discuss the theory but are summarized with bullet points. It is encouraged to read the section and refer back to the bullet points as a section summary.

As we progress through the section, more circuits are developed that can be added to the system. These additions might conflict with system considerations and goals, such as the need to be handheld which limits board space. Deciding what to add and what not to add is part of the art of high-power design.

4.1 Bulk and Decoupling Capacitors

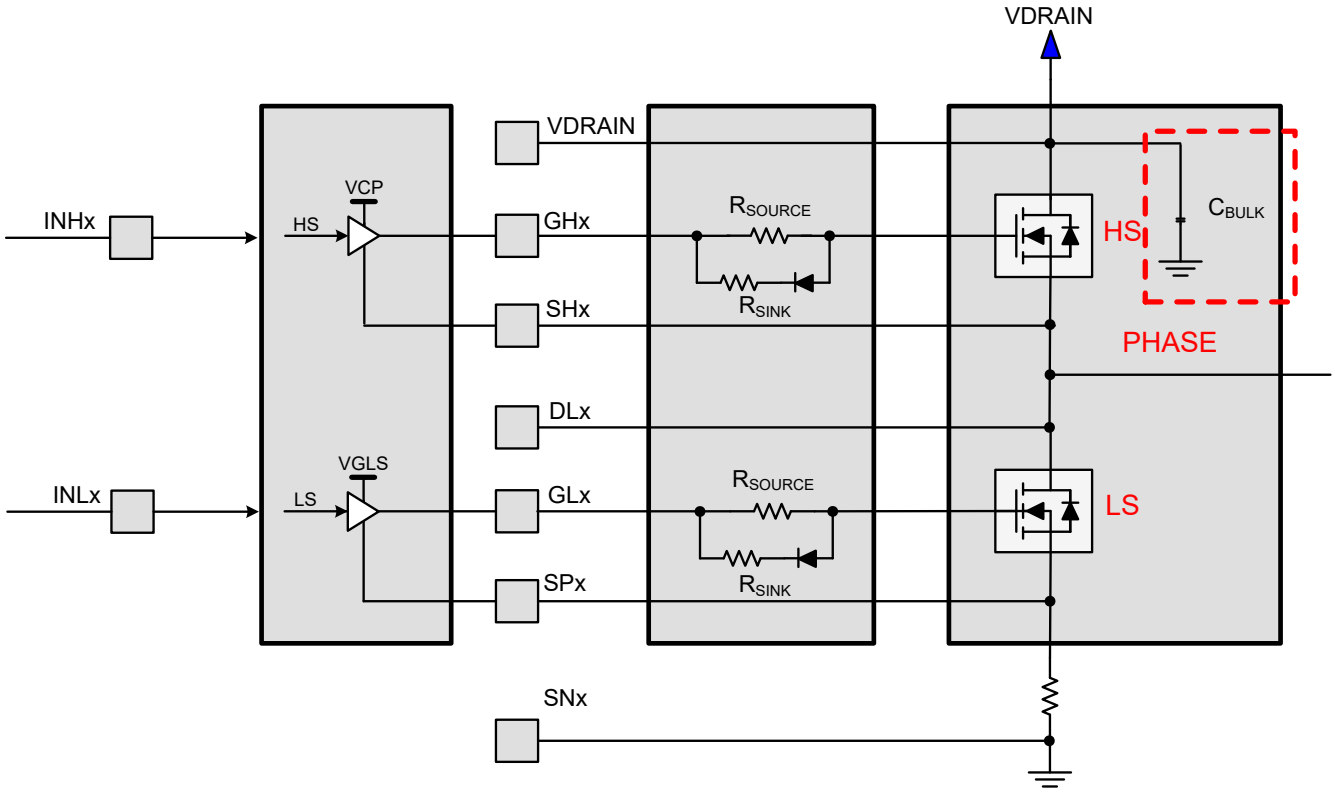

Figure 4-1. Bulk Capacitor Example

Bulk and decoupling capacitors have the primary purpose of providing instantaneous charge into a system so the main power supply does not have to. To be more specific, current ripple within the supply, and voltage spikes from parasitic inductance created from wire and traces are the result of insufficient charge in the supply. Since the power supply is be physically located far from the motor drive circuit, there is quite a lot of inductance in the path from the supply to the MOSFETs.

Small-valued capacitors can be emptied and filled with charge relatively quickly, where larger valued capacitors can store a lot of energy, but do not react as quickly. This is why most data sheets show recommended components with large and small capacitors placed in parallel on power supplies. In the context of the power stage, millifarads or hundreds of microfarads electrolytic or ceramic capacitors are used in combination with singular to tens of microfarads ceramic capacitors.

In addition, there are times where the motor can act as a generator where the bulk and decoupling capacitors store energy from the motor to prevent rising voltage on the drain of the high-side FET, or VDRAIN as shown in Section 4.1.

In summary:

- Because low value capacitors can provide some charge quickly and high value capacitors provide a lot of charge over time, it helps to reduce voltage ringing and voltage spikes in the system
- It is highly recommended to always use them. A few 100-µF to 330-µF capacitors in parallel with a few 1 µF to 2.2 µF is a good starting point with some more footprints that can be replaced later.
- A common rule of thumb is 2 µF/W; however, actual system results vary significantly

Truthfully, this is nebulous advice. This does not describe the process of estimating parasitics for a given layout and simulating their effects through SPICE to get an optimal bulk capacitor value. As a result, there are no equations or hard math. However, we want to highlight this as practical advice. There is a lot less effort in the design process to test the system in reality or rely on past system knowledge in combination with the data sheet. If the performance is not good enough, then designers add more capacitors or change the bill of materials so an existing capacitor is replaced with a capacitor of a different value to fix the problem.

In summary, planning to implement a general rule to get a baseline capacitor value, but testing a system in reality, might result in good performance with no other changes needed, or bad performance where an experimental and iterative process fixes the performance issues.

4.1.1 Note on Capacitor Voltage Ratings

Ceramic capacitors have poor DC voltage derating. This is a known disadvantage of using a ceramic capacitor instead of a different material, like an aluminum oxide electrolytic. A ceramic capacitor experiences one half of the rated capacitance when exposed to the rated voltage.

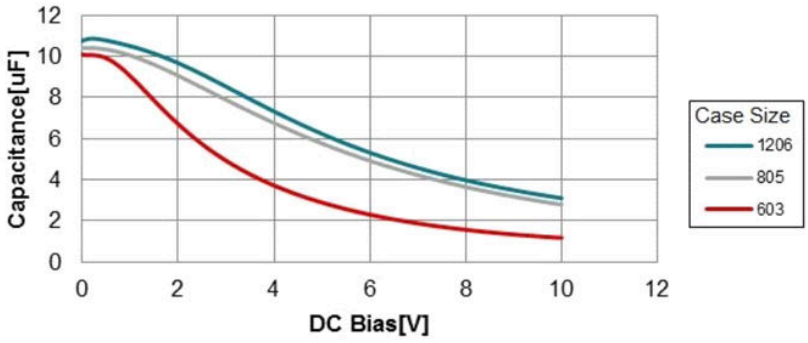

Figure 4-2. Capacitance vs Voltage Exposed to Capacitor by Package Size

Figure 4-2 shows an actual production capacitor example. Observe, the 10-µF capacitor rated for 10 V results in an equivalent capacitance of only 1–3 µF when biased at 10 V. These graphs are found in any capacitor data sheet and other engineers have already explored and exposed these facts.

In the context of high power, a 48-V system needs ceramic capacitors rated for a minimum of 100 V, or 2 multiplied by 48 V, which equals 96 V with the closest industry rating at 100 V. As a result, 48-V rated capacitors in the power stage are not helpful and must be sized accordingly.

Note, this guideline is sometimes relaxed to 1.5 multiplied by the supply voltage, as in the case of 60-V applications where multiplying by 2 gives 120 V which sits between the 100 V and 150 V industry standard. Therefore, the 1.5 times 60 V calculates to 90 V or 100 V, just like the 48-V case. As Figure 4-2 shows, this guideline may fail and it is recommended to consult the data sheet of the capacitor for more information.

In summary:

- Effective capacitance decreases when more voltage is exposed to a capacitor
- Choose capacitors with voltage ratings at 2 or 1.5 times the typical voltage that the capacitors are exposed to:
  - This is approximately a 100-V rating for 48-V systems

- Ceramic capacitors have much worse voltage derating compared to aluminum capacitors so the general guidelines do not apply to aluminum electrolytic capacitors
  - It is recommended to check the data sheet of the capacitor for the exact derating provided by the manufacturer

4.2 RC Snubber Circuits

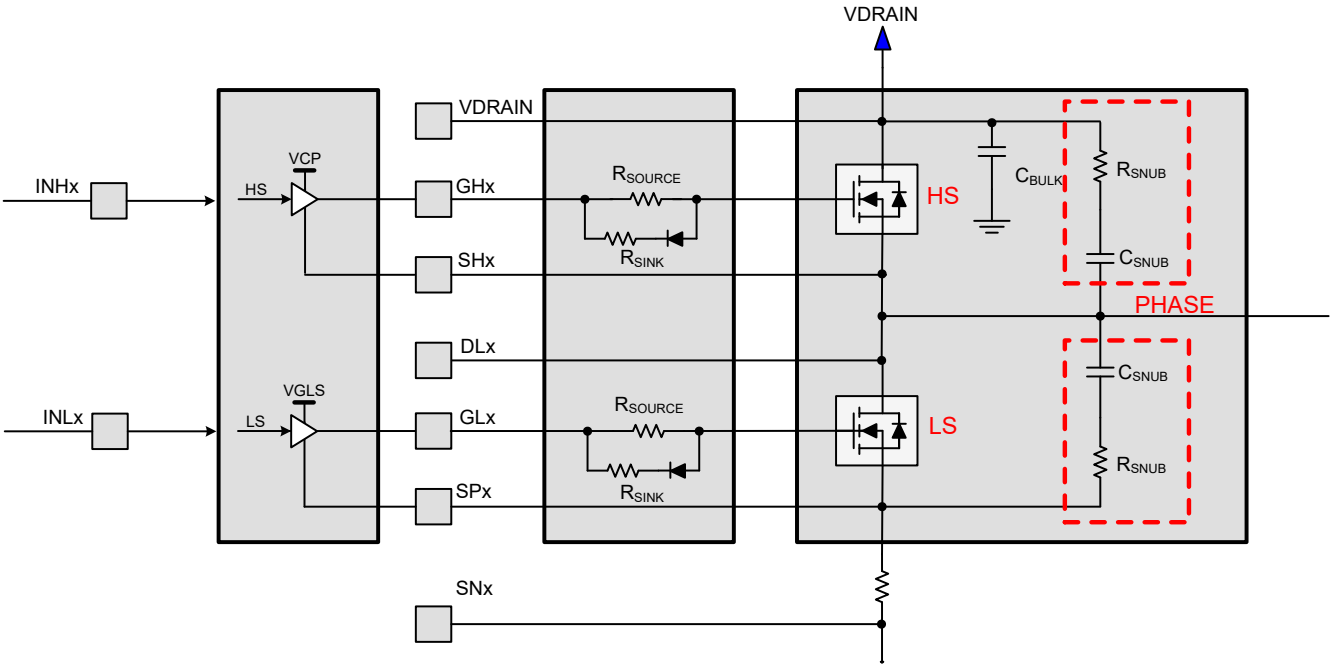

Figure 4-3. Example RC Snubbers

The snubber circuit is not only used in motor driver applications but is also used in a lot of switching regulator circuits. As a result, there are a lot of resources that have covered this subject.

For an introduction, the RC snubber consists of a resistor and capacitor connected in series from the switch node to a constant voltage reference, such as a GND connection. For a motor drive circuit, place an RC snubber between the phase node and the high-side drain of the FET, and between the phase node and the low-side source of the FET shown in Figure 4-3.

They are most effective reducing phase oscillations, or voltage ringing across each MOSFET. They reduce the initial spike at a node and provide a dampening factor to reduce the number of ringing cycles.

However, the values of RC must be tuned for the parasitics of a particular system. Unless the parasitics can be modeled, the R and C values are chosen experimentally. Luckily, there are many resources explaining how to calculate them, such as the E2E FAQ for Proper RC Snubber Design for Motor Drivers as an example.

In summary:

- RC snubbers are very good at reducing the settling time of a ringing node
- Optimal RC snubber values depend on the parasitic values of a given system
- Place snubbers very close to the MOSFET, on the same layer
  - If placed on opposite layers of the FET, the via inductance reduces the effectiveness of the snubber

4.3 High-Side Drain to Low-Side Source Capacitor

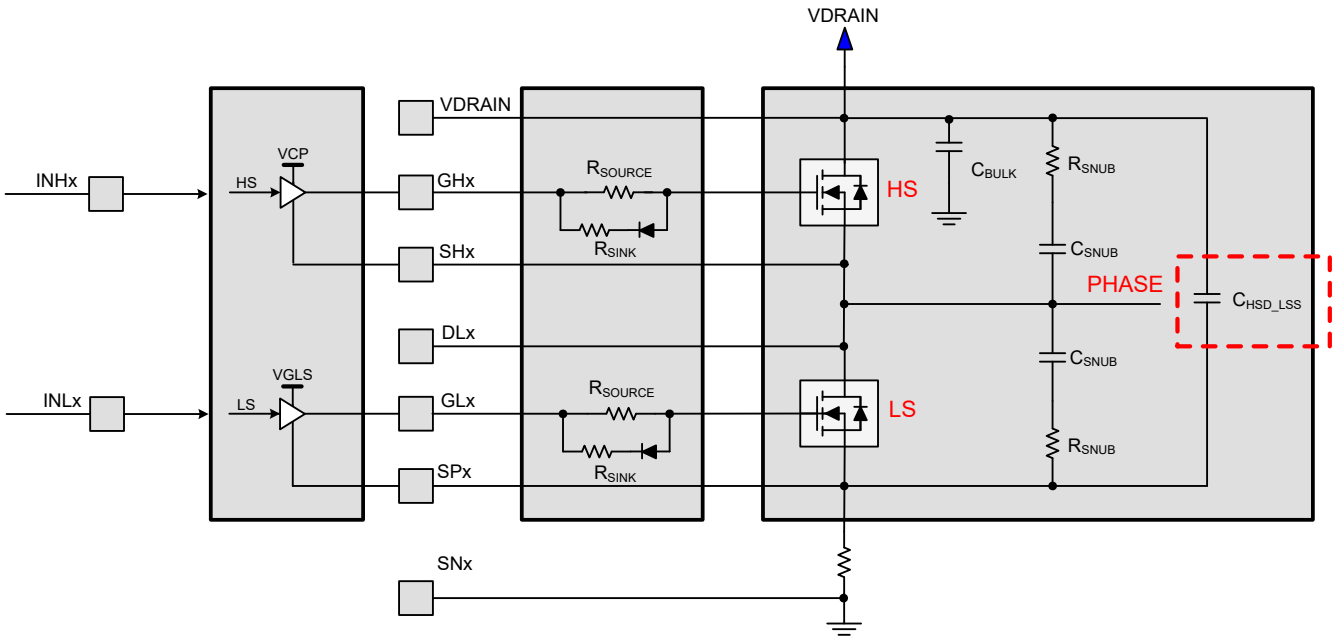

Figure 4-4. Example High-Side Drain to Low-Side Source Capacitor Location

At first glance in Figure 4-4, high-side drain to low-side source capacitors seem to be self-explanatory and are often confused with the decoupling or bulk capacitors. However, most motor driver applications do not have the low-side source connected to GND. Instead, the low-side source is usually connected to a shunt resistor which is used for current sensing, and is then is then connected to GND.

This is important because decoupling capacitors need stable references to reliably provide charge. GND instability can be present in a system as a result of inductance introduced by the sense resistor layout, motor current flowing through the low-side FET, or bad grounding techniques. If GND bounces along with the switch node then the decoupling capacitors cannot do their job to provide charge from a stable reference and low inductive path. For reference, a 0.2512 component package size, which is a common package for sense resistors, introduces 1–5 nH of parasitic inductance.

The HS drain to low-side source capacitor can circumvent these problems because it is connected to VDRAIN, which is assumed to be stable, and can dump charge directly onto the node, instead of through the path of a sense resistor. This is the concept of an AC GND and is the reason why the RC snubber can also be connected to the HS drain, as well as the LS source.

As a result:

- This method does a great job suppressing negative bouncing on the low-side source and GND.
- Selecting a value of around 0.01 µF–1 µF and placing them as close to the FET as possible ensures they work correctly
  - Specifically, the value should be low enough to not impact the non-parasitic ripple of the current sense waveform, which reflects the real behavior of the motor

A lot of engineers underestimate this mitigation technique and fail to use footprints as they have already prioritized RC snubbers and bulk capacitors at this point. If GND or the sense resistor is ringing negative, or below GND, the HS drain to LS source capacitor provides charge in a low impedance path. Waveforms showing the GND and LS source voltage are helpful to determine if negative ringing is occurring and whether to update the design to add HS drain to LS source capacitors to the half bridges.

4.4 Gate-to-GND Diodes

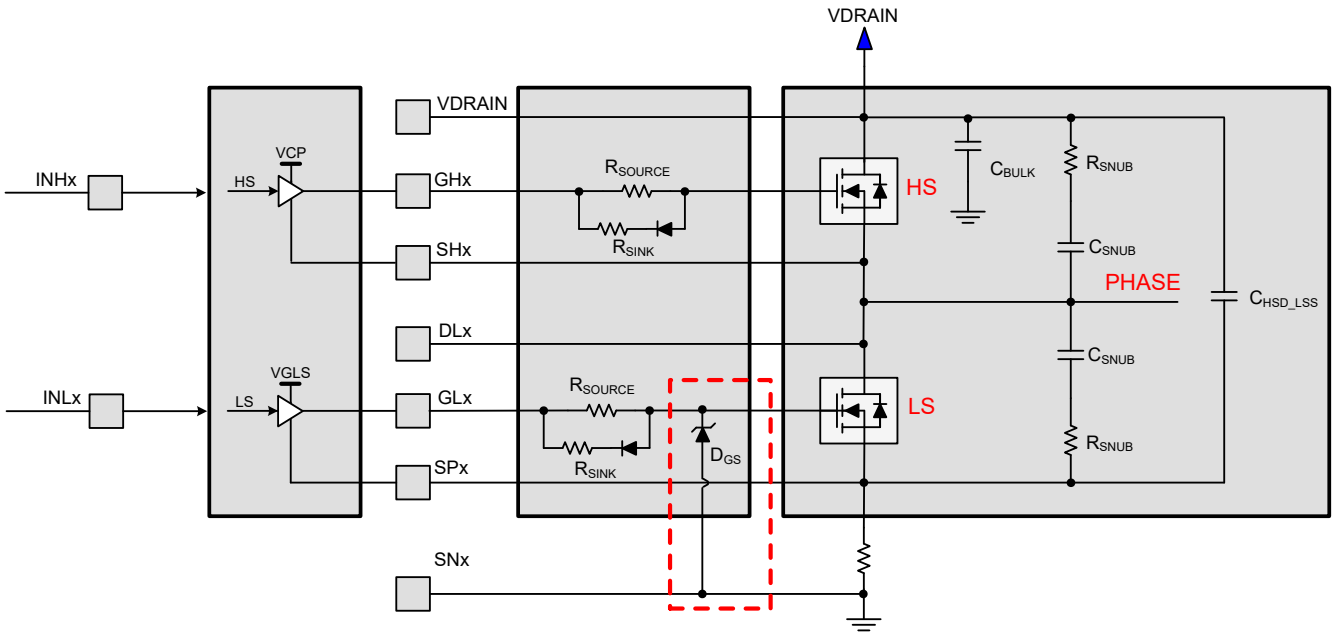

Figure 4-5. Example Gate-to-GND Diode

Simply put, diodes clamp a node to a voltage so no absolute maximum ratings are violated for the device. Current rating, clamping voltage, and timing information that are in accordance with the absolute maximum ratings of the gate driver and MOSFET are important for choosing an effective diode. A popular location is to connect the cathode to the GLx node, near the FET, and the anode to GND to help with negative transient spikes as shown in Figure 4-5.

These are not the primary recommended mitigation techniques that are meant to replace the other methods because diodes simply reroute energy as opposed to suppress energy by filtering or decoupling. Diodes often introduce more losses and power dissipated compared to a capacitor since voltage spiking can occur every PWM cycle.

In summary:

- TVS diodes clamp voltage below absolute value ratings of the device to prevent damage
- Diodes should be used in conjunction with other mitigation techniques and not be relied upon
- Diodes dissipate more power compared to current moving in and out of capacitors

5 High-Power Design Through a Parallel MOSFET Power Stage

To increase the current-conducting capability of a half-bridge circuit, it is common to place multiple MOSFETs in parallel by tying drains, sources, and gates of the MOSFETs together. From a theoretical standpoint, treat these multiple parallel MOSFETs as one single component.

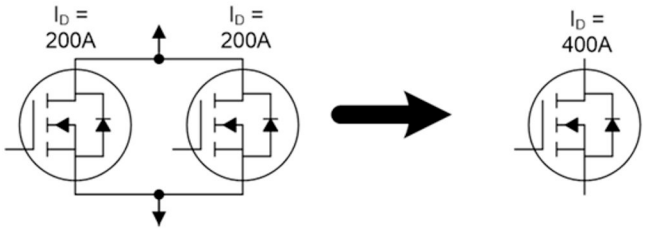

Figure 5-1. Using MOSFETs in Parallel to Achieve Higher Current-Carrying Capability

In reality, no two MOSFETs are ever exactly identical. This means that ultimately, one MOSFET turns on first, and one MOSFET carries more of the current. Minimizing this difference is critical to system operation. The theory and process behind parallel MOSFET design is explained in the *Driving Parallel MOSFETs* application brief.

There are a few considerations that can be summarized:

- Add one resistor for each gate of the FETs used in parallel, not one resistor for all of the parallel FETs. Mismatched MOSFET gates will ring against each other without additional impedance between them.
- Keep FETs physically very close together and with similar or identical layout
- Keep gate trace unified and of equal thickness, and split them very close to the gates of the FETs
- Pair GHx with SHx, and GLx with SLx traces that route back to the gate driver so they are similar lengths and widths
- Source and drain connections should use copper planes, not only traces

6 High-Power Design Through Protection

6.1 VDS and VGS Monitoring

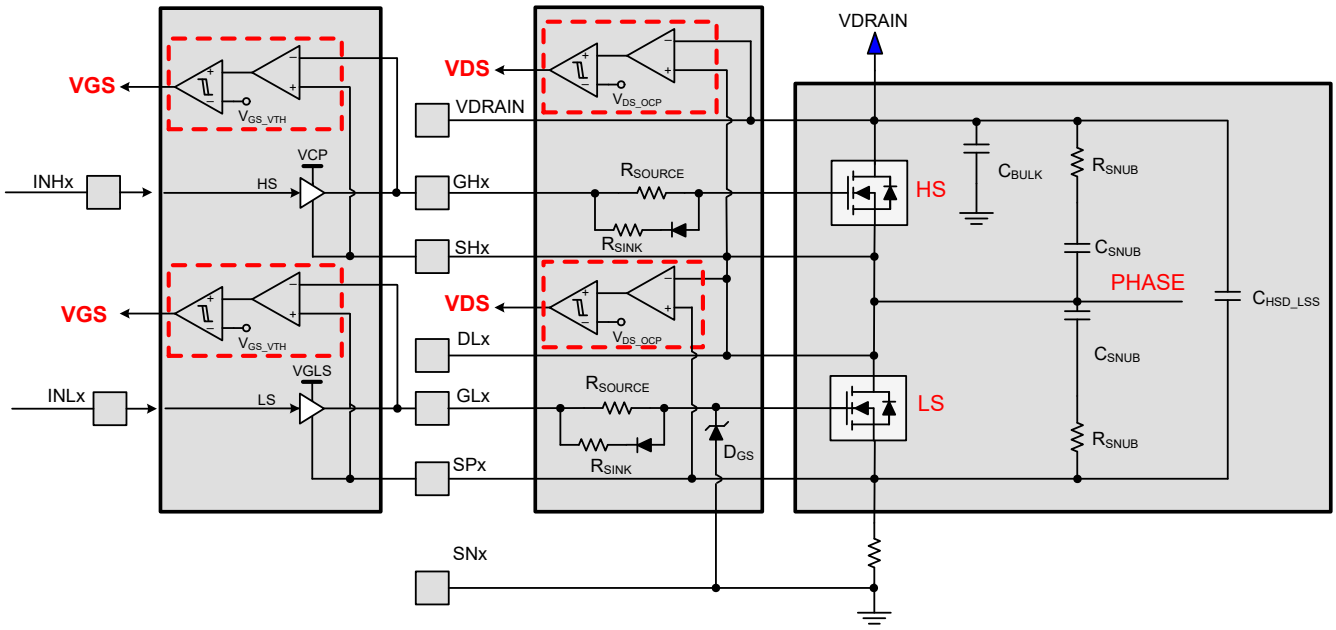

Figure 6-1. Example Implementation of VDS and VGS Monitors

As the names imply, VDS and VGS monitoring simply aim to monitor the voltage at the gate, source, and drain of the FET.

In a shoot-through example, a high-side FET within one phase, or inverter leg, is turned on. After some time, the input signals are changed to turn off the high-side FET and then turn on the low-side FET within the same phase. If the high-side FET and the low-side FET are turned on at the same time, the motor is bypassed and current flows through the much lower resistance path of the high-side and low-side FET at the same time.

The problem with a shoot-through event is that the resistive path to ground is really low. For example, the resistive path from a 48-V supply through the motor resistance (between hundreds of milliohms and one ohm) is much higher resistance than when the supply is shorted to ground through the ones of milliohms resistance of the FETs. The excess current can exceed the current rating of the FETs, can cause massive inductive spiking which can violate the absolute maximum ratings of the device, and can also cause the PCB to increase dramatically in temperature which can result in permanent damage to the PCB.

If the difference between the gate and source voltage (VGS) is monitored, we can understand whether or not the FET is on and conducting current. If the difference between the drain and source voltage is monitored, we can understand if the current is conducting through the FET. As a result, we can monitor these two voltages and make intelligent decisions when to turn the FETs on and off and prevent the driver from turning on both FETs in the same phase. In short, VGS monitors determine if the gate is on and VDS monitors determine if current is flowing when the gate is on.

The typical implementation is to monitor these voltages with comparators. Some integrated devices have some shoot-through protection features by inserting a time delay between turning off one FET and turning on the other, or not allowing the input signals to turn the high and low side on at the same time. However, some devices do not integrate the VGS or VDS monitors within the device, and will therefore, not override the inputs in the case of a shoot-through event. It is always best to check the data sheet of the gate driver for more information.

In the case of TI technology, Smart Gate Drive relies on the states of the VGS and VDS monitors to determine whether to allow or prevent the gates from turning on. More information is found in the *Understanding Smart Gate Drive* application note.

In summary:

- Monitoring VGS determines if the FET is on
- Monitoring VDS determines if current is flowing through the FET when the gate is on
- Including VGS and VDS comparator outputs into the commutation logic, which overrides the inputs, protects the system during high current or damaging power stage situations such as shoot-through

6.1.1 Turning Off the FETs During an Overcurrent, Shoot-Through, or FET Shorting Event

If the VDS monitors or other current protection recognizes an overcurrent event, the obvious solution is to turn off the FETs so they stop current from passing through. In this scenario, the phase current could be more than 10 or 100 times higher than the typical use case. As already explored in Section 2, more current in the phase results in higher parasitic inductive spiking, but increasing the FETs rise or fall time by decreasing the gate drive current decreases the inductive spiking.

In a typical gate-driver case, Section 3.1.2.2 established the sink current is fixed by the external gate resistors and cannot be changed during the overcurrent event. However, TI's Smart Gate Drive technology automatically lowers the gate drive current so that the FET has a longer fall time than the typical value, which reduces the overall voltage spiking that occurs from an overcurrent event.

6.2 Passive Gate-to-Source Pulldown Resistors

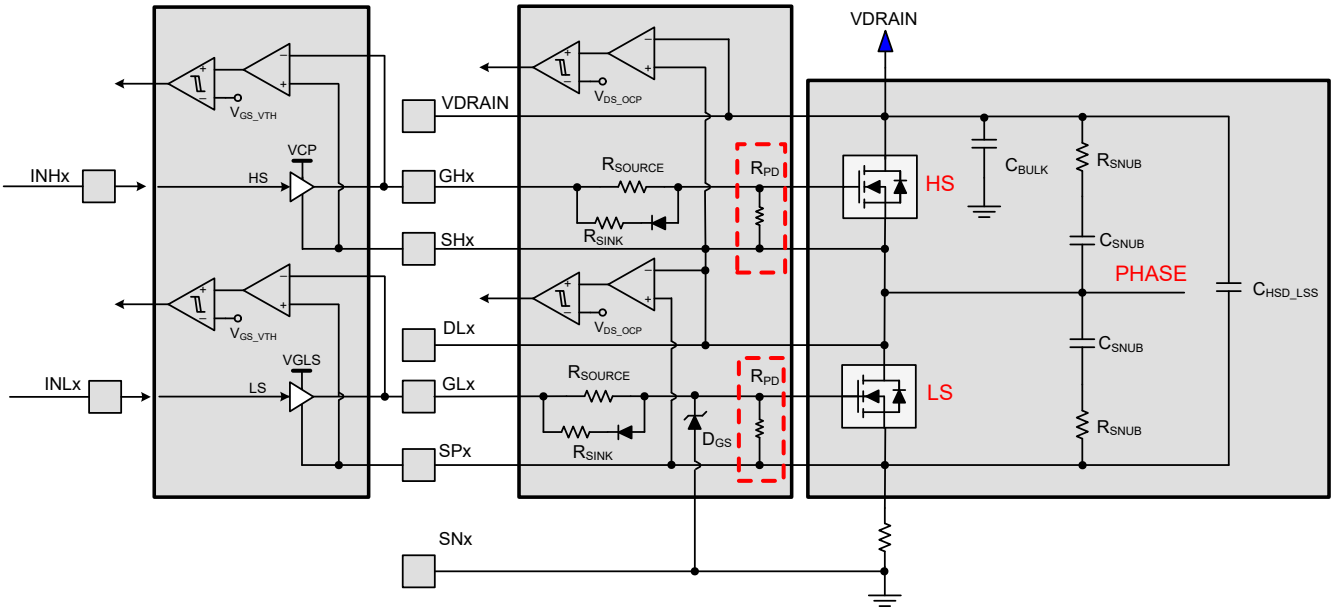

Figure 6-2. Example Passive Gate-to-Source Pulldown Resistors

The primary purpose of the passive pulldown resistor is to ensure that there is a known relationship between the gate and source if the gate driver fails. Specifically, if the gate driver is stuck in a sink or source current state, or if the gate driver goes into a high impedance state, the resistor ensures there is a path to keep the FET from conducting.

The passive gate-to-source pulldown resistors offer a path for the charge to equalize the gate and source voltages so the FET turns off more quickly. In reality, if the gate driver was damaged, some other protection or commutation logic circuit notices there is a problem, and the system detects it. The importance of these pulldown resistors is to make sure the shoot-through condition does not occur before other protection circuits can identify a problem has occurred. This is the difference between replacing the gate driver IC to fix the system and dealing with a melted motor, blown FETs, or irreversible damage to the PCB.

It is important to note that some gate drivers have passive, hundreds of kΩ pulldown resistors integrated into the device to fill this protective role. However, some designers might want a stronger pulldown located near the gate and source of the FETs so the charge at the gate does not need to travel through a potential gate resistor and inductive traces to equalize the gate and source voltage. Another benefit is that the external pulldowns have no

dependency on the gate driver which also helps in the context of adding redundancies to allow the system to fail in a known state.

As a final note, every pulldown resistor needs to be considered in the final power loss calculation. However, pulldowns usually contribute less than a milliwatt of total power dissipation which is much less than the tens of milliwatts produced by the $R_{DS(on)}$ or sense resistor. Remember that any current through these pulldown resistors must be accounted for when considering the capability of the VGLS, charge-pump, or bootstrap capability.

In summary:

- External passive pulldown resistors provide a path for charge at the gate-to-move to the source so that a FET can turn off if the active pulldowns fail
- These pulldowns range from tens of kilo-ohms to hundreds of kilo-ohms
- These external passive pulldowns contribute a lot less power dissipation compared to major sources of loss in a gate driver circuit
- Many gate drivers integrate the passive pulldown within the device

6.3 Power Supply Reverse Polarity or Power Supply Cutoff Protection

One danger that all electrical systems face is a reversed polarity from the power source. Several techniques are available to provide reverse battery protection when designing electrical systems, but all have the common purpose of preventing current flow when the battery terminals are connected in reverse. The theory and techniques are covered in the *Protecting automotive motor-drive systems from reverse polarity conditions* application note.

Additionally, some motor drive applications with high-current motors require power switches to get an alternative load turnoff path or to decrease quiescent current. Because the system output power is very high, discrete pass elements must be implemented. The methods for implementing the cutoff switch are discussed in the *Cut-Off Switch in High-Current Motor-Drive Applications* application note.

In summary:

- Prevent reverse battery and cutoff switches with a series diode, single MOSFET, or NMOS and BJT circuits
- There are cost, power dissipation, and PCB area tradeoffs between the different methods

7 High-Power Design Through Motor Control Methods

7.1 Brake versus Coast

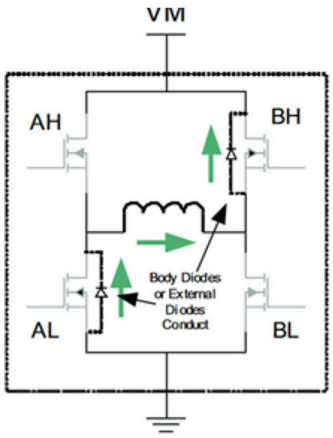

Figure 7-1. Example of Current Flowing Through Body Diodes During Coast Condition

Stopping or coasting a rotor already in motion is a typical use case that can cause problems for a high-power design. In this specific definition, coasting is when all of the high and low sides are turned off, which can be understood as floating the motor phases. Motors are partially inductive loads, so inductors attempt to resist changes in current by producing voltage to maintain current to flow in addition to the back EMF generated from the magnetic material of the rotor passing by the stator coils. As a result, the voltage at the motor phase rises higher than the voltage seen at the drain of the FET, which causes current to flow from the motor, through the body diodes of the FETs and into the supply over time during this coasting condition.

These spikes in voltage and the increased current out of the motor phases goes into the supply and increases the equivalent voltage at the FET drain to a higher value. As mentioned previously, the bulk capacitors absorb some or all of this energy, but the resulting rise in voltage can easily exceed absolute maximums for the gate driver if left unchecked as the bulk capacitors increase in voltage.

This actually occurs during the dead time of every PWM cycle, but the FETs stay in the coast state for such a short amount of time that the resulting energy usually does not move to the supply fast enough to cause damage. However, the increased voltage on the high-side source can be detected.

Luckily, this is avoided through motor control methods or external circuits, and the best practice is to have a plan to manage the energy stored up in the coils. Instead of coasting, implementing a braking control method or adding an external circuit is preferred.

7.1.1 Algorithm-Based Solutions

A general example of low-side braking is to turn off all high-side gates and turn on all low-side gates. This connects all motor phases to GND and allows current to cycle and collapse as the buildup of energy in the inductor flows in and out of GND. By using current sensing or VDS monitors, the designer determines when current has fully decayed and then releases the motor from the low-side braking state.

A general example of active braking is to oppose the current state of the motor by applying a PWM input to the opposite pairs of gates. For a more concrete example referencing Figure 7-1, imagine the high side of A is on and the low side of B is on. Active braking would PWM the low side of A and high side of B to force current from the supply to oppose the current stored up in the stator coils.

The same general concept is applied in the in the slow and fast decay modes covered in the *Current Recirculation and Decay Modes* application report in the context of stepper motors.

7.1.2 External Circuit Solutions

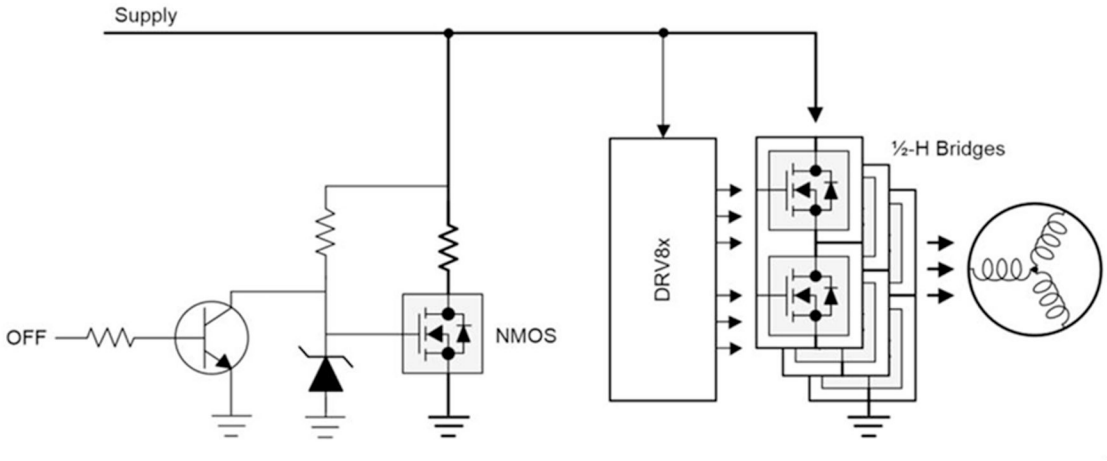

Figure 7-2. Example Active Brake Circuit

As previously mentioned, the bulk capacitors can absorb some or all of the energy generated by the motor, so increasing the number of capacitors or the value helps during the coast condition.

For an active approach, one solution is to add an external pulldown that controls power to the motor driver. This circuit provides a path to GND externally, dissipates the motor power, and prevents the voltage from rising on the high-side drain shown in Figure 7-2. This is popular for those who want system control external to the motor driver and not dependent on the gate drive stage to manage the external power generated by the motor. Because of the increased energy, the resistor and pulldown FET must be sized and rated for the wattage. In addition, some sort of feedback is needed to know when the voltage has risen too high; this is usually implemented with a voltage divider leading to the ADC of an MCU.

7.1.3 Summary of Brake versus Coast

In summary:

- Going into the coast state when the rotor is spinning can cause Back EMF to rise higher than the supply voltage and push current from the motor phases, into the high-side FET body diodes, and eventually into the supply. The increase in voltage can damage the gate driver.
- Have a plan to manage energy stored in the motor during the stop or coast condition by using a braking algorithm or external braking circuit

8 High-Power Design Through Layout

8.1 What is a Kelvin Connection?

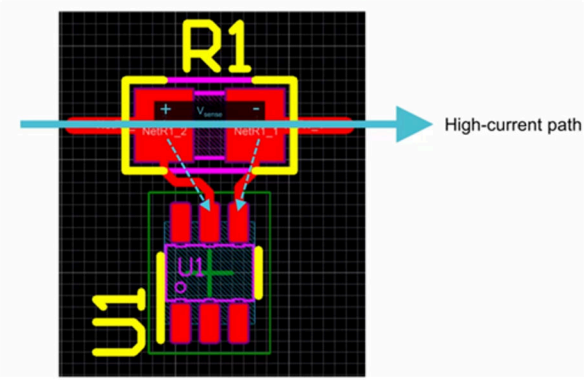

Figure 8-1. Example of a Good Kelvin Connection

A Kelvin connection is a precision electrical potential contact point with a current carrying path or reference point in such a way that contact resistance is reduced or eliminated. Conversely, imagine two traces on a PCB with the same electrical node. One trace is used for carrying current and the other is used only to sense the voltage. In a way, using a digital multimeter (DMM) to sense voltage across a component is the same theory as using a Kelvin connection.

This type of connection is frequently used when sensing current through external motor driver systems. The main motor current flows through the resistor path and the Kelvin connections are routed to the inputs of the CSA (SPx and SNx pins).

A full video training about Kelvin connections is found in the *TI Precision Labs - Current Sense Amplifiers: Shunt Resistor Layout* presentation.

In summary:

- Ensure there is a primary current path and primary sensing path
- Try minimizing length between the sense resistor and the sensing pins of the IC
- Try to keep the sensing paths of identical length and thickness to minimize errors between the signals. Differential routing helps here.
- Follow any recommendations provided by the landing pad of the shunt resistor used

8.2 General Layout Advice

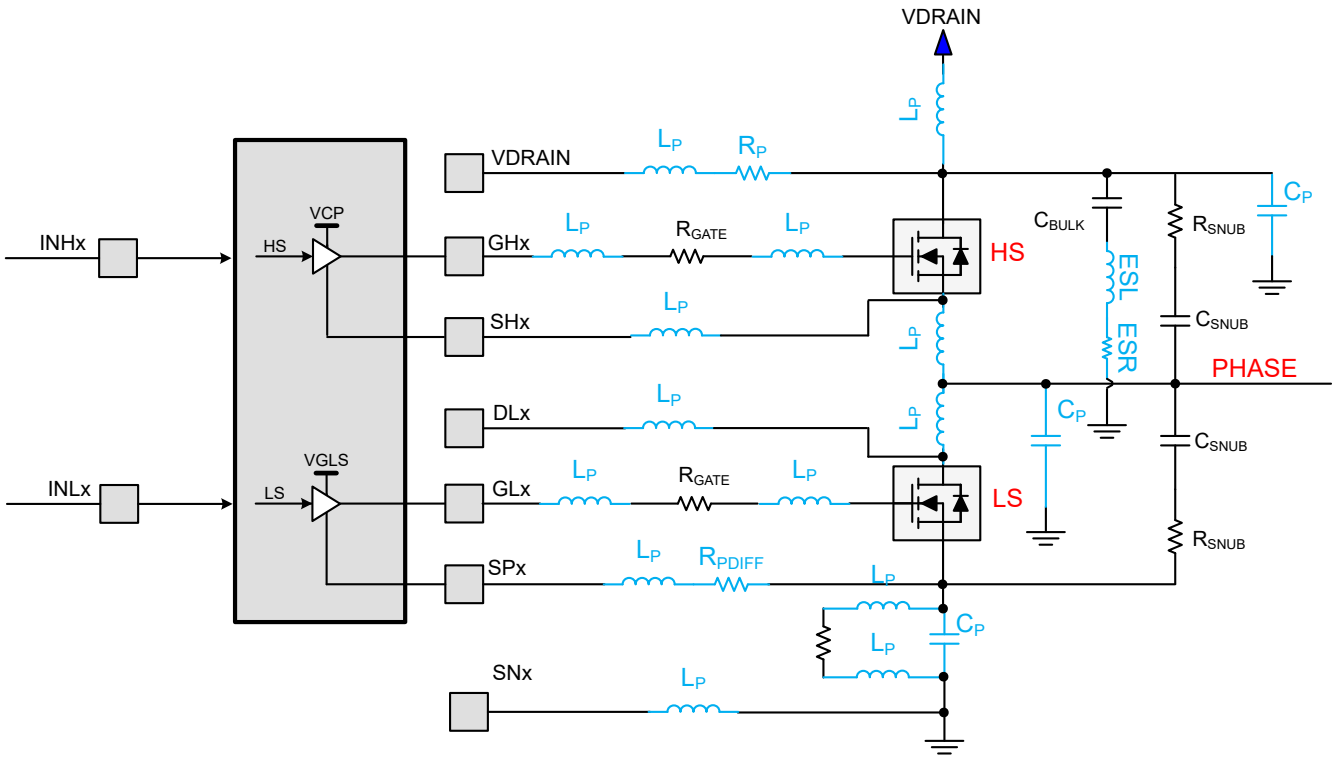

Figure 8-2. Example Smart Gate Drive Schematic Accounting for Parasitics

When PCBs are manufactured, physics dictates that some more resistors, inductors, and capacitors are added to the system. These added components are the result of parasitics - an example is illustrated in Figure 8-2.

One of the primary goals of layout is to minimize these parasitics so they are effectively negligible. What makes high power design difficult is that more current and voltage makes the effects of these parasitics more pronounced.

As a result, an entire application note has been devoted to *Best Practices for Board Layout of Motor Drivers*. It is highly recommended to read through the document in its entirety.

However, additional bullet points have been added here to help in the context of the high-power gate driver devices offered by TI:

- Actual PCBAs have parasitic components that are added to the system
  - Long traces add capacitance and resistance
  - Thin traces also add resistance and inductance
- 10 mil/A with 1-oz copper pour is a guideline for the trace width but it also applies to vias, specifically angular ring area. The larger or wider the traces and vias are, the less inductance.
  - As such, use at least 15 mil gate current source and sink paths, but 20 mil is preferred

Note

The 10 mil/A with 1-oz copper guideline starts to break and wider traces are required as a result of heat within the middle layers

- To get better thermal and current capability it is recommended to provide the VDC, motor phases, and GND power polygons in the external layers and, if possible, repeat the polygons in internal layers as well
- Making sections of a trace thinner and smaller in the same trace adds impedance mismatch
  - Use teardrops or planes to smooth out the mismatch
- More current means higher voltage spiking due to the parasitic effects
- Component footprints, in addition to the components, add parasitics
- Vias in the path add parasitics, namely inductance

- The return path must be understood:
  - DC current spreads out on the GND planes as far as it can go, whereas high-frequency current gravitates underneath the corresponding high-speed trace. This is why common GND, as opposed to split GND, is always better unless current needs to be diverted from flowing in a certain area of the board.
- Common ground is always better than split GND from a parasitic perspective. Split GND is only ever used to divert high-frequency current as well as large amounts of current away from the sensitive components. That means that these signals must be traveling towards or near those components to warrant a split GND.
  - If a split GND is chosen, then know inductance is added to some paths
- For additional understanding, imagine that you are the current: draw the loop from the source of the pin or component to the GND pin of the device or external connector. Make the loop as small as possible. This sometimes means adding lots of vias in the planes, increasing ground plane coverage, or rearranging components.
- Experience shows that the price difference between 100 and 300 GND stitching vias is negligible in PCB manufacturing. Create a plane of GND stitching vias to connect outer- and inner-layer GNDs.
  - Manually place GND stitching vias where the automated tools fail
- The most important signals and component locations on a typical gate driver IC are included in the following list, in descending order of importance:

1. Voltage regulators and their associated capacitors (like VCP, VGLS, or low-voltage regulators AVDD, DVDD, and so forth) (most critical)
2. Bypass capacitors for input supplies and reference voltages (like VM, GND, and CSAREF)
3. Signal path and higher current or power paths (like GHx, GLx, and SHx)
4. Digital signals that switch often, ordered by frequency (like SPI or PWM signals)
5. Digital signals that do not switch often (like ENABLE or nFAULT) (least critical)

9 Conclusion

While the example in Section 1.2 was generic, many issues are solved using this thought process. By analyzing the considerations for high power motor driver applications, we were able to plan ahead for problems that might have occurred and evaluated the functions of the gate driver to quickly identify what the problem was. This is the art of high-power design.

10 Acknowledgments

Cole Macias thanks Matt Hein, Adam Sidelsky, Prajkta Vyavahare (PV), Manu Balakrishnan, Nicholas Oborny, Anthony Lodi, and Aaron Barrera for their technical contributions and review during the creation of this application note.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265