Application Report

DiSEqC™ 2.x Filter Optimization

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ABSTRACT

The TPS65235 supports two way communications for receiver, controller and accessory, peripheral modes. Switching between receiver mode and accessory mode can lead to a voltage drop or negative spike in the V_{OUT} signal that can interfere with correct communication. This application note introduces the ways to handle the problem with theoretical analysis and practical results.

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1 Introduction

The DiSEqC™ 2.x protocol supports two way communications for receiver or controller and accessory or peripheral modes. Figure 1-1 shows a typical DiSEqC 2.x implementation using TPS65235.

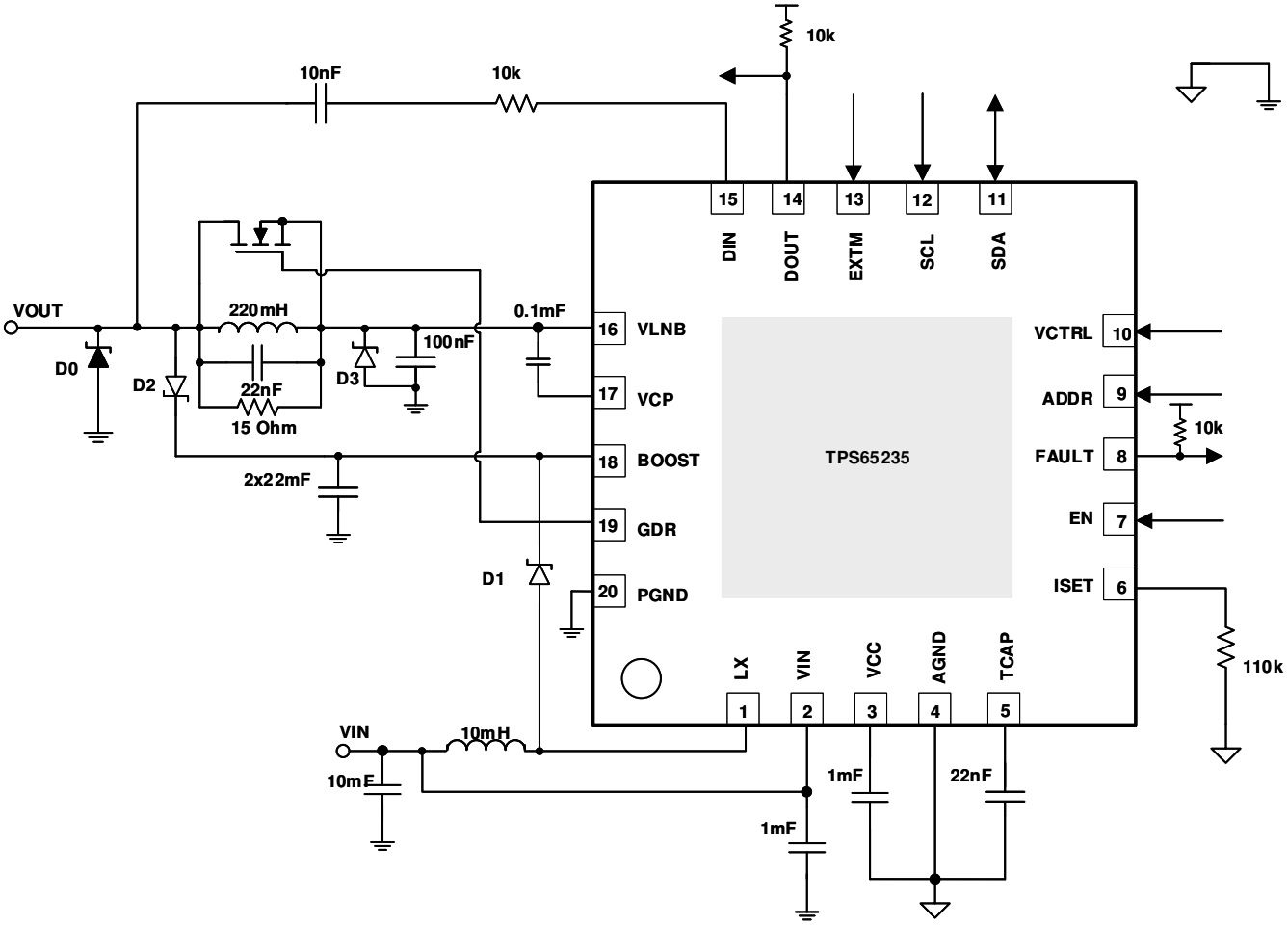

Figure 1-1. Typical DiSEqC™ 2.x Implementation

In accessory or peripheral mode a 22-kHz tone is received at V_{OUT}. The tone is blocked from reaching VLNB by the LCR filter. This is a band stop filter presenting 15-Ω impedance at 22 kHz. The tone is passed via the 10 nF, 10-kΩ RC filter to the DIN pin. The DC current for the LNB power flows from VLNB to V_{OUT} via the 220-µH inductor which has low DC resistance.

In receiver or controller mode, the LNB power supply transmits a 22-kHz tone on V_{OUT}. When transmitting, a FET is turned on to bypass the LCR filter and avoid unwanted attenuation of the 22-kHz tone. The lowest resistance DC path is through this FET when on. However, when the FET is turned off, the current cannot ramp instantly in the inductor and initially the current flows through the 15-Ω resistor. The voltage dropped across the resistor leads to a sudden drop or negative spike in the V_{OUT} signal, which subsequently decreases as the inductor current ramps. For a 600-mA LNB current, the drop across the resistor could be as high as 9 V but it is clamped at approximately 700 mV by the body diode of the FET as seen in Figure 1-2. This negative spike can be incorrectly interpreted by some LNBs and can lead to incorrect communication and missed commands.

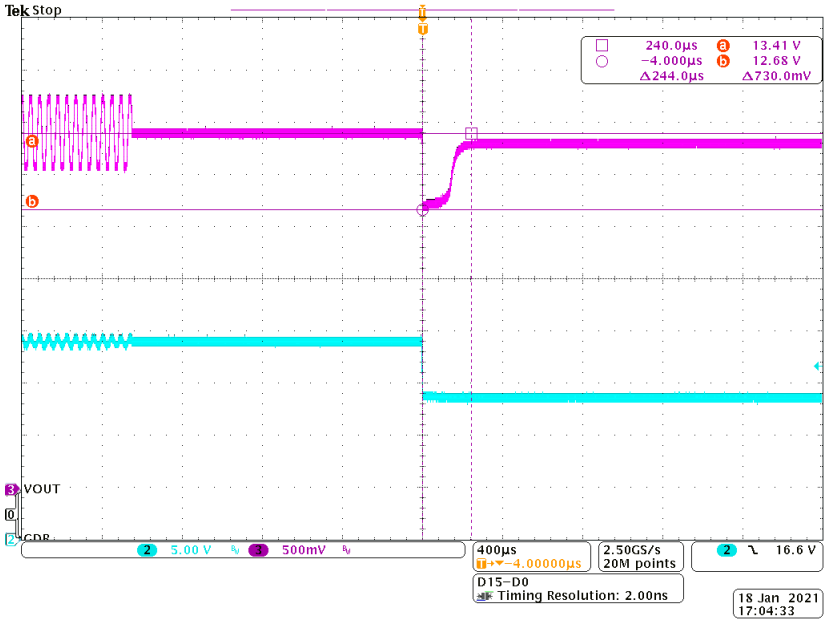

Figure 1-2. Negative Voltage Spike Clamped to Approximately 700 mV by FET Body Diode

2 Solutions

To avoid this negative spike, a couple of options are available. One is to add a Schottky diode across the FET as shown in Figure 2-1. This diode clamps the spike similar to the FET body diode, but with a lower forward voltage. Figure 2-2 shows the output with a B320A-13-F Schottky diode added. The spike is still present but is reduced to approximately 330 mV.

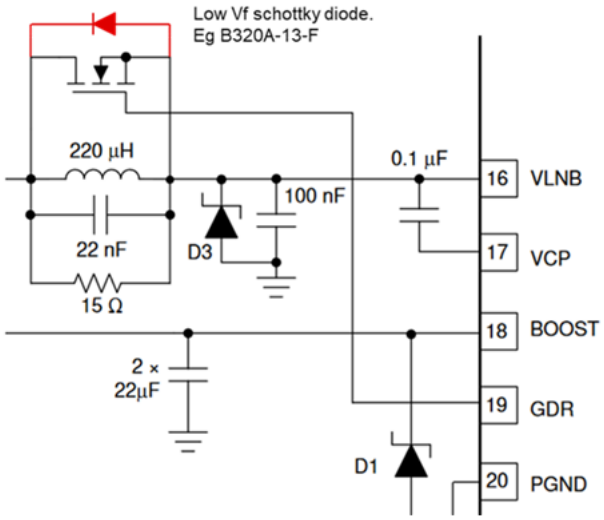

Figure 2-1. Schottky Diode Added to Clamp Negative Spike

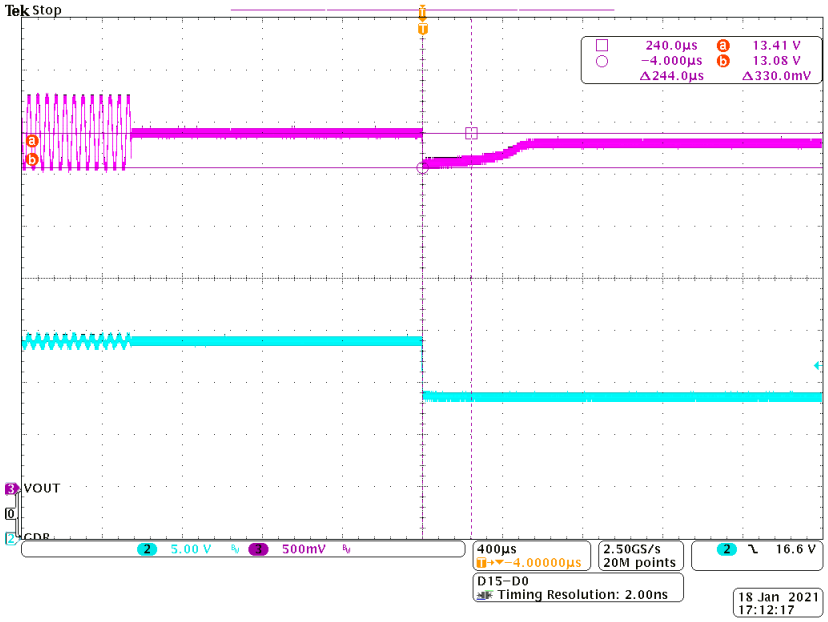

Figure 2-2. Spike Clamped to Approximately 330 mV by Adding Schottky Diode Across the FET

Another solution is to add a DC blocking capacitor in series with the FET as shown in Figure 2-3. In this way, when the FET is turned on, the 22-kHz tone passes through the capacitor whose impedance is approximately 330 mΩ at 22 kHz. However, the DC current is blocked and continues to flow via the inductor. So when the FET is turned off there is no change in the DC current flow and no negative spike is generated (Figure 2-4). A 22-µF, 25-V with 0805 capacitor was used for this test, but similar results were achieved with a 10-µF, 25-V capacitor. In normal working conditions, the voltage across the capacitor is less than 2 V but, as the output may be subjected to surges, a 25-V rated capacitor is recommended.

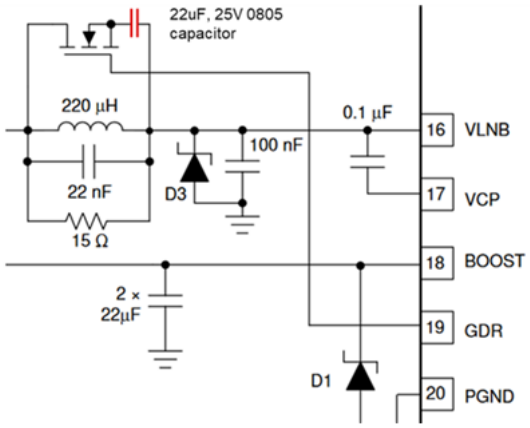

Figure 2-3. DC Blocking Capacitor Added in Series With FET

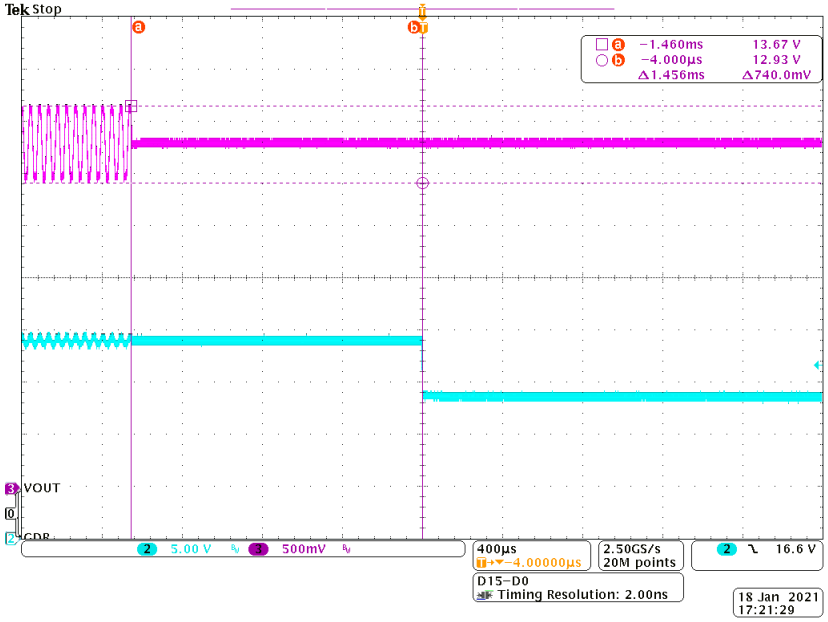

Figure 2-4. Inserting a 22-µF Blocking Capacitor Removes the Negative Spike Entirely

3 Theoretical Analysis

Figure 3-1 shows the equivalent circuit of the typical implementation, where V_{LNB} is the output voltage of V_{LNB} pin and it is equivalent to a voltage source supplying to the LRC network and the load resistor R_o. V_o is the output voltage, i_o is the load current, i_{sw} is the current of the FET and V_{sw} is the voltage drop across the FET.

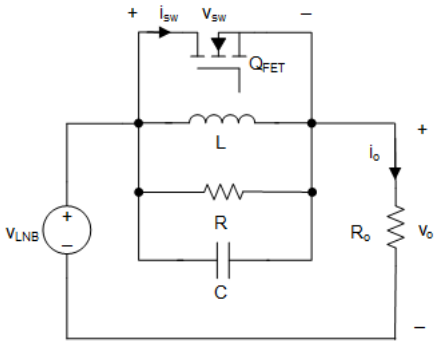

Figure 3-1. Equivalent Circuit of DiSEqC™ 2.x Implementation

To reflect the attenuation of data transmission, the transfer function of V_o to V_{LNB} is defined as follows in Equation 1

$$G(s) = \frac{v_o(s)}{v_{LNB}(s)} \tag{1}$$

When the FET is on, assuming all component are ideal, then $i_{sw} = i_o$ and $V_o = V_{LNB}$. Therefore, G(s) = 1, which means there is no attenuation of the 22-kHz tone.

When the FET is off, $i_{sw} = 0$, the tone signal is attenuated due to LCR network. And G(s) can be expressed as Equation 2.

$$G(s) = \frac{R_o}{R_o + Z(s)} \tag{2}$$

Where Z(s) can be expressed as Equation 3:

$$Z(s) = \frac{1}{\frac{1}{R} + sC + \frac{1}{sL}} \tag{3}$$

Hence the attenuation of 22-kHz tone can be expressed as Equation 4:

$$A(22kHz) = 20\log|G(j22k \times 2\pi)| = -4.459dB \tag{4}$$

Figure 3-2 shows the simulation waveforms of the equivalent circuit, where GDR is the gate drive signal of the FET. It can be seen from the waveforms that there is no attenuation of the tone signal when FET is on, and when the FET is off, the attenuation of 22-kHz tone is –4.437 dB.

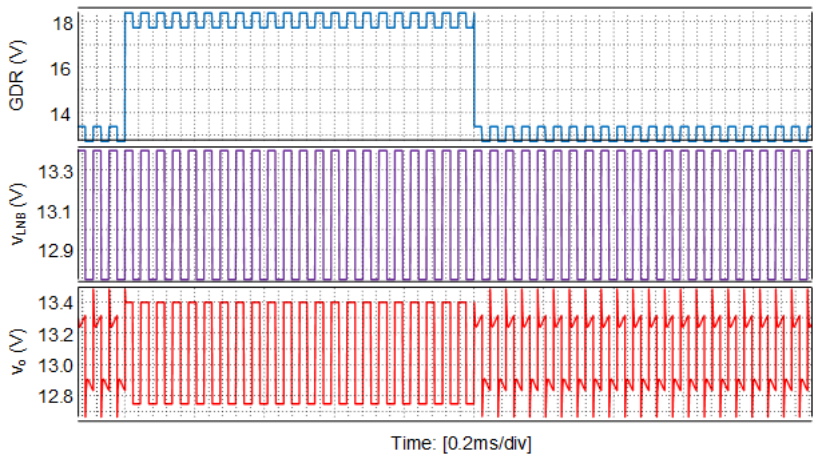

Figure 3-2. Simulation Waveforms of DiSEqC™ 2.x Implementation

In practice, when the 22-kHz tone ends, V_{LNB} is a constant voltage, but the FET will not turn off at once. So there is a constant current flowing through the FET and $i_{sw} = i_o$. After a fixed delay time t_{delay}, the FET turns off and $i_{sw} = 0$. The switching action causes a current transient ΔI_{sw} to the FET path. At the moment the FET turns off, there will be a voltage drop across the FET due to the current transient. To better understand, the control circuit of the typical implementation can be represented by the blocks in Figure 3-3 based on Figure 3-1.

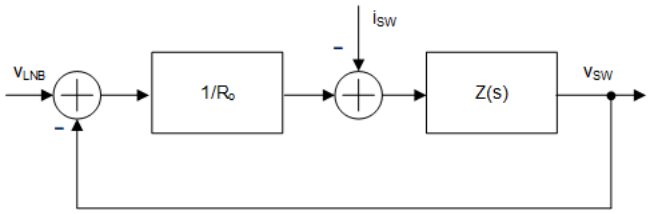

Figure 3-3. DiSEqC™ 2.x Implementation Control Circuit

The transfer function of $V_{sw}(s)$ to $i_{sw}(s)$ can be generated as Equation 5:

$$G_{vi}(s) = \frac{v_{SW}(s)}{i_{SW}(s)} = \frac{Z(s)}{1 + \frac{Z(s)}{R_o}} \tag{5}$$

The inverse Laplace transform of Equation 5 allows the voltage to be expressed as Equation 6.

$$v_{SW}(t) = \frac{1}{C(x_1 - x_2)}(e^{x_1 t} - e^{x_2 t})\Delta I_{SW} \tag{6}$$

where: x_1 and x_2 can be expressed as Equation 7 and Equation 8.

$$x_1 = \frac{-\frac{R_o + R}{R_o RC} + \sqrt{(\frac{R_o + R}{R_o RC})^2 - \frac{4}{CL}}}{2} \tag{7}$$

$$x_2 = \frac{-\frac{R_o + R}{R_o RC} - \sqrt{(\frac{R_o + R}{R_o RC})^2 - \frac{4}{CL}}}{2} \tag{8}$$

The maximum value of the voltage drop can be calculated at the extremum point t_{EP} when the derivative of $v_{sw}(t)$ equals 0, and can be expressed as Equation 9:

$$\frac{dv_{SW}(t)}{dt} = \frac{1}{C(x_1 - x_2)} \frac{d(e^{x_1 t} - e^{x_2 t})}{dt} \Delta I_{SW} \tag{9}$$

According to Equation 9, t_{EP} becomes Equation 10:

$$t_{EP} = \frac{lnx_1 - lnx_2}{x_2 - x_1} \tag{10}$$

Considering that R_o = 22.3 Ω, so ΔI_{sw} = 0.6 A, then $V_{sw\_dropmax}$ can be expressed as Equation 11:

$$v_{SW\,dropmax} = 4.6V\ @0.6A\ transient \tag{11}$$

Figure 3-4 shows the simulation results of the voltage drop across the FET, and it can be found that $V_{sw\_dropmax}$ = 4.59 V.

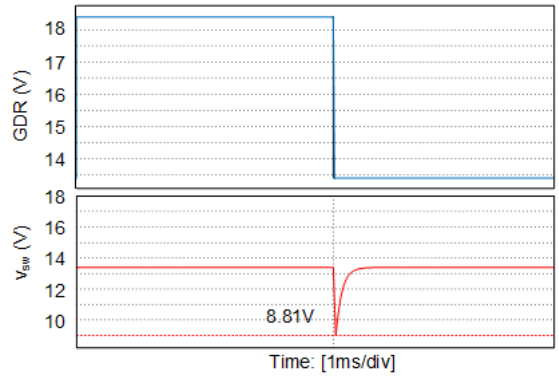

Figure 3-4. Simulation Waveforms of Voltage Drop in DiSEqC™ 2.x Implementation

However, in practice, the voltage drop is clamped by the V_f of body diode of the FET. So the voltage drop V_{sw_drop} = min[V_f, $V_{sw\_dropmax}$].

As previously described, adding a capacitor in series with the FET blocks the DC current path. The DC current flows continuously in the inductor and there is no transient dip when the FET is turned off. Figure 3-5 shows the equivalent circuit with the added capacitor.

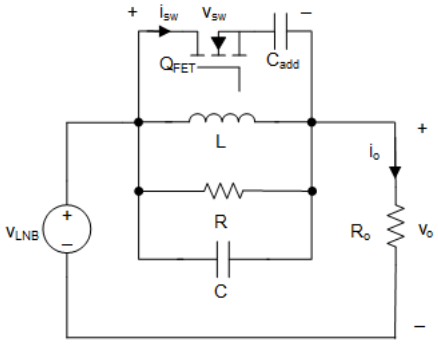

Figure 3-5. Equivalent Circuit of DiSEqC™ 2.x Implementation With C_{add}

The value of the capacitor will affect the attenuation of 22-kHz tone when FET is on, and G(s) will be changed as Equation 12:

$$G(s) = \frac{R_o}{R_o + Z_1(s)} \tag{12}$$

where $Z_1(s)$ can be expressed as Equation 13:

$$Z_1(s) = \frac{1}{\frac{1}{R} + s(C + C_{add}) + \frac{1}{sL}} \tag{13}$$

Hence the attenuation of the 22-kHz tone can expressed as Equation 14:

$$A(22kHz) = 20\log|G(j22k \times 2\pi)| \tag{14}$$

Based on Equation 14, C_{add} can be selected to meet the maximum attenuation. For example, if the amplitude of 22-kHz tone is 650 mV, and maximum attenuation is 100 mV, then C_{add} of at least 1 µF is required. Figure 3-6 shows the experimental results for 1-µF C_{add}. Results for a 22-µF C_{add} have already been seen in Figure 2-4.

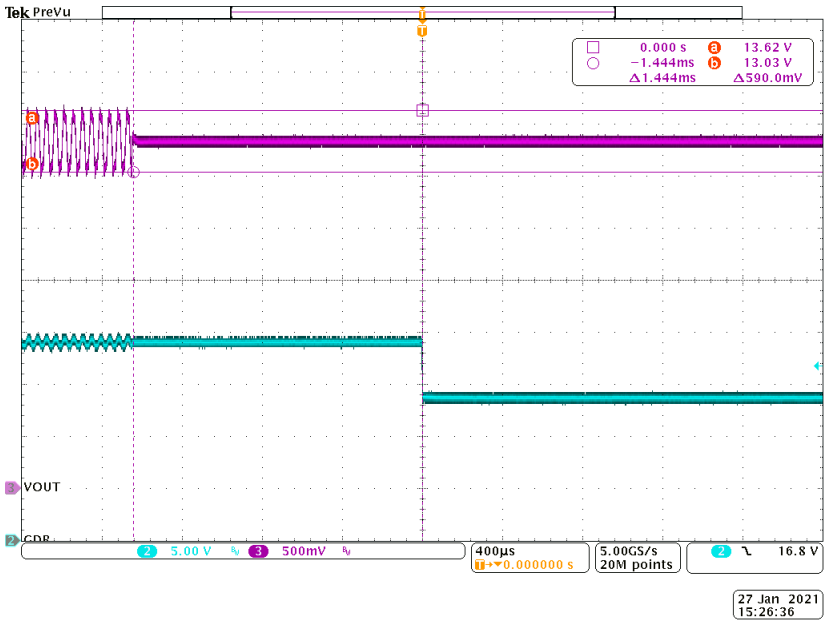

Figure 3-6. Experimental Results of DiSEqC™ 2.x Implementation With C_{add}

4 Summary

In a DiSEqC 2.x system, switching between receiver or controller mode and accessory or peripheral mode can lead to a voltage drop or negative spike in the V_{OUT} signal that can interfere with correct communication. Adding a Schottky diode in parallel with the LCR filter and bypassing FET reduces this voltage spike. Adding a capacitor in series with the bypass FET eliminates the voltage spike. Both solutions avoid unnecessary attenuation of the transmitted tone in receiver mode. Theoretical analysis of the equivalent circuit corroborates the practical results.

5 References

- Texas Instruments, *DiSEqC™ Protocol and Low-Noise Block Voltage Regulator TPS65235 for Satellite – STB/TV Application Report*
- Texas Instruments, *TPS65235 LNB Voltage Regulator With I2C Interface Data Sheet*
- Texas Instruments, *TPS652353 LNB Voltage Regulator With I2C Interface Data Sheet*
- Texas Instruments, *TPS65235-1 LNB Voltage Regulator With I2C Interface Data Sheet*

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