

Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter



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ABSTRACT

The *Powering the AFE7920 with the TPS62913 Low-Ripple and Low-Noise Buck Converter* application report includes the following information:

- The noise sensitive 1.8 V Analog rails of the AFE7920 are supplied using the TPS62913 switching regulators without the need for low-dropout linear regulators (LDOs) while maintaining the same performance as the original design. The LMK04828 can also be supplied by the TPS62913, but is not shown on in this application note.
- The power supply design demonstrates a simplified and efficient implementation of the TPS62913 low ripple and low noise buck converter to power the 1.8-V noise sensitive analog rails, reducing the solution size and increasing the efficiency to 90.7% compared to the traditional DC/DC + LDO efficiency of 73.5%. This efficiency increase saves 1.24W for the 1.8 V rails, a power savings of 19%.
- The design is applicable to the AFE79xx and other AFEs that require low noise power supplies that are size constrained and thermal constrained. Examples of applications are remote radio units (RRU), active antenna systems (AAS), distributed antenna systems (DAS), small cell base stations, and repeaters.
- Included is an AFE79xx description and overview of the EVM modifications to use a switching supply only, without the need for LDOs.
- The digital core power rails of 0.9-V and 1.2-V rails are powered by the TPS541620 dual 6 A converter, enabling smaller solution size by having a dual supply converter, and increasing the switching frequency to 1 MHz.
- Key measurement results showing comparable performance to the previous implementation.

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1 Introduction and System Description

1.1 Introduction

High speed RF sampling converters often include integrated PLL/VCO to supply the high frequency sampling clock. The integrated clock, such as the one included in the AFE7920, is sensitive to power supply spurs and noise. Any degradation on the clock from the power supply directly impacts the data converter performance. The most common solution to minimize that noise is to use linear power supplies, or a DC-DC converter from the main bus rail followed by a low dropout regulator. Compared to a linear supply, there are two big advantages of being able to use a DC-DC converter alone: the reduction in power loss and the size of the power supply. To use a DC-DC converter alone requires careful consideration of the switching supply selected, as well as the design and layout of the DC-DC converter. However, with the TPS62913, it is possible to achieve the desired results of the same performance as a traditional design using LDOs but with lower power dissipation and smaller board space.

This application note uses the AFE7920 as an example of a high performance RF sampling transceiver where the 1.8 V supplies have been changed from a DC-DC converter+LDO approach to a DC-DC converter-only approach. This methodology can be used for many other noise sensitive applications as well. The TPS62913 low-ripple and low-noise buck converter used in this application note is specifically designed to help engineers design power supplies that meet the noise and ripple requirements for noise sensitive applications.

1.1.1 AFE79xx Noise and Ripple Requirements

The AFE79xx is a family of high performance, wide bandwidth multi-channel transceivers, integrating four RF sampling transmitter chains, four RF sampling receiver chains, and up to two RF sampling digitizing auxiliary chains (feedback paths). The high dynamic range of the transmitter and receiver chains allows the device to generate and receive 3G, 4G, and 5G signals from wireless base stations, while the wide bandwidth capability of the AFE79xx devices is designed for multi-band 4G and 5G base stations.

The original product evaluation module (EVM) implements low-noise LDOs in addition to the DC-DC buck regulators on the noise sensitive 1.8 V supply rails to minimize any impairments from the supply network. While the DC accuracy of the supply rail is specified for the AFE79xx, there is no specification on supply voltage noise and supply voltage ripple. Any supply ripple or noise appears attenuated on the output spectrum of the ADC. This attenuation can be expressed as Power Supply Rejection Ratio (PSRR) and PSRR_{MOD} (or PSMR) as shown in Figure 1-1.

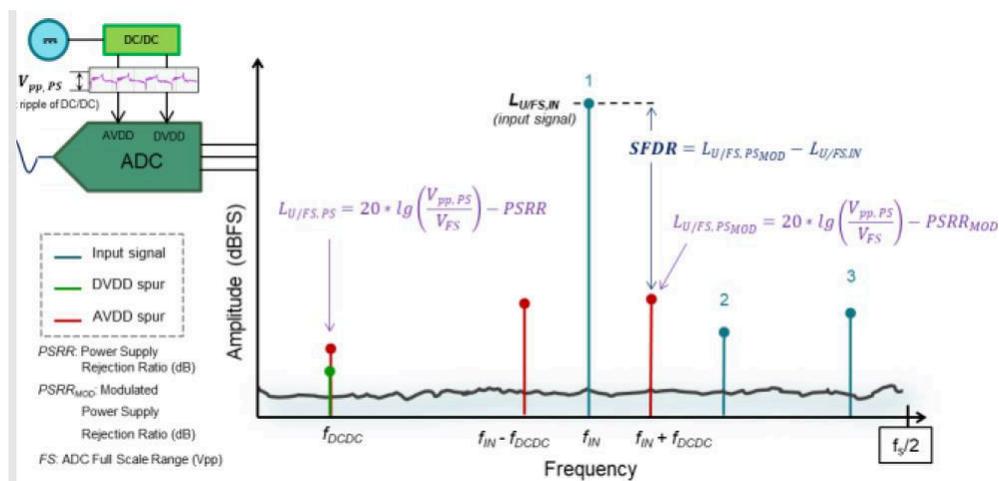


Figure 1-1. Power supply noise and ripple in the ADC output spectrum

PSRR is the attenuation of the ADC input supply ripple to the ADC output spectrum at the switching frequency fundamental of the DC-DC converter (f_{DCDC}). PSRR_{MOD} (or PSMR) is the attenuation from the ADC input to the modulated spur in the output spectrum ($f_{in} - f_{DCDC}$, $f_{in} + f_{DCDC}$).

1.1.2 TPS62913 Low-Noise and Low-Ripple Buck Converter

The TPS62912 and TPS62913 devices are a family of high-efficiency, low-noise and low-ripple synchronous buck converters. The devices are ideal for noise sensitive applications that would normally use an LDO for post regulation such as AFEs, high-speed ADCs, Clock and Jitter Cleaner, Serializer, De-serializer, and Radar applications. The device operates at a fixed switching frequency of 2.2 MHz or 1 MHz, and can be synchronized to an external clock. To further reduce the output voltage ripple, the device integrates loop compensation to operate with an optional second-stage ferrite bead L-C filter. This allows an output voltage ripple below 10 μ V_{RMS}. Low-frequency noise levels, similar to a low-noise LDO, are achieved by filtering the internal voltage reference with a capacitor connected to the NR/SS pin. The optional spread spectrum modulation scheme spreads the DC/DC switching frequency over a wider span, which lowers the mixing spurs.

1.1.3 TPS541620 Dual 6A Converter

The TPS541620 is a high-efficiency, fixed frequency, dual 6-A output buck converter. This device is ideal for applications where board space is limited. The two outputs switch out-of-phase to minimize the conducted noise generated on the input. The device uses Advanced Current-Mode (ACM) Control to simplify compensation and to allow for a low minimum on-time enabling high switching frequency in low duty cycle applications. For example, it is capable of operating at 1-MHz switching frequency in a 12-V input to 0.9-V output application. The device can also be synchronized to an external clock to provide more control over the noise generated in the power supply design. The low output ripple needed for the 0.9V and 1.2V rails in this design is achieved with passive filtering only. Lastly, the two 6-A outputs can also be combined to drive a single 12-A load.

1.2 Block Diagram

The original AFE7920 RevC evaluation module used a DC-DC converter with LDO followers to provide power to the AFE 1.8 V rails.

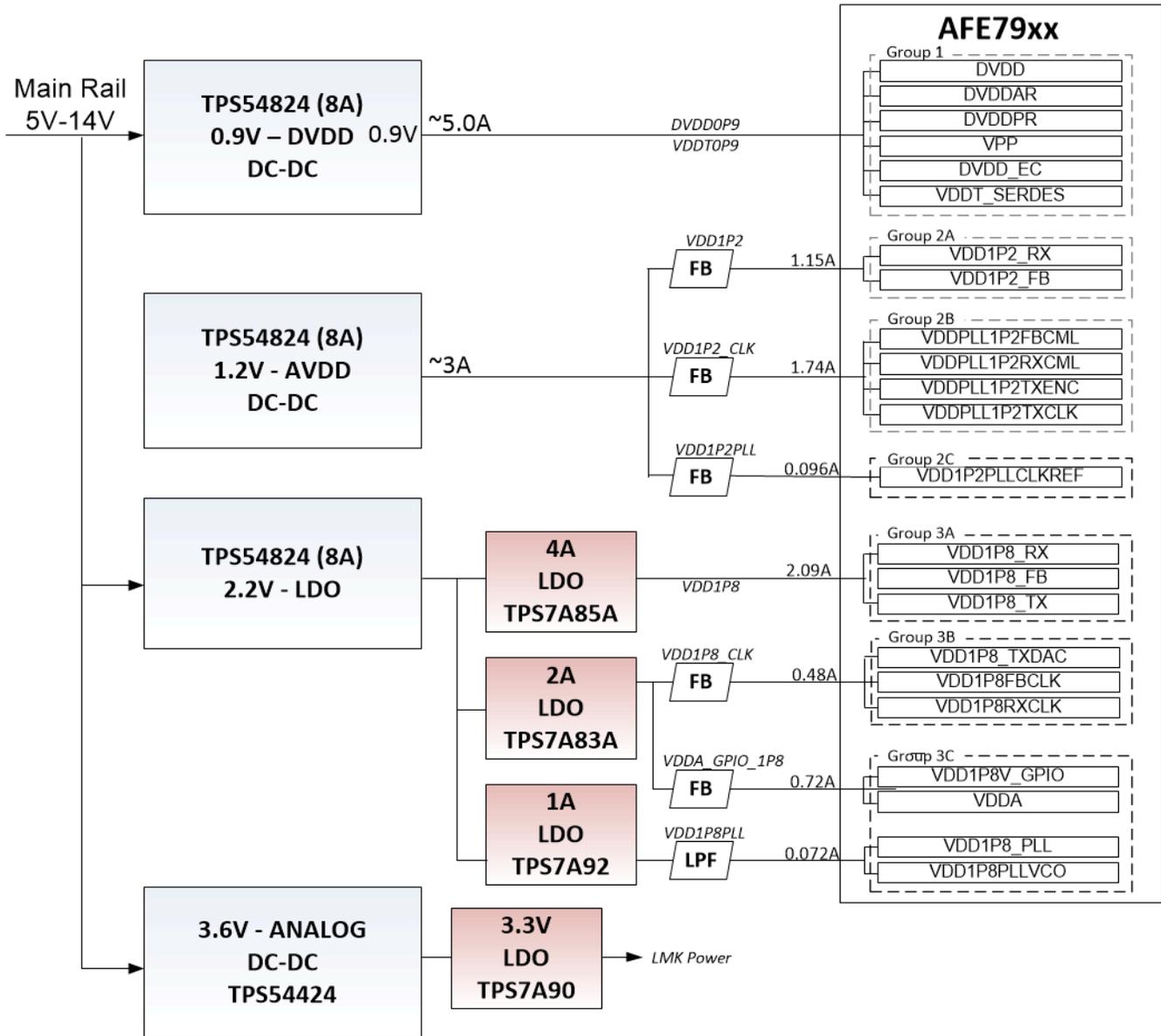


Figure 1-2. Original Power Block Diagram for AFE7920 RevC Evaluation Module

The original EVM power supply is outlined in blue and shown in [Figure 1-3](#). The DC/DC and LDO's consume a large amount of the board area in this design, and uses two sides of the board.



Figure 1-3. Image of top of Original board with Switchers and LDO's outlined in Blue

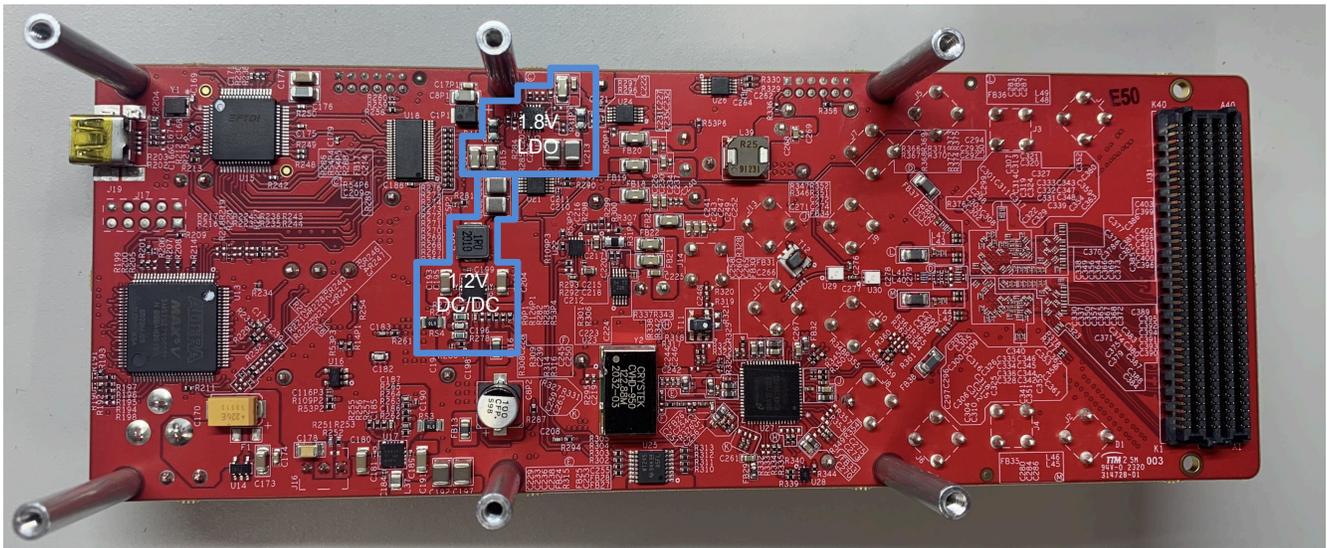


Figure 1-4. Image of bottom of Original board with Switchers and LDO's outlined in Blue

In the revised design, the LDOs are removed for the 1.8 V rails, and the TPS62913 low-ripple, low-noise DC-DC converter is used instead. This implementation improves the efficiency (reducing power loss), reduces temp rise, and reduces the part count in comparison to a solution using LDOs while maintaining the output voltage ripple and noise requirements of the AFE for good performance.

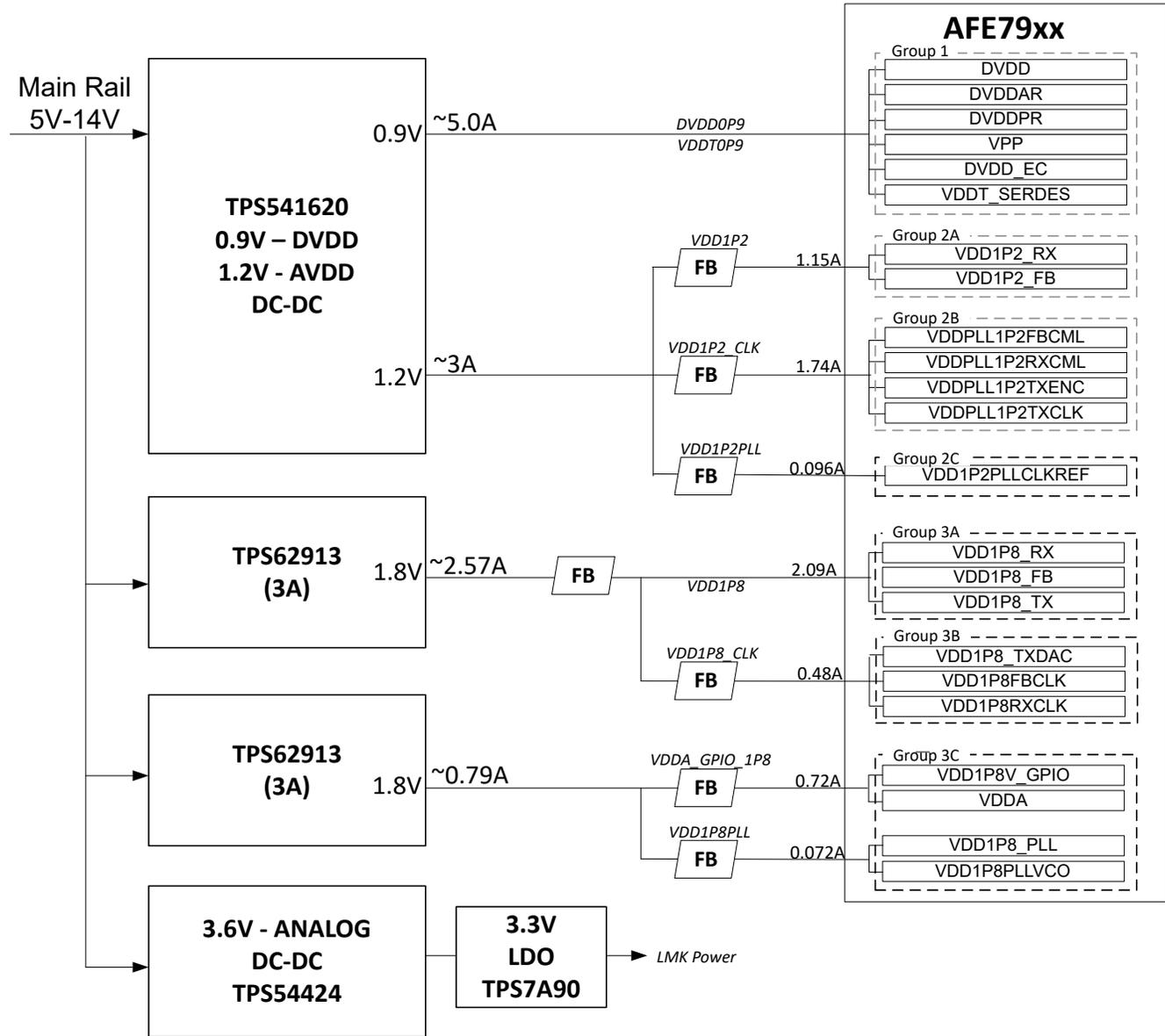


Figure 1-5. Power Block Diagram for AFE7920 Rev C Evaluation Module with TPS62913

The updated EVM power supply with the TPS62913 and dual output TPS541620 is outlined in blue and shown in [Figure 1-7](#). The DC/DC solution size is considerably smaller in this design, and is on a single side of the board.

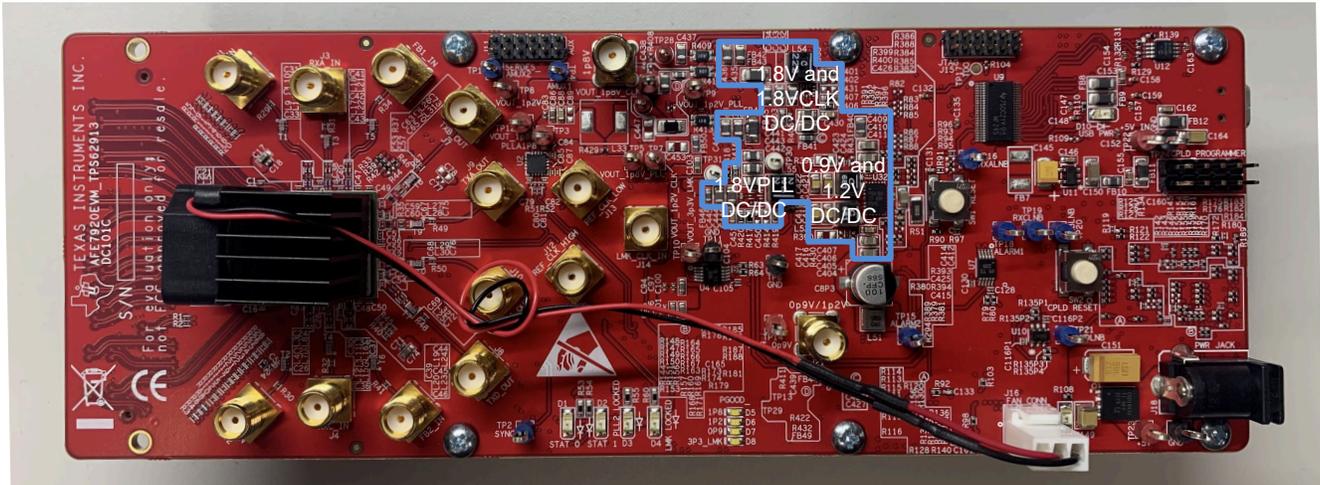


Figure 1-6. Image of top of Revised board with TPS541620 and TPS62913 Switchers outlined in Blue

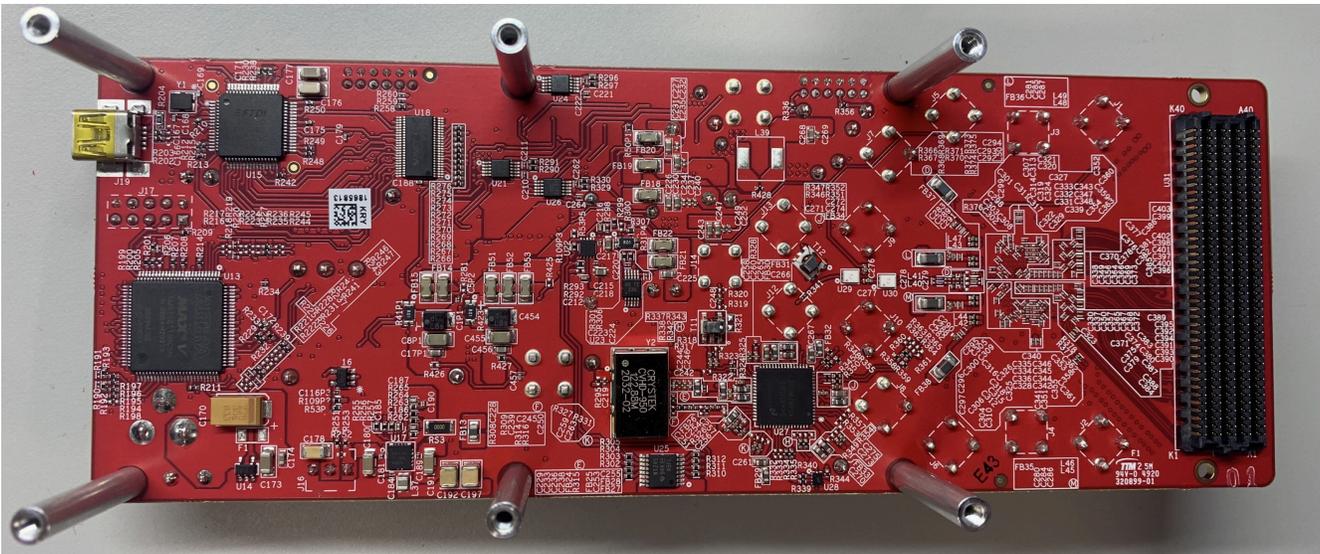


Figure 1-7. Image of bottom of Revised board

The schematics for the 1.8 V rails can be found in the [Schematic](#).

Table 1-1. AFE7920 Evaluation Module Component Comparison

Component	Original Rev C	Rev C with TPS62913
Switching Power Supplies	1 x TPS54824 (3.5mm x 3.5mm)	2 x TPS62913 (2mm x 2mm ea)
LDO's	1 x TPS7A85A 4A LDO (3.5mm x 3.5mm), 1 x TPS7A83A 2A LDO (3.5mm x 3.5mm), 1x TPS7A92 1A LDO (2.5mm x 2.5mm)	None
Size of Power Supplies	43 sqmm + passives	8 sqmm + passives

1.3 Design Considerations

The AFE79xx is a high performance multi giga-sample per second (GSPS) AFE and is sensitive to noise and spurious contents that result from high current in the switching elements, output capacitor ESL, and the magnetics involved when using a standard DC-DC converter. Utilizing the TPS62913 low-ripple, low-noise converter enables a significant reduction in noise and ripple without using a post-regulation LDO through the converters' unique low-ripple and low-noise design features.

The converter's analog and clock inputs often get most of the scrutiny when it comes to addressing low noise on their inputs. Keep in mind that power supplies are inputs too. Because we think of them as DC biasing circuits we often don't think of them as affecting RF performance. However, this is not true. Spurious performance is dependent on the layout structure. The DC-DC converters generate switching spurs which can be large. Switching spurs infiltrate unwanted circuits via conducted paths or radiated paths. Conducted spurs are mitigated with the ferrite bead isolation, supply filtering, and adequate low frequency bypass capacitors. Radiated emissions are more difficult to control.

The primary location for radiated emissions is right at the DC-DC converter itself and the switching inductor. Since the switching spurs are large in amplitude and at low frequency, localized shielding or PCB ground planes do little to attenuate the spurs. Switching spurs penetrate ground planes easily and infect internal, sensitive power traces. As such, keep sensitive routing from running on an internal layer directly underneath the DC-DC converter. Further, no other board with sensitive internal nets should be placed directly above or below. Even physical spacing as much as 1 inch is not sufficient to reduce the spurious coupling. Instead, the DC-DC converters should be offset from any sensitive area or other boards so that there is nothing directly above or below the converters that will be contaminated by switching spurs. When designing power supply domains for any high-speed converter, here are some useful tips in maximizing power supply noise immunity:

- Decouple all power supply rails and bus voltages as they come onto the system board near the AFE itself.
- Remember that approximately 20 dB/decade noise suppression is gained for each additional filtering stage.
- Decouple both high and low frequencies, which might require multiple capacitor values.
- Series ferrite beads are commonly used at the power entry point just before the decoupling capacitor to ground. This should be done for each individual supply voltage coming into the system board regardless of whether it comes from an LDO or switching regulator.
- For added capacitance, use tightly stacked power and ground plane pairs (≤ 4 mil spacing). This adds inherent high-frequency (>500 MHz) decoupling to the PCB design.
- Keep supplies away from sensitive analog circuitry such as the front-end stage of the AFE and clocking circuits if possible.
- Some components could be located on the opposite side of the PCB for added isolation.
- Follow the IC manufacture recommendations; if they are not directly stated in the application note or data sheet, then study the evaluation board. These are great vehicles to learn from.

Applying these points above can help provide a solid power supply design yielding datasheet performance in many applications.

2 Tests and Results

2.1 Test Methodology

Signal-to-Noise Ratio (SNR, dBFS)

The SNR is the ratio of the rms signal amplitude to the rms value of the sum of all spectral components excluding DC, HD2 to HD9, $f_s / 2$, $f_s / 2 - f_{IN}$. The difference between SNR (dBc) and SNR (dBFS) is the difference between the fundamental amplitude and full scale.

Phase Noise (dBc/Hz)

The phase noise parameter measures the frequency noise or jitter that is related to the sampling clock. Phase noise measurement sweeps from a very low frequency offset (~100 Hz) out to over 10 MHz relative to the carrier frequency. This measurement examines low frequency spurious and noise that may come from the clock or the power supply at the transmitter output.

Harmonic Distortion (dBc or dBFS)

A harmonic is a spectral component that is an integer multiple of the driven analog input frequency. For example, the frequency of the second harmonic is twice the analog input. Most ADCs have specifications for one or more harmonics. Typically, the second and third harmonics are singled out because they account for the worst performance of all the harmonics. Harmonic distortion, no matter the order, is the ratio of the rms signal amplitude to the rms value of the specified harmonic component, reported in dBc or dBFS. ADCs are nonlinear devices, therefore output FFT captured will be rich in spectral components.

Spurious-Free Dynamic Range (SFDR, dBc or dBFS)

The SFDR is the ratio of the rms value of the signal to the rms value of the peak spurious spectral component for the analog input frequency that produces the worst result. In most cases, SFDR is either the second or third harmonic (HD2 or HD3) of the input signal applied to the ADC. SFDR is intended to capture the spurious performance and not be inadvertently misled by spectral content close in to the carrier due to the phase noise spread. As such, in many of the FFT plots a handful of bins around the fundamental are notched so that the true highest spur is captured.

Noise Spectral Density (NSD, dBFS/Hz)

The NSD is defined the entire noise power, per unit of bandwidth, sampled at an ADC's input. NSD is effectively the ADCs' SNR plus the power of the noise spread across the entire Nyquist band, which is equal to half the sample frequency, or $f_s/2$. Therefore, $NSD = SNR + 10 \cdot \log(f_s/2)$.

For a visual description of how to read SNR, SFDR, Harmonic Distortion, and NSD, refer to [Figure 2-1](#).

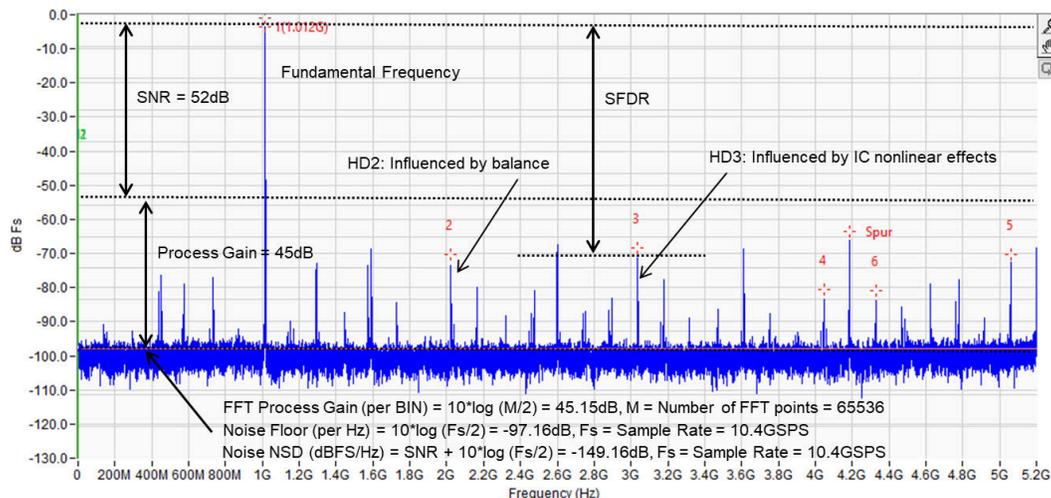


Figure 2-1. FFT showing SNR, SFDR, NSD, and Harmonic Distortion

2.2 Test Conditions

The original design and the new design with the TPS62913 were tested in identical conditions for comparison. The input supply is 5.6 V nominal, and the ambient temperature is 25 C nominal. The transmit and receive specifics are detailed in the test results.

2.3 Test Results

Performance tables and graphs comparing the original AFE7920 Original EVM with the TPS541620/TPS62913 modified board are shown below.

RX (Receive) SNR and SFDR

The FFT spectral plot is shown for an input frequency of 3.51 GHz, NCO of 3.5 GHz, and notch of 150. [Figure 2-2](#) shows the performance of the standard EVM compared with the TPS541620/TPS62913 board. No close-in spurious on either board. The SNR and SFDR performance between the two units is roughly the same; however, the TPS541620/TPS62913 board achieves slightly better very close-in noise as shown in the spectrum close to the carrier as shown by the phase noise spread. The original board achieved -50dBFS, where the TPS541620/TPS62913 board achieved -62 dBFS, which shows improved performance with the new design.

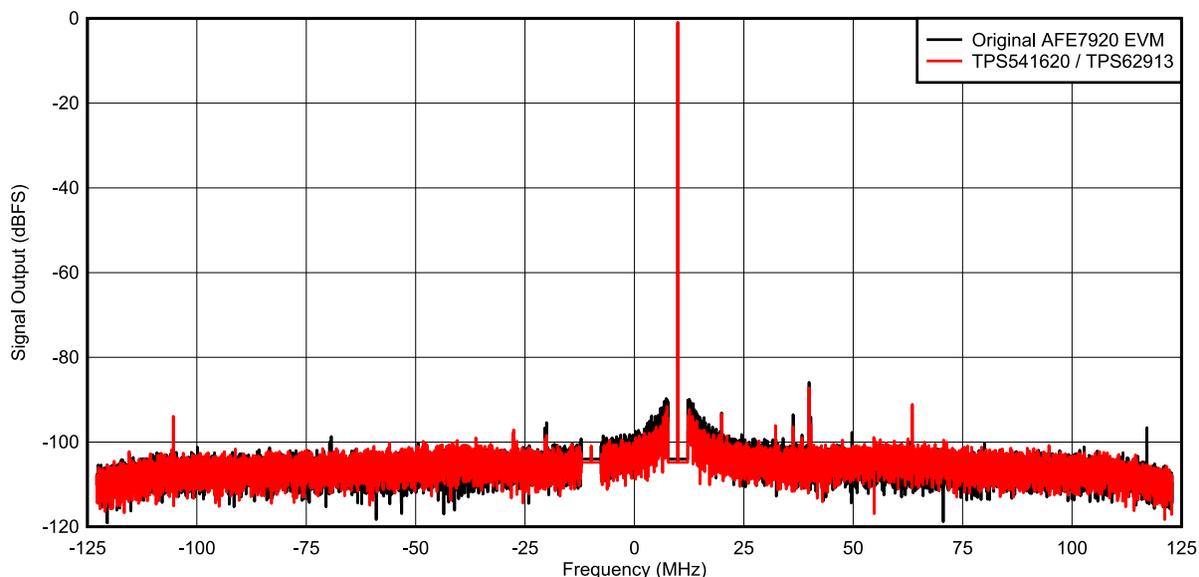


Figure 2-2. Full Spectrum Comparison Plot

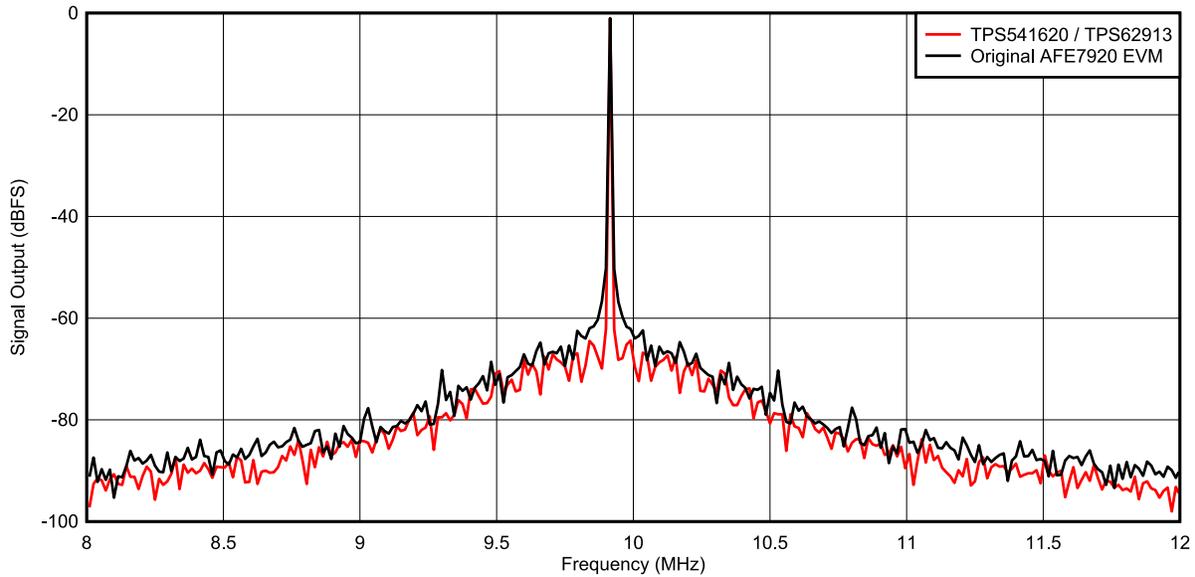


Figure 2-3. 4 MHz Close-in Comparison Plot

TX (Transmit) Spectrum

Figure 2-4 show the transmit spectrum performance close to the carrier at 2 MHz span between the standard EVM compared with the TPS62913. Both boards show good performance, although the original AFE7920 board shows a spur at ~613kHz, likely from the original switching power supply. The TPS541620/TPS62913 low noise board has a clean spectrum and an increased switching frequency of 1 MHz.

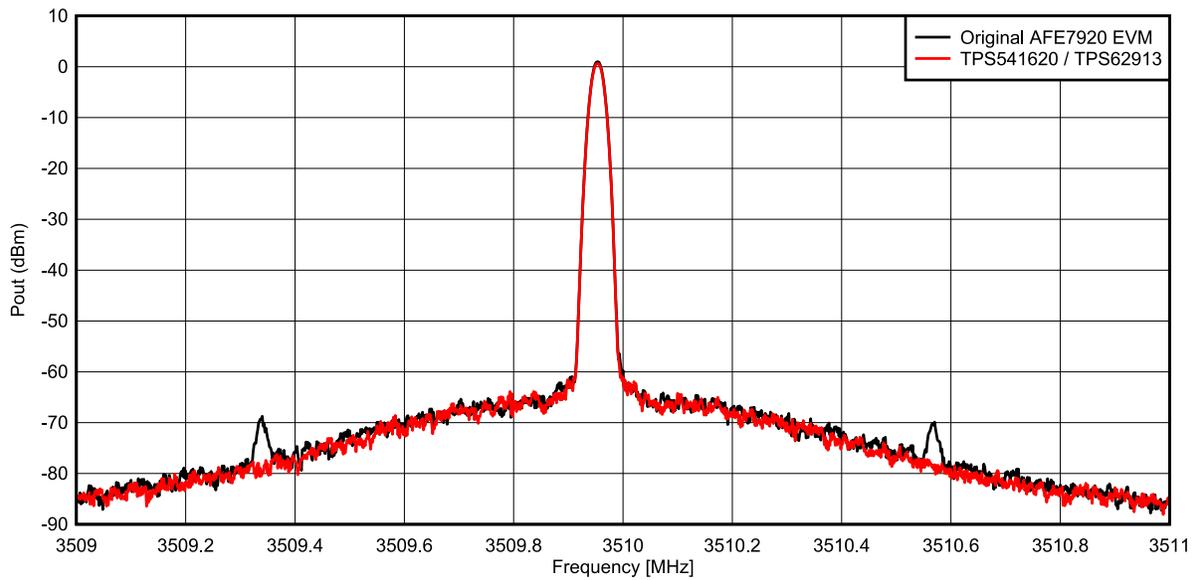
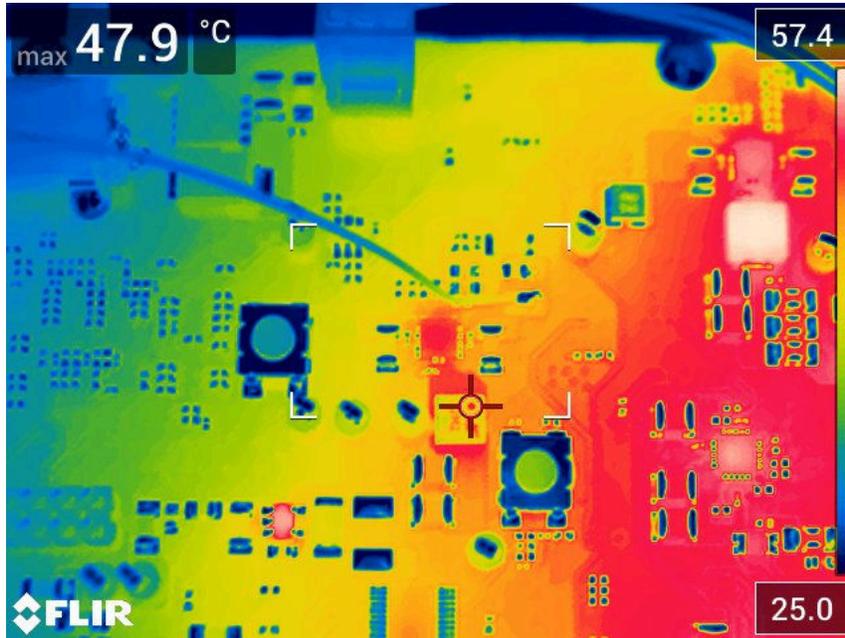


Figure 2-4. 2 MHz Span TX Spectral Plot

Table 2-1. Power Consumption Comparison for the 1.8 V rails on the Original and TPS62913 Boards

Configuration	Input Voltage and Current	Input Power
Input Power for the 1.8 V rails with the Original AFE7920 EVM with DC-DC converters + LDOs	5.6 V @ 1.165 A	6.526 W
Input Power for the 1.8 V rails with two TPS62913	5.6 V @ 0.944 A	5.286 W
Input Current and Power Savings for the 1.8 V rails	221 mA input current reduction	1.24 W Power Savings

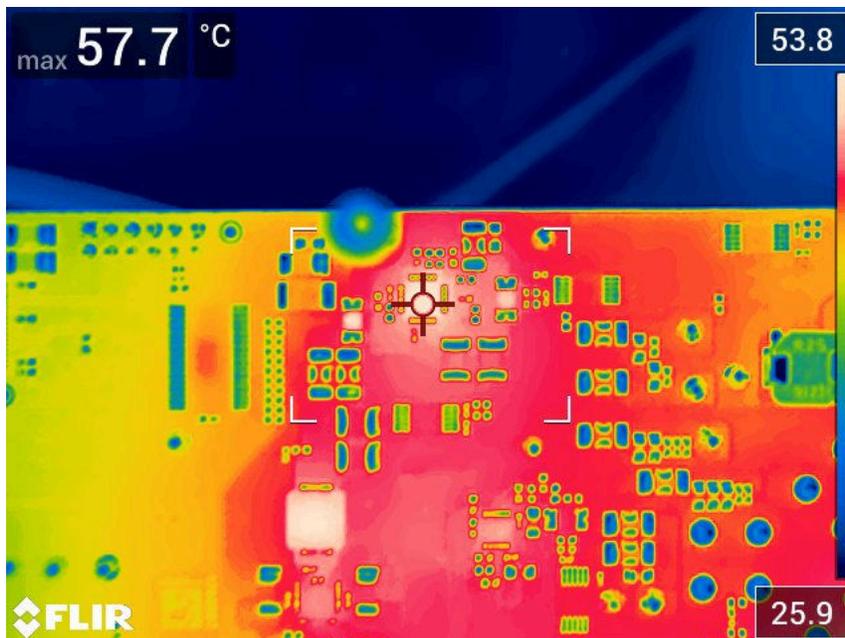
The following are thermal images of the power supplies running when taking data for the power performance comparison tables.



Note

Original Board DC-DC Max Temp is 47.9 C

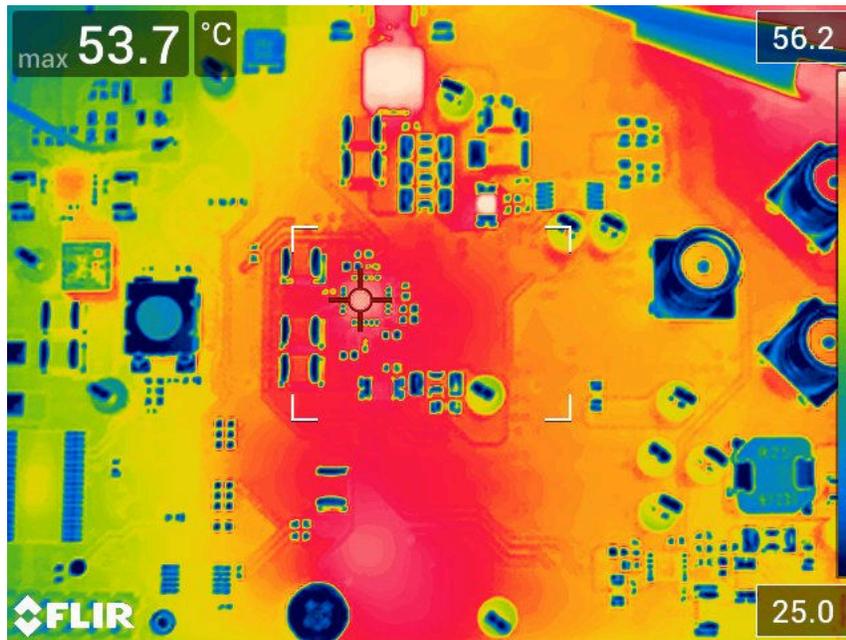
Figure 2-5. Original 2.2V Switching Converter



Note

Original Board LDO Max Temp is 57.7 C

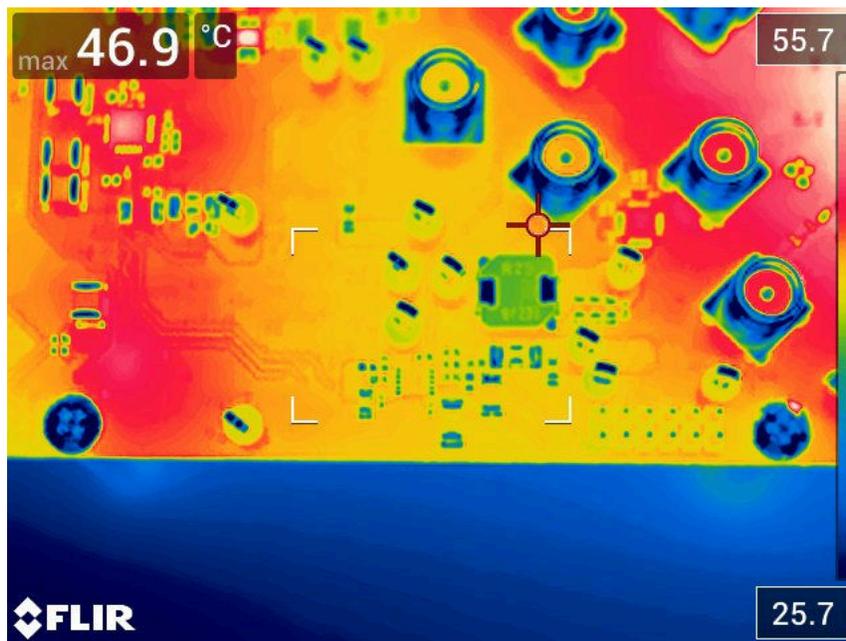
Figure 2-6. Original 1.8V LDO



Note

Original Board LDO Max Temp is 53.7 C

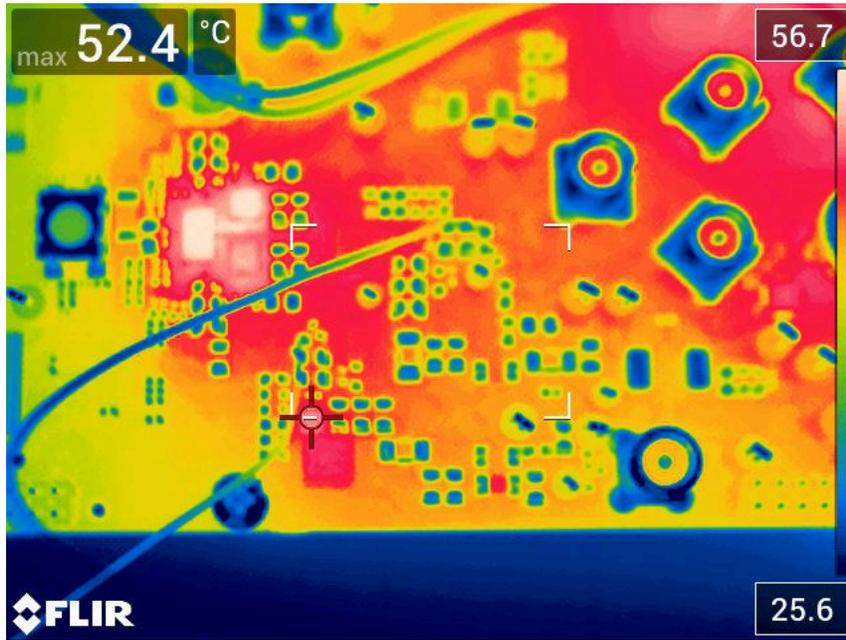
Figure 2-7. Original 1.8V_CLK LDO



Note

Original Board LDO Max Temp is 46.9 C

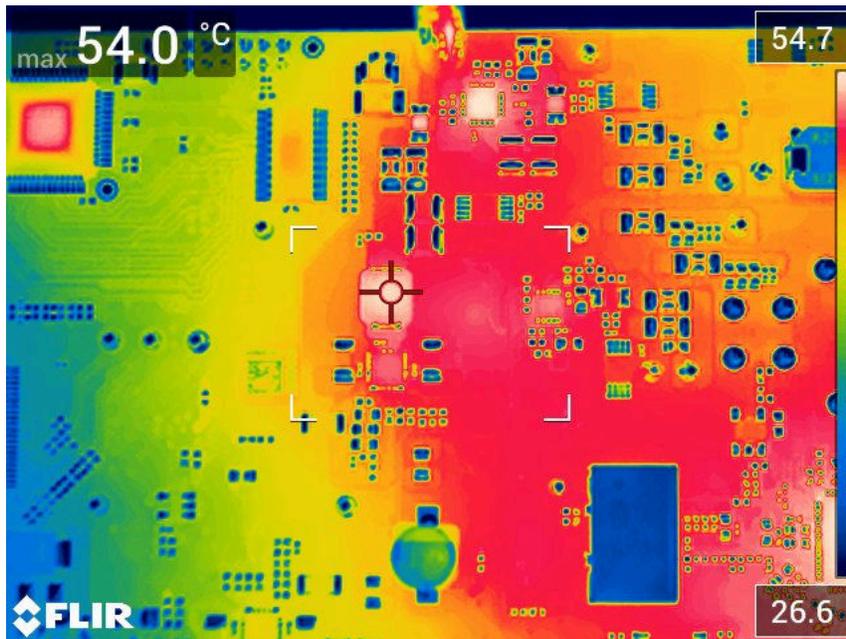
Figure 2-8. Original 1.8V_PLL LDO



Note

TPS62913 Max Temp is 52.4 C

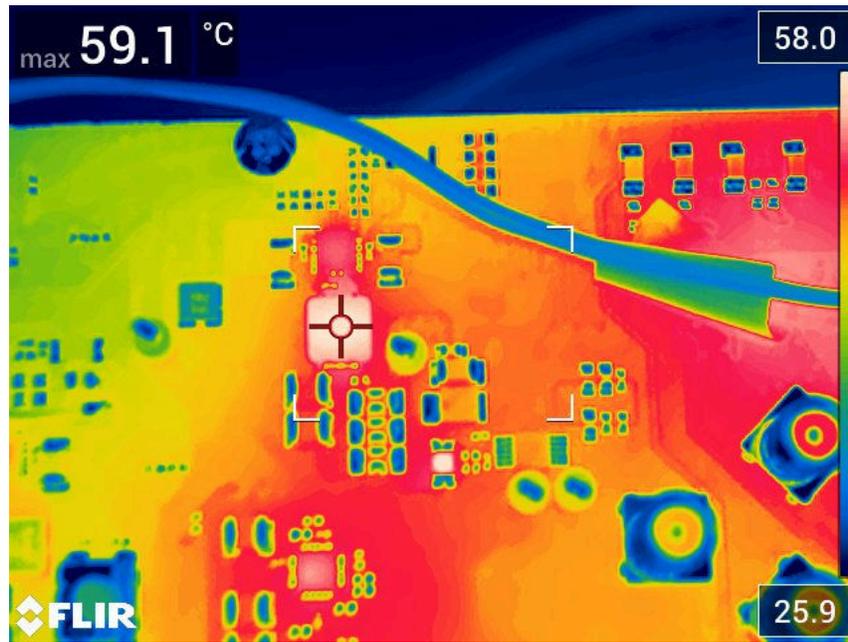
Figure 2-9. TPS62913 1.8V Switching Converters



Note

Original Board DC-DC Max Temp is 54.0 C

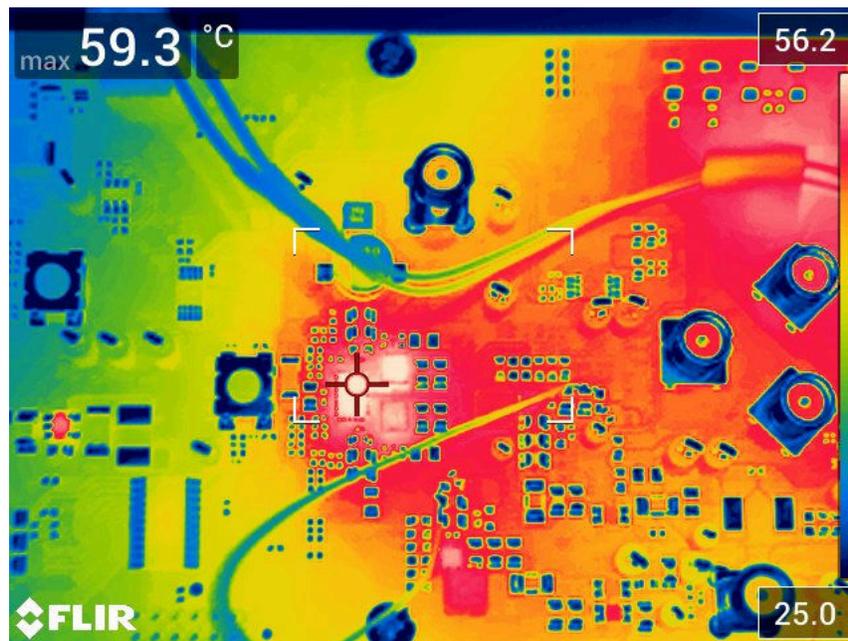
Figure 2-10. Original 1.2V Switching Converter



Note

Original Board DC-DC Max Temp is 57.7 C

Figure 2-11. Original 0.9V Switching Converter



Note

TPS541620 Max Temp is 59.3 C

Figure 2-12. TPS541620 0.9V and 1.2V Dual Switching Converter

3 Schematic

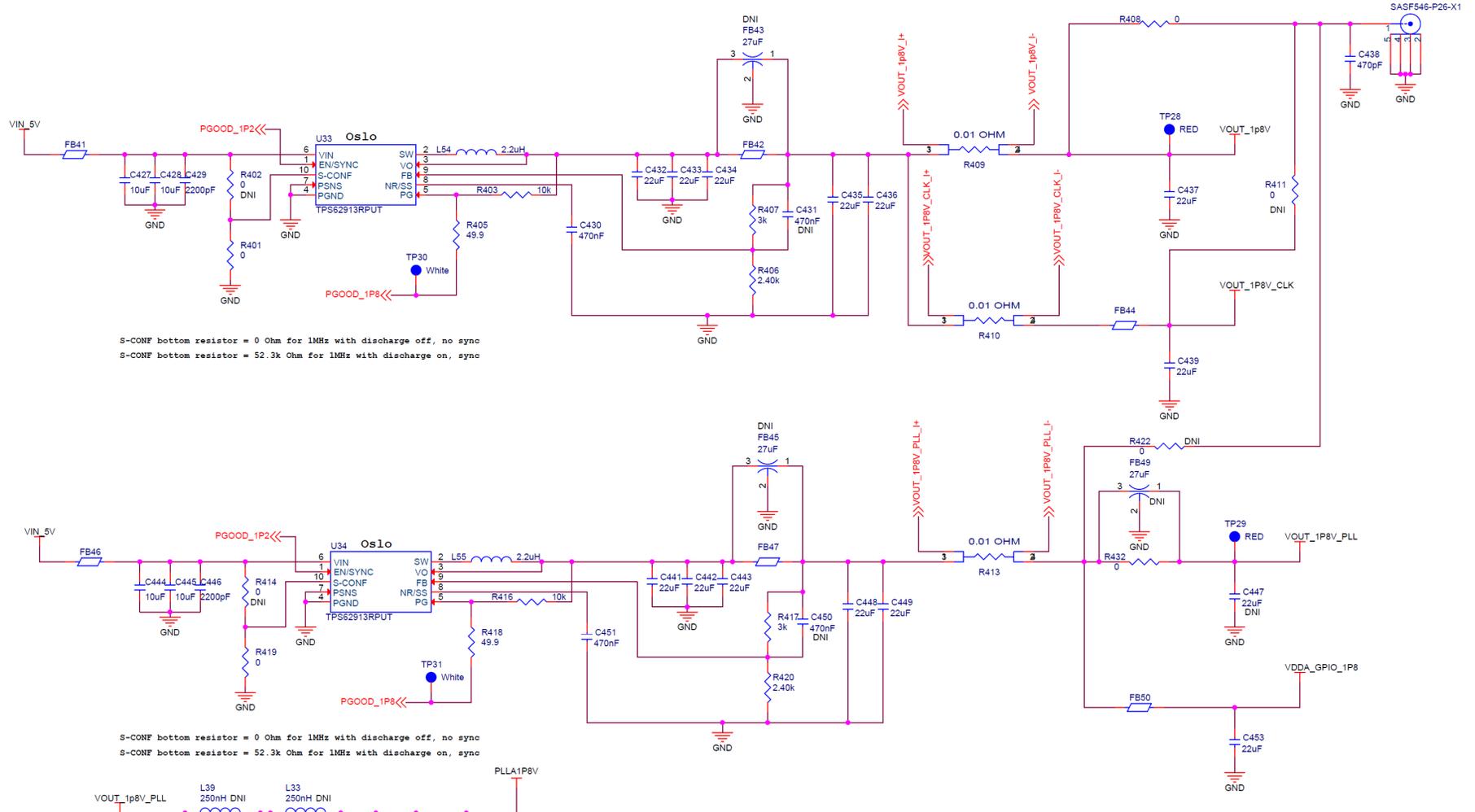


Figure 3-1. TPS62913 1.8 V Power Schematic

4 Conclusion

As shown by the test results, a simplified power supply design using the TPS62913 low-ripple and low-noise buck converters can provide similar performance to the traditional DC-DC converter + LDO approach. The 1.8 V rails are all supplied using the TPS62913 switching regulator without the need for a low-dropout linear regulator (LDO) while maintaining the same performance as the original design. The performance is similar to the DC-DC converter + LDO approach. Use of the TPS62913 design reduces the power consumption by 1.24 W for the 1.8 V rails, reduces the size of the design, and reduces the temperature rise of the power supply components.

Although this design used the AFE7920, other AFEs that require low noise power supplies that are size constrained and thermal constrained can also use this approach.

5 References

- Texas Instruments, [AFE7920, Four-transmit four-receive RF-sampling transceiver with dual-band DUC/DDC and two feedback paths](#) data sheet.
- Texas Instruments, [TPS6291x 3-V to 17-V, 2-A/3-A Low Noise and Low Ripple Buck Converter with Integrated Ferrite Bead Filter Compensation](#) data sheet.
- Texas Instruments, [TPS541620 4.5-V to 17-V, Advanced Current Mode, Dual 6-A Synchronous SWIFT Step-Down Converter](#) .

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2022) to Revision A (December 2021)	Page
• Updated Power Consumption Comparison for the 1.8 V rails on the Original and TPS62913 Boards table....	11

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