Application Report

Enhance Stability of TPSM41625 Buck Module Designs with Minimized Ceramic Output Capacitors

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ABSTRACT

Reducing the value and quantity of output capacitors can help reduce overall solution size and cost. This application report shows how to improve the stability (phase and gain margins) of TPSM41625 when using a minimum number of all ceramic output capacitors. The TPSM41625 is an 11 x 16 mm, 25-A rated, synchronous step-down power module that features an input range of 4 V to 16 V, and a wide adjustable output range from 0.6 V to 7 V. The minimum output capacitor recommendations outlined in the TPSM41625 datasheet are fit for typical Point-of-Load (POL) applications where tight transient response is required and a mix of bulk polymer and ceramic output capacitors are often used. However, for applications with less stringent transient requirements, the output capacitance required for stability can be reduced below the typical datasheet recommendations to just a few ceramic capacitors by adjusting the device configuration and adding a feedforward capacitor.

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Trademarks

1 Introduction

The TPSM41625 is a fixed frequency buck power module that uses an internally compensated Advanced Current Mode (ACM) control scheme intended to simplify the design process. While the ACM scheme in TPSM41625 offers a ramp selection feature to tune the gain of the loop response, the fixed power stage inductor in the module and the finite internal compensation options result in minimum requirements on the output capacitor network for stable operation.

This application report will demonstrate how a combination of TPSM41625 ramp and reference settings, along with an external feedforward capacitor, can enhance the phase and gain margin of all ceramic, minimized output capacitor designs. While this report does not delve into the internal details of ACM control (1), measured loop response data is provided for an example design to illustrate the effect of output capacitance, ramp setting, and other design factors on TPSM41625 loop stability. Figure 1-1 shows the schematic of a 12-V input, 1.8-V output, 25-A, 500-kHz rail that is taken as the starting point for the design.

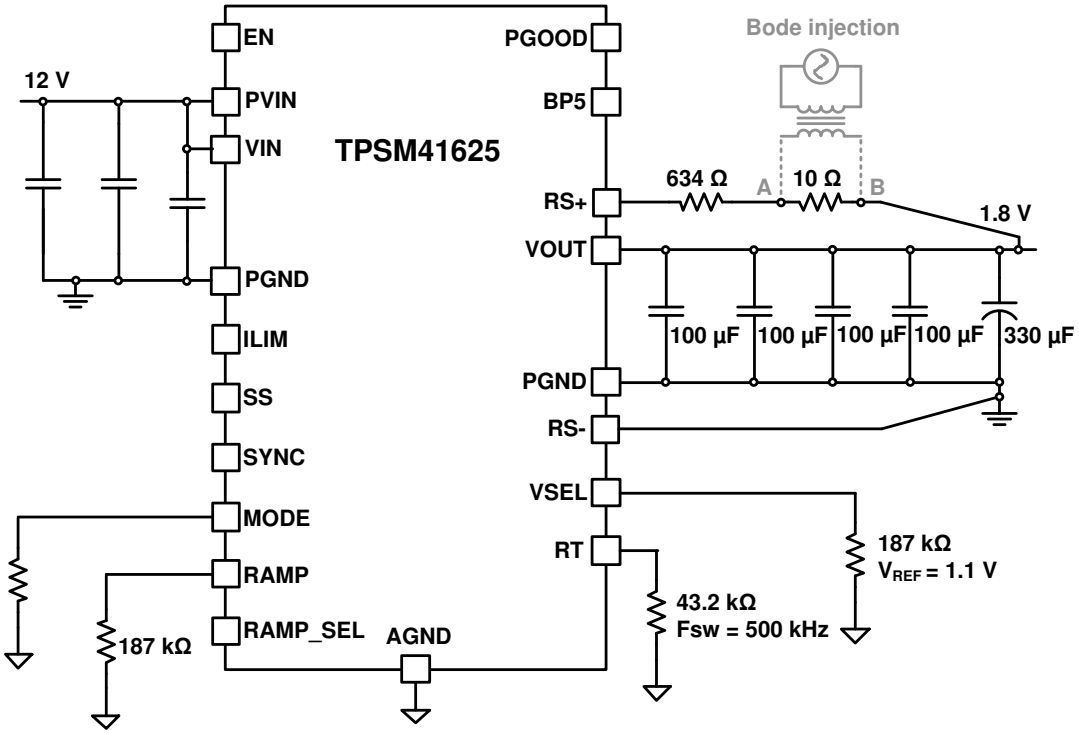

Figure 1-1. Original 12-V input, 1.8-V output, 25-A, 500-kHz design

2 Effect of Reducing Output Capacitance on Loop Response

Figure 2-1 shows the measured loop response of the TPSM41625 with different output capacitor configurations. The capacitor configurations span from the initial design shown in Figure 1-1, which is based on the TPSM41625EVM evaluation module and consists of a bulk 330-µF polymer (6TPE330MAA) and four 100-µF ceramic (GRM32EC70J107ME15L) capacitors, down to a design using only three of the same 100-µF ceramic capacitors.

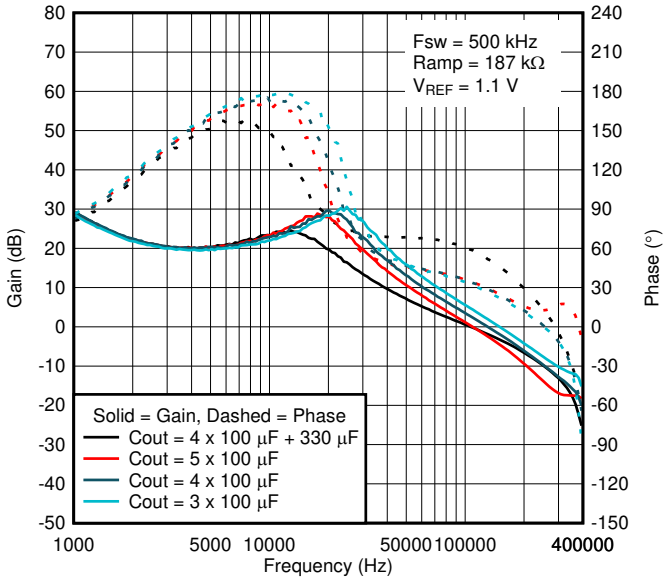

Figure 2-1. Bode plot for different Cout (12-V input, 1.8-V output)

For the default evaluation module design, the bulk capacitor contributes an ESR zero which provides phase boost. The phase margin is almost 60° at the loop crossover frequency of 105 kHz where the gain curve crosses 0 dB. The phase curves are lower when the bulk capacitor (and the zero from the ESR) is removed. Decreasing the number of ceramic capacitors pushes the loop crossover frequency higher with decreasing phase margin.

With only 3 x 100 µF of nominal ceramic output capacitance, the loop crossover frequency is 148 kHz with a phase margin of 23° and gain margin of 8 dB. The typical recommendations are to have a minimum of 45° of phase margin and greater than 10 dB of gain margin. Furthermore, while crossover frequencies up to 1/5 of the switching frequency are acceptable for TPSM41625 designs, a crossover frequency of 148 kHz may be considered too high for a switching frequency (Fsw) of 500 kHz. The subsequent sections of this report show different adjustments that can be made to the design to stabilize the control loop for this 3 x 100 µF (300 µF) nominal ceramic output capacitor configuration.

3 Effect of Ramp Setting on Loop Response

The TPSM41625 provides RAMP and RAMP_SEL pins which can be used to program the internal ramp and tune the loop response. With the RAMP_SEL pin left open, an external resistor connected between RAMP and AGND sets the internal ramp. Connecting RAMP_SEL to AGND and leaving RAMP pin open will select the internal 78.7-kΩ resistor such that no external resistor is required. Figure 3-1 shows these connection options.

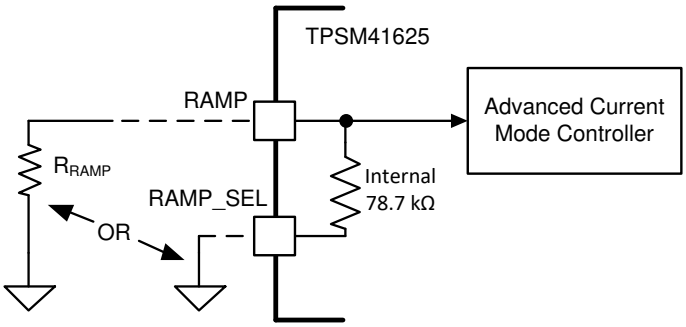

Figure 3-1. Ramp connection options

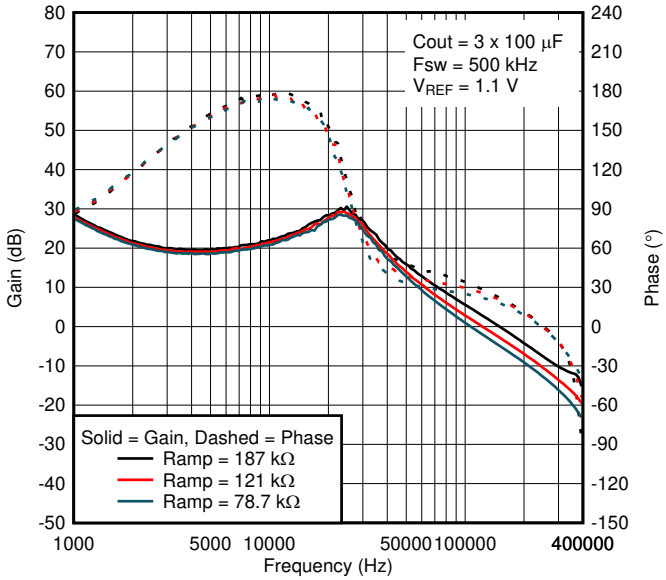

Figure 3-2. Bode plot for different ramp setting (12-V input, 1.8-V output)

The loop response for three different ramp settings is shown in Figure 3-2 for the 300-µF ceramic output capacitor configuration introduced in the previous section. As shown in the figure, decreasing the ramp resistor from 187 kΩ (the original value) to the lower options decreases the loop crossover frequency. A lower ramp resistor selects a lower internal ramp capacitor, which lowers the gain curve and thus the crossover frequency. With the internal 78.7-kΩ resistor selected, the crossover frequency has decreased from 148 kHz to 105 kHz and the gain margin has improved from 8 dB to 12.5 dB. However, in this case the phase curve has also shifted such that the phase margin is 24.5°, only a minor improvement compared to the 23° of phase margin with the 187-kΩ ramp setting. The following sections explore methods to increase the phase margin of this design with the internal 78.7-kΩ resistor selected.

4 Effect of Switching Frequency on Loop Response

The switching frequency of the TPSM41625 is adjustable from 300 kHz to 1 MHz and is programmed by a resistor connected between the RT pin and AGND. The TPSM41625 can also be synchronized to an external clock. Frequency synchronization is useful for applications that require multiple power rails to be synchronized to the same switching frequency to avoid beat frequency problems on the common input power line.

Figure 4-1 shows the loop response of the 300-µF output capacitor design with the 78.7-kΩ ramp resistor for switching frequencies of 500 kHz, 700 kHz, and 1 MHz. Higher switching frequencies improve the stability of the module as the Fsw/2 pole moves higher resulting in higher phase maintained near the crossover. The loop response for 1 MHz has a phase margin of 46.2°, indicating a stable design, and its crossover frequency of 146 kHz is below 1/5 of the switching frequency and is acceptable.

Switching at higher frequencies has a tradeoff of higher switching losses and lower efficiency. The efficiency at different switching frequencies is shown in Figure 4-2. At a switching frequency of 500 kHz, the efficiency is 91% peak and 89.5% at full 25-A load. At 1 MHz, the efficiency is 88.5% peak and 86.9% at full 25-A load, which translates to 1.6 W of higher power dissipation at full load when operating at 1 MHz versus at 500 kHz.

Therefore, while switching at 1 MHz provides a more stable design, the lower efficiency and higher power dissipation may be undesirable. Moving to higher switching frequency may also not be allowed if the application requires lower switching frequency to minimize switching harmonic content from falling into certain frequency bands, and, as previously mentioned, if the application requires the module to be synchronized with other power rails that are switching at a given frequency. Different approaches to improve phase margin must be used to maintain the high efficiency and operate at the original 500-kHz switching frequency of the design.

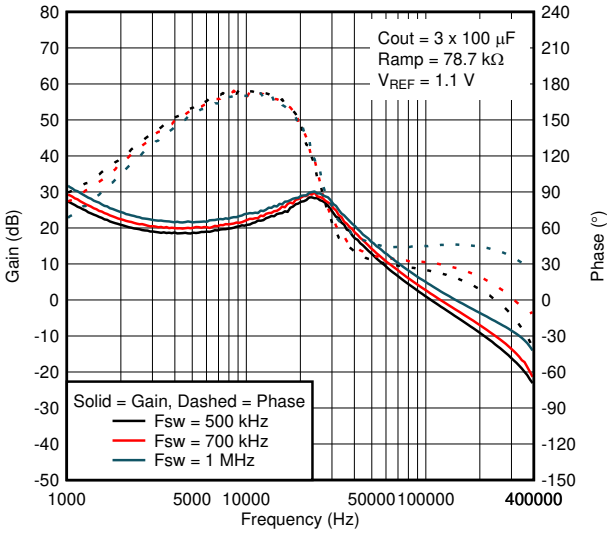

Figure 4-1. Bode plot for different switching frequency (12-V input, 1.8-V output)

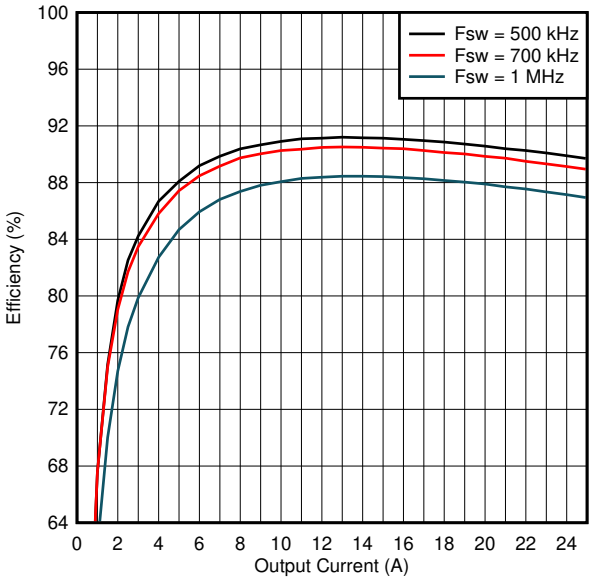

Figure 4-2. Efficiency for different switching frequency (12-V input, 1.8-V output)

5 Improving Stability by Decreasing the Voltage Reference and Adding a Feedforward Capacitor

The use of a feedforward capacitor (C_{FF}) to increase loop bandwidth and phase margin is well documented in other application reports (2). One consideration when using a feedforward capacitor is that the maximum possible phase boost is limited by the ratio of the reference voltage to the output voltage. The maximum possible phase boost for a given reference voltage (V_{REF}) and output voltage (V_{OUT}) can be calculated using Equation 1 or determined using Figure 5-1.

$$\theta_{max} = \tan^{-1}\left(\frac{V_{OUT} - V_{REF}}{2\sqrt{V_{OUT}\ V_{REF}}}\right) \quad (1)$$

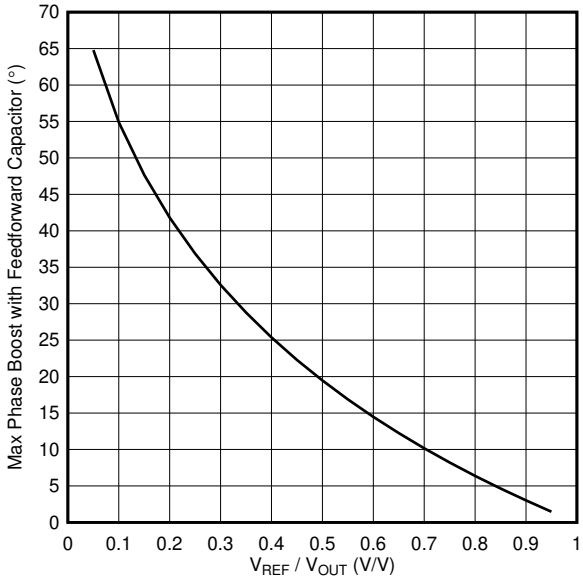

Figure 5-1. Maximum phase boost with feedforward capacitor

The results shown in this report thus far have been with a reference voltage of 1.1 V. For a 1.8-V output with a 1.1-V reference, the ratio is 1.1 V / 1.8 V = 0.61 V/V and the maximum possible phase boost with a C_{FF} capacitor is only 14°. Recall that the 300-µF output capacitor design switching at 500 kHz has a phase margin of 24.5°, thus, the C_{FF} capacitor alone cannot provide sufficient phase boost to increase the phase margin above 45°. Furthermore, the maximum theoretical phase boost cannot be realized directly as phase margin improvement because C_{FF} boosts the phase and the gain such that the crossover frequency also increases to where there is more phase lag in the loop.

To increase the amount of C_{FF} phase boost, it is necessary to lower the reference voltage. The TPSM41625 has 10 selectable internal reference voltage options ranging from 0.6 V to 1.1 V. The reference voltage is programmed with a resistor R_{VSEL} connected from VSEL pin to AGND. By using the 0.6-V reference (V_{REF} / V_{OUT} = 0.33 V/V), the maximum phase boost possible with C_{FF} increases to 30°. The changes required to switch from the 1.1-V to the 0.6-V reference voltage are shown in Figure 5-2. The R_{VSEL} resistor of 187 kΩ is replaced with a short to AGND. The R_{ADJ} resistor is increased from 634 Ω to 2 kΩ to keep the output voltage set at 1.8 V.

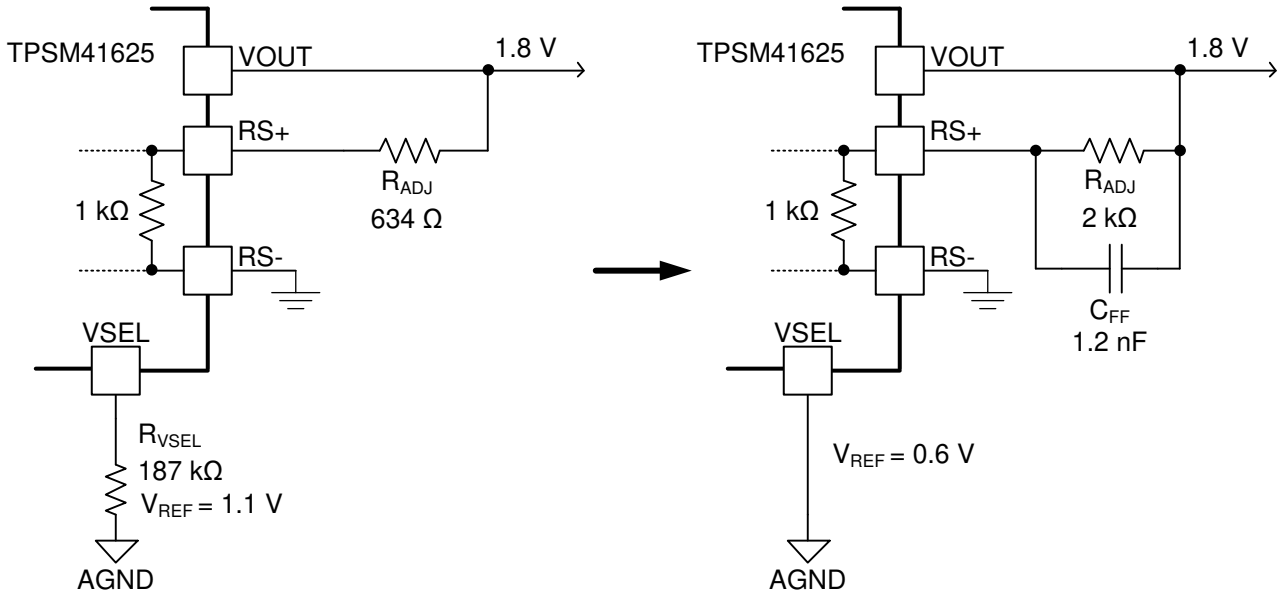

Figure 5-2. Changes to lower reference voltage and add feedforward capacitor

Switching to the 0.6-V reference has other impacts on stability in addition to increasing the maximum C_{FF} phase boost. Lowering the reference voltage decreases the divider gain and lowers the entire gain curve, lowering the crossover frequency and increasing the phase and gain margin. Figure 5-3 shows the Bode plot with the original 1.1-V reference and 0.6-V reference. By switching to the 0.6-V reference, the crossover frequency has reduced from 105 kHz to 79 kHz, phase margin has increased from 24.5° to 29°, and gain margin has increased from 12.5 dB to 16.7 dB.

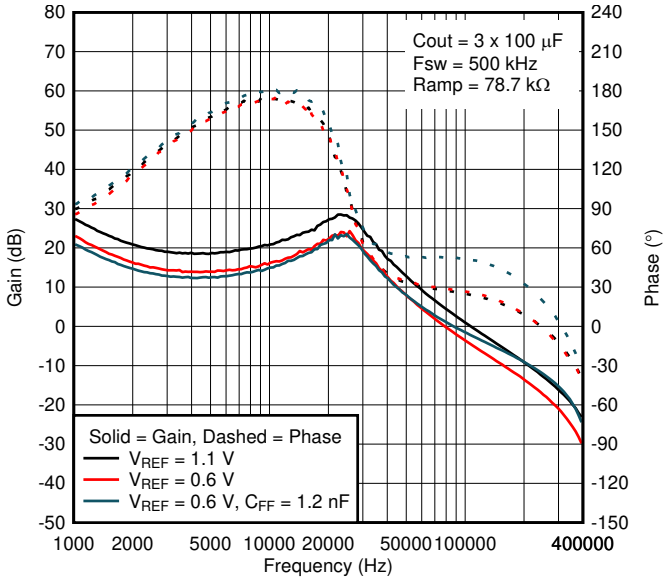

Figure 5-3. Bode plot with lower reference voltage and feedforward capacitor (12-V input, 1.8-V output, 20-A load)

Figure 5-3 also shows the measured Bode plot for 0.6-V reference with a 1.2-nF C_{FF} capacitor which shows the final stable design with a crossover frequency of 87 kHz, phase margin of 52.5°, and gain margin of 16 dB. These are all meeting the recommended criteria for a stable design. The final schematic with all modifications is shown in Figure 5-4.

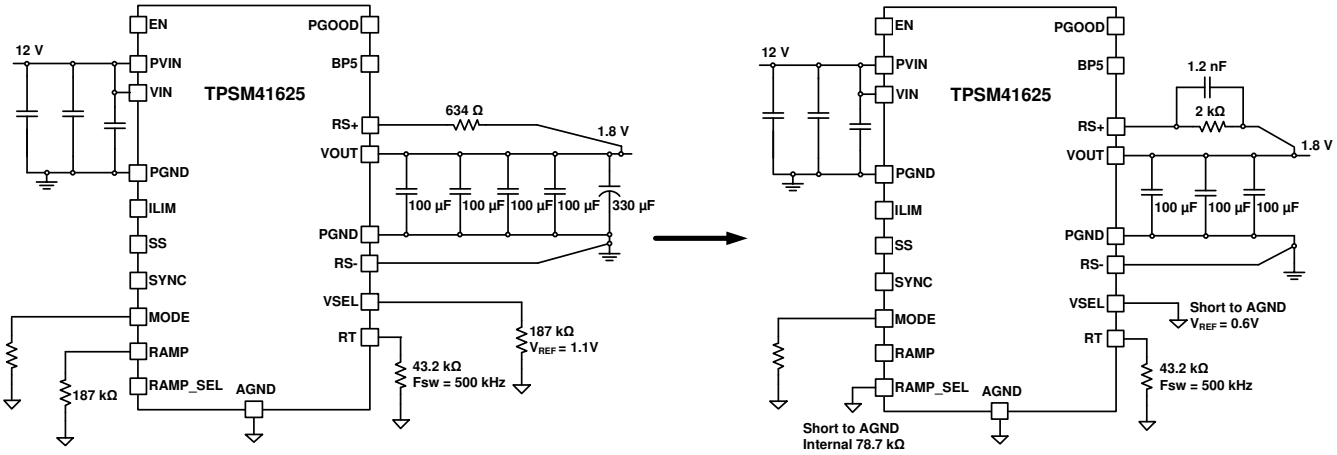

Figure 5-4. Original and Optimized 12-V input, 1.8-V output, 25-A, 500-kHz design with 3 x 100 µF of ceramic output capacitance

Figure 5-5 and Figure 5-6 show the transient response for a 0 to 5-A step at 10 A/µs with the 0.6-V reference without and with the 1.2-nF feedforward capacitor, respectively. The ringing is clearly reduced with the addition of the feedforward capacitor, and the transient undershoot and overshoot remain within ±3% of the 1.8-V output. Figure 5-7 shows a larger step of 0 to 10 A at 10 A/µs, showing a transient deviation of about ±5%.

There is a tradeoff in using the lower reference voltage, however: the output voltage accuracy is reduced. Assuming ideal resistors and ignoring all other error sources such as resistor tolerance, the ±0.5% reference accuracy will reflect as a ±1.5% (±0.5% × 1.8 V / 0.6 V) accuracy at the output for the 0.6-V reference, compared to ±0.81% (±0.5% × 1.8 V / 1.1 V) accuracy for the 1.1-V reference. This may be an acceptable tradeoff for stabilizing a minimum ceramic output capacitor design and maintaining 500-kHz operation at high efficiency.

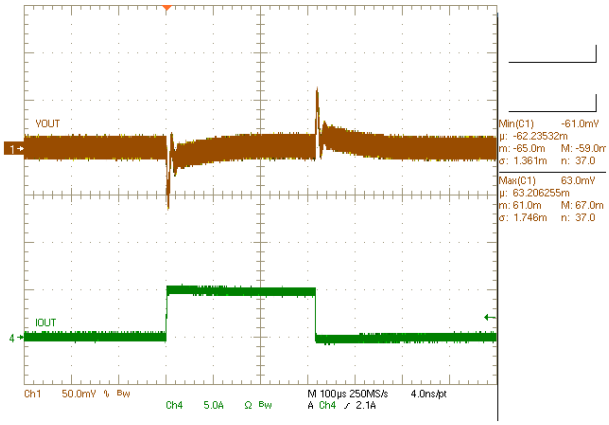

Figure 5-5. Load transient 0 to 5 A at 10 A/µs without C_{FF}

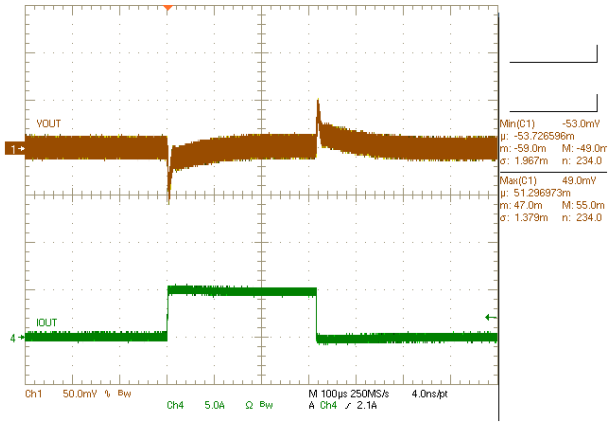

Figure 5-6. Load transient 0 to 5 A at 10 A/µs with 1.2-nF C_{FF}

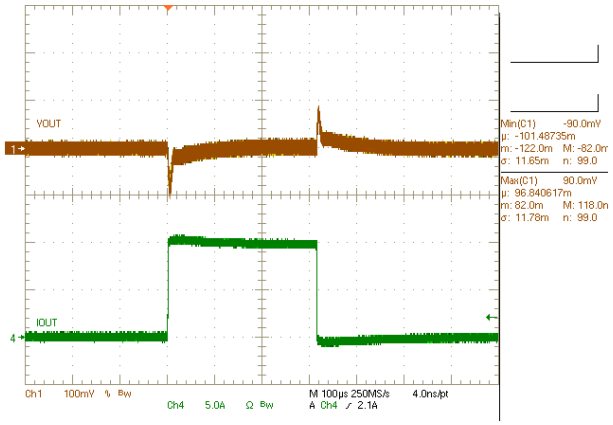

Figure 5-7. Load transient 0 to 10 A at 10 A/μs with 1.2-nF C_{FF}

6 Summary

This application report has shown how the output capacitor configuration, ramp setting, and switching frequency can affect the loop response of the TPSM41625. Furthermore, this report has demonstrated how a lower reference voltage and a feedforward capacitor help improve the loop stability when using all ceramic output capacitor configurations. With the lower reference voltage and feedforward capacitor, the example 12-V input 1.8-V output 25-A design with three 100-μF ceramic output capacitors is made stable while maintaining ±3% undershoot and overshoot for a 0 to 5 A step at 10 A/μs.

7 References

The following documents are available for download from TI.com:

1. Texas Instruments, Internally Compensated Advanced Current Mode (ACM)
2. Texas Instruments, Optimizing Transient Response of Internally Compensated dc-dc Converters With Feedforward Capacitor

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