Application Report

How to Achieve Low EMI with TPS55288 Buck-Boost Converter

Helen Chen

ABSTRACT

In switching power supplies, EMI noise is unavoidable due to the high switching actions of the semiconductors and the resulting high di/dt current in the circuit. EMI control is one of the most difficult challenges in switch-mode power supply design (SMPS). In this application note, the root cause of the EMI noise is analyzed. Then a list of design guideline for minimizing the EMI noise is presented. The guideline contains the layout level tips, which involves components placement, layer stack up, ground plane routing. The guideline also contains circuit level design, which involves the frequency dithering, snubber circuit and the filter circuit design.

Table of Contents

1 Introduction 2
2 Design Process 3
2.1 Radiation Theory 3
2.2 Root Cause of the Broad Band EMI in a Buck-Boost Converter 4
2.3 How to Achieve Low EMI with TPS55288 Buck-Boost Converter 5
3 Schematic and Test Result 10
3.1 Test Result 11
4 Summary 13
5 References 14

List of Figures

Figure 2-1. Harmonic Content of a Pulsed Current Waveform 3
Figure 2-2. Buck-boost Converter Schematic with Critical Loops 4
Figure 2-3. Cross Section of Two-Layer Board and Four-Layer Board 5
Figure 2-4. Radiated EMI Result of a 2-Layer PCB 6
Figure 2-5. Radiated EMI Result of a 4-Layer PCB 6
Figure 2-6. Symmetrical PCB Layout of TPS55288 Buck-Boost Converter 6
Figure 2-7. Radiated EMI Comparison with Symmetrical Placement 7
Figure 2-8. Benefits of Frequency Dithering 7
Figure 2-9. Conduction EMI Comparison with Frequency Dithering 8
Figure 2-10. Equivalent Model of the Switching Loop 8
Figure 2-11. Radiation EMI Comparison with and without RC snubber 9
Figure 2-12. Simplified Input EMI Filter 9
Figure 2-13. Impedance Characteristics of BLM21PG300SN1 9
Figure 3-1. Schematic for the EMC Test 10
Figure 3-2. Buck Mode EMI Result (VIN = 12 V, VOUT = 5V / IOUT = 3A) 11
Figure 3-3. Boost Mode EMI Result (VIN = 12 V, VOUT = 20V / IOUT = 3A) 12

Trademarks

All other trademarks are the property of their respective owners.

1 Introduction

SMPS generates electronics noise due to high dv/dt and high di/dt transition during the switching. The high frequency SMPS typically generates three types of EMI: low frequency noise (<30MHz) as harmonics of the switching frequency; mid-frequency broadband noise (30-300MHz) from switching node voltage ringing and high frequency pulsating current; high frequency noise from reverse recovery. The low frequency EMI is easy to be filtered by the LC filters. The aim of this design guideline is to minimize mid-to-high frequency radiation EMI which is most difficult to deal with, and pass the vert strict CISPR25 level5 EMI test.

In this application note, the root cause of the EMI noise is analyzed. Then a list of design guideline for minimizing the EMI noise is presented. The guideline contains the layout level tips, which involves components placement, layer stackup, ground plane routing. The guideline also contains circuit level design, which involves the frequency dithering, snubber circuit and the filter circuit design.

2 Design Process

2.1 Radiation Theory

Some of the energy is radiated directly from the PCB, which can be modeled as a small antenna carrying the interference current. A small loop is one whose dimensions are smaller than a quarter wavelength at the frequency of interest (75cm at 100MHz). Most PCB loops count as small at emission frequencies up to a few MHz. The maximum electric field strength from such a small loop over a ground is proportional to the square of the frequency, the loop area and the current:

$$E = 263 \times 10^{-16} \times \frac{\left(f^2 \times A \times Is\right)}{r} \quad (1)$$

Where frequency is in Hz, A is the loop area in m^2, I is in Amps and r is in meters. For square waveforms with many harmonics, the Fourier spectrum must be used for Is.

We can use Equation 1 to indicate roughly whether a PCB design is need to be improved. For example if A=4cm^2, Is=10mA, f=100MHz, r=3m, therefore:

$$E = 263 \times 10^{-16} \times \left(100 \times 10^{6}\right)^2 \times 4 \times 10^{-4} \times \frac{0.01}{3} = 351 \times 10^{-6} \text{ V/m} = 50.9 \text{ dBuV/m} \quad (2)$$

The limit line for the CISPR 22 Class B at 3 meters, is around 40 dBuV/m, 50.9 dBuV/m is over the limit. So we need do some improvement on the circuit to make the filed fall under the limit. From Equation 1, we know that the items we can control are loop area A and the high frequency current. The loop area A can be reduced by good components placement and ground shielding; the high frequency current can be reduced by slowing down the switching speed or using symmetrical switching loop placement.

Figure 2-1 (A) shows a simplified trapezoidal current waveform with period T, pulse width t_W, rise time t_R and fall time t_F. Figure 2-1 (B) shows the frequency domain which consists of fundamental frequency and many upper harmonics. The relation with the pulse period, pulse width, rise/fall timesm and the amplitude of the upper harmonics can be derived through Fourier analysis.

Figure 2-1 is based on a 500 kHz switching signal with 1 us pulse width, 5 ns rise time and 8 ns fall time. At t_R‡ t_F condition, only the smaller one is considered. So the band width f_R is determined by t_R. Radiated EMI problems often occur in the 50 MHz~500 MHz range. It can be seen that increasing rise (or fall) time will shift the f_R point to a lower frequency. Thus the high frequency harmonic content will roll-off more quickly with 40dB/dec.

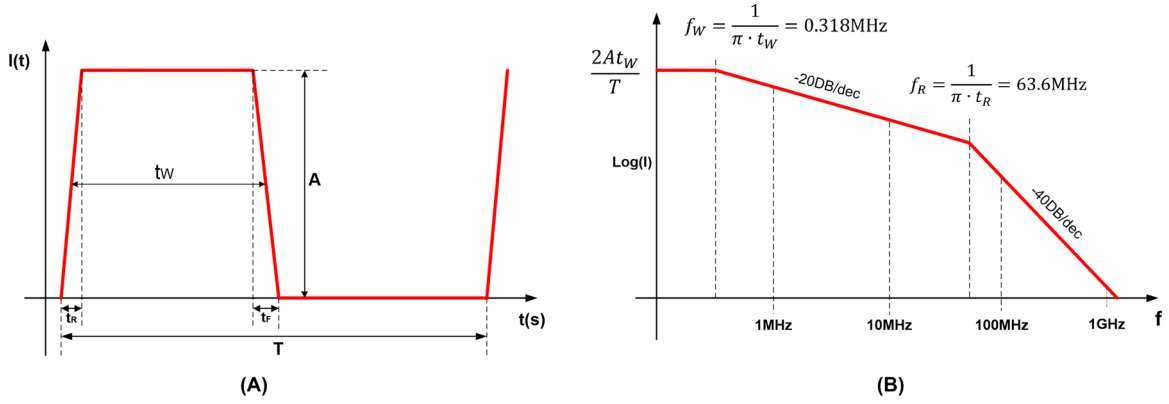

Figure 2-1. Harmonic Content of a Pulsed Current Waveform

2.2 Root Cause of the Broad Band EMI in a Buck-Boost Converter

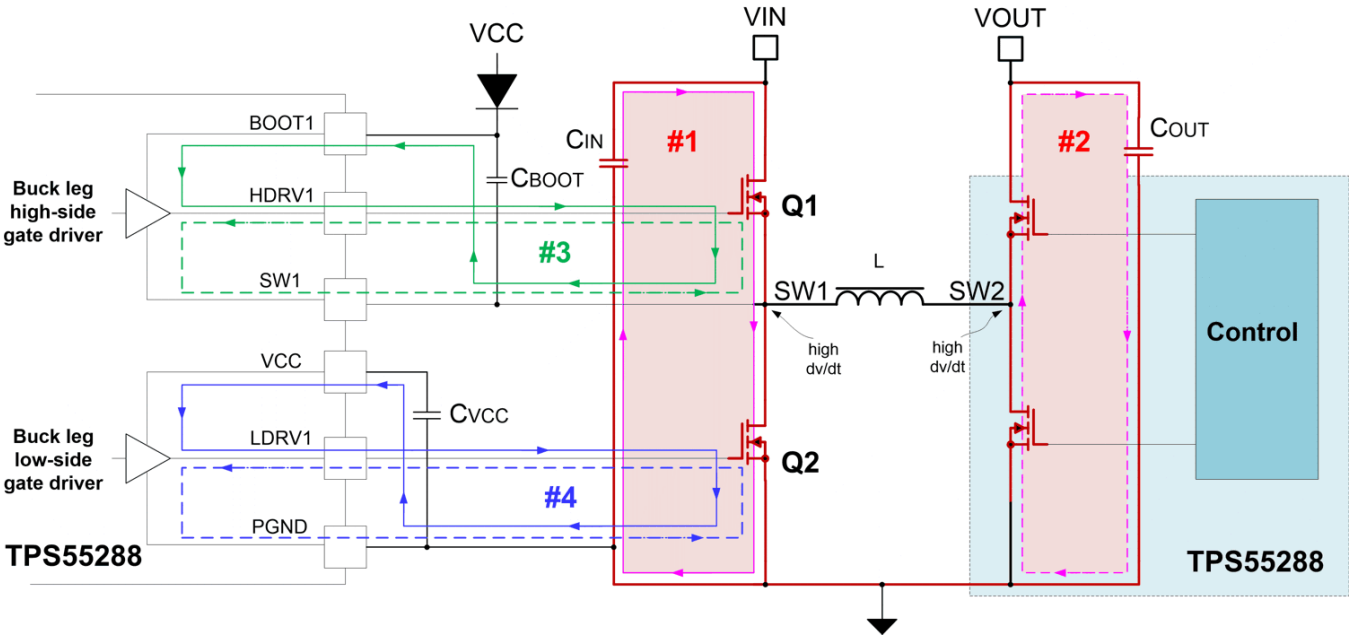

Figure 2-2. Buck-boost Converter Schematic with Critical Loops

Figure 2-2 shows the TPS55288 four-switch buck-boost converter with power stage components, an integrated gate drivers and a VCC bias supply. Figure 2-2 also distinguishes by color the high current traces, high dI/dt critical loops, and the high dv/dt switching nodes.

Loop 1 and loop 2, shaded in red, are the two critical high-frequency power loops for the buck-legs and the boost-legs. Long and thin traces in these two loops can cause excessive noise, overshoot and ring on the switching node, and the ground bounce because of the parasitic inductance. During a MOSFET switching event, the slew rate of the commutating current can exceed 3-5A/ns, so a 2nH parasitic inductance can results in a voltage spike of 6 V. The pulsed rectangular current waveforms flowing in these critical loops are rich in harmonic content, so a big loop area can cause big radiated energy emanating from it, which cause electromagnetic interference issue. So it is vital to minimize the trace length and the enclosed area of loop1 and loop2.

Loop 3 and 4 in Figure 2-2 are gate loops for the buck-leg MOSFET. To charge and discharge the MOSFET's gate capacitance during turn-on and turn-off transitions, an instantaneous current up to around 1A peak flows briefly in the gate loop, which may also cause interference issue. So we also need to minimize the enclosed area of loop3 and loop4 during the trace routing.

Loop1 and loop2 are the most critical loops. Because they are in the power loop, they carry high pulsed power current. They can directly radiate, they can also interfere adjacent traces and escape into the input and output cables and cause severe EMI issue.

The maximum voltage ringing at the switching node SW1 and SW2 corresponds to the switching speed and the loop area of loop1 and loop 2. Bigger loop area will cause more severe voltage ringing at the switching node. This ringing frequency also corresponds to the frequency range which the broad band EMI centered at.

2.3 How to Achieve Low EMI with TPS55288 Buck-Boost Converter

2.3.1 Adding Ground Planes under the Critical Loops

We can minimize the critical loop area A by compact placement. But this method is restricted by the physical size of the components. To get low EMI, one of the most important thing we can do is adding ground planes under the switching loops. Placing whole layer GND copper planes under the switching loops establish a passive shielding for the circuit. By Lenz's law, the current in the shield layer generates a magnetic field to counteract the original switch-loop magnetic field. The result is magnetic flux reduction, hence smaller equivalent loop area and better EMI performance.

In a multi-layer PCB with ground planes, the approximation inductance of a given loop can be calculated by Equation 3:

$$L = \frac{\mu_o \times h}{2 \times W_g} \approx \frac{6 \times h}{W_g} \left(\frac{nH}{cm} \right) \quad (3)$$

Where

- $\mu_o = 4\pi \times 10^{-7}$
- h is the insulation thickness between the signal layer and the ground plane.
- W_g is the width of the ground plane.

From Equation 3, we can see that wider and bigger ground plane results in smaller signal loop inductance. Thinner insulation thickness between the ground plane and the signal loop also results in smaller inductance.

Table 2-1 gives out the inductance of a given loop on different PCB boards. We can see that for a 4-layer PCB with 0.4 mm insulation thickness between the signal layer and the ground plane, the trace inductance is much smaller than that of a 1.6 mm thickness 2-layer PCB. So putting a solid ground plane with minimum distance to the critical loop is one of the most effective ways to reduce the EMI.

Table 2-1. Loop Trace Inductance (Trace Length = 5cm)

PCB	h (mm)	Wg(mm)	L(nH)
2-Layer PCB	**1.6**	**10**	**4.8**
4-Layer PCB	**0.4**	**10**	**1.2**

Figure 2-3shows the cross section of a 2-layer PCB and a 4-layer PCB. Figure 2-4 shows the radiated EMI result of a 2-layer PCB, Figure 2-5 shows the radiated EMI of a 4-layer PCB. The layer-stack and the PCB cross section is similar to that of Figure 2-4. With the same component placement and same test condition, the radiated EMI is improved by more than 15dBuV/m with a 4-layer PCB.

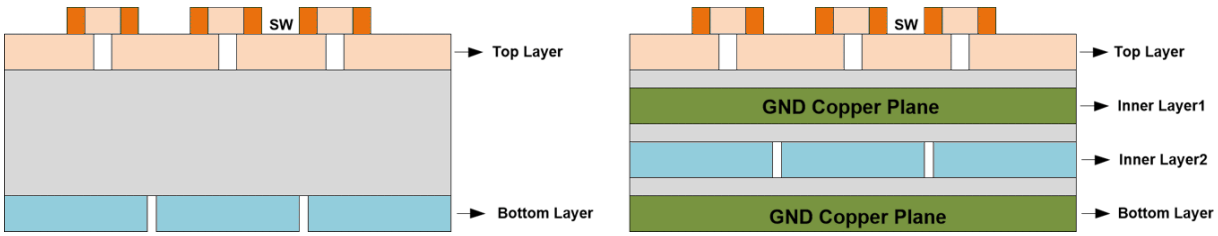

Figure 2-3. Cross Section of Two-Layer Board and Four-Layer Board

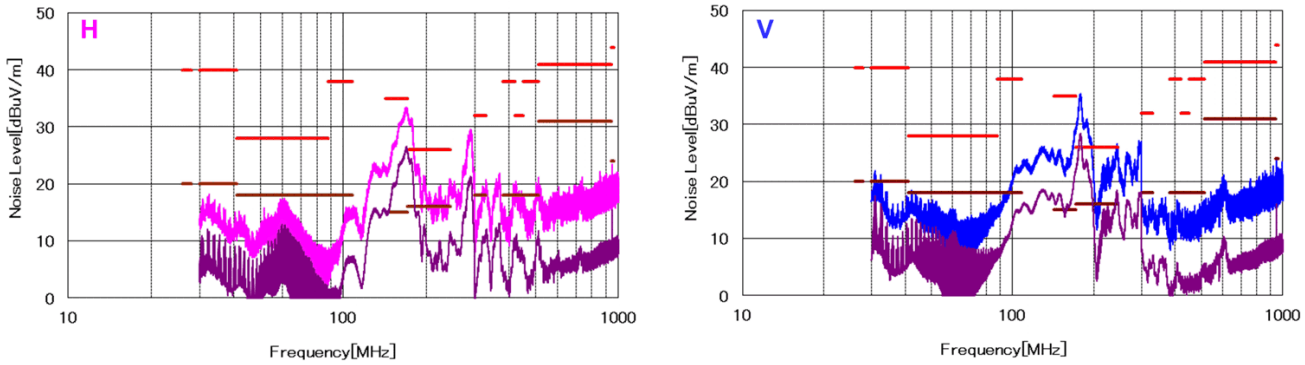

Figure 2-4. Radiated EMI Result of a 2-Layer PCB

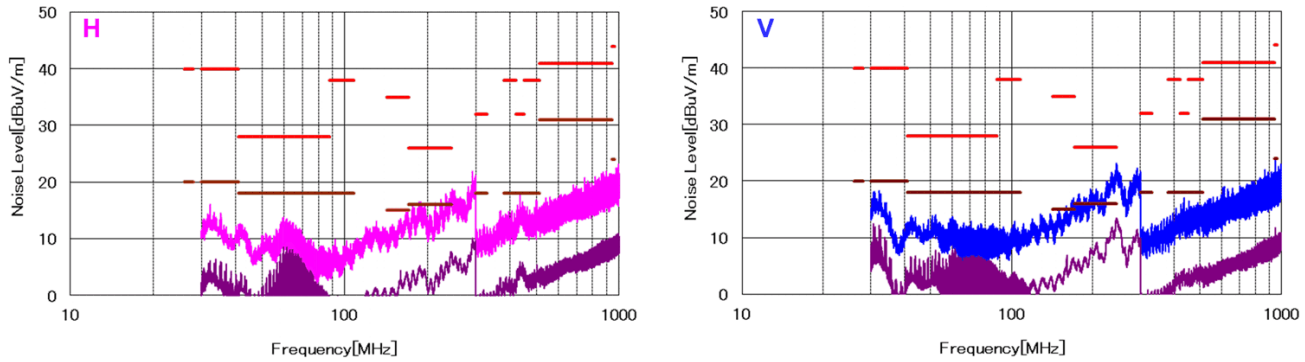

Figure 2-5. Radiated EMI Result of a 4-Layer PCB

2.3.2 Using Symmetrical Layout Configuration

EMI performance can be improved by minimizing the critical switching loops and by adding ground planes under the critical switching loops. If the test result is still over the limit, then other solutions like slowing down the switching speed, adding a metal shield over the power supply circuit should be considered. But slowing down the switching speed will sacrifice the efficiency, adding a metal shield will increase the cost and make the system assembly more complex.

Using symmetrical placement of the decoupling capacitors can further improve the EMI performance without sacrifice the efficiency or increase the cost. Figure 2-6 and Figure 2-7 show the schematic and the related PCB layout of this symmetrical placement concept.

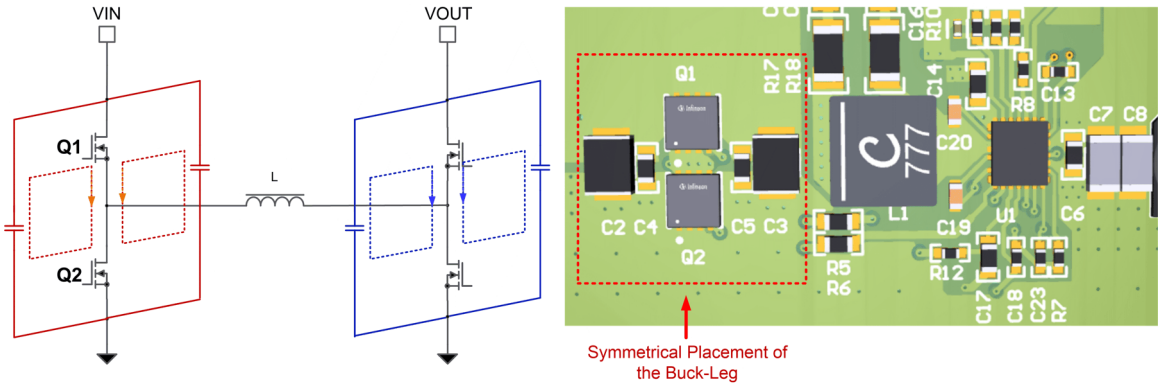

Figure 2-6. Symmetrical PCB Layout of TPS55288 Buck-Boost Converter

Figure 2-7 shows the radiated EMI result with symmetrical placement and without the symmetrical placement. Symmetrical placement helps reduce the radiated EMI in the 200MHz -600MHz high frequency range, the radiated EMI is improved by more than 6dBuV/m with symmetrical placement.

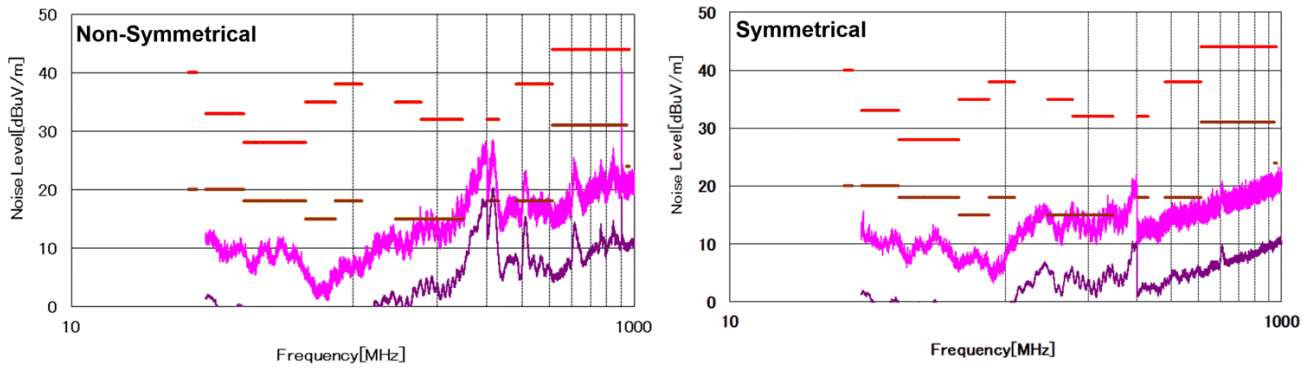

Figure 2-7. Radiated EMI Comparison with Symmetrical Placement

2.3.3 Using Frequency Dithering Function

When the above various techniques for mitigating the generation of EMI fail to provide enough noise suppression, and fail the required EMI test, extra filtering and shielding is needed to further reduce the noise. But the typical filtering and shielding EMI solutions add significant cost, size and weight to the circuit, especially in the automotive applications which need to pass the strict CISPR25 level5 limit. For some electrical control unit (ECU), the filtering and shielding solution occupy a high percentage of the total cost. The application of spread-spectrum dithering offers a simple and cost effective solution for the average EMI noise reduction.

The aim of the frequency dithering is to spread out the harmonics of the switching frequency fs concentrated at multiple integers of fs to a broad brand noise, see waveform in figure 8. The EMI noise is periodical with respect to the switching frequency. The emission centers at the switching frequency and its nth harmonics. With frequency dithering, the fundamental frequency changes from *fs*-Δ*f* to *fs*+Δ*f*, its nth harmonic spread from nx(*fs*-Δ*f) to nx(fs*+Δ*f)*. Hence the repetition of the fundamental frequency gets lower, so the measured quasi-peak and the average noise level gets lower, and the noise spectrum is broadened because of the side-band frequencies.

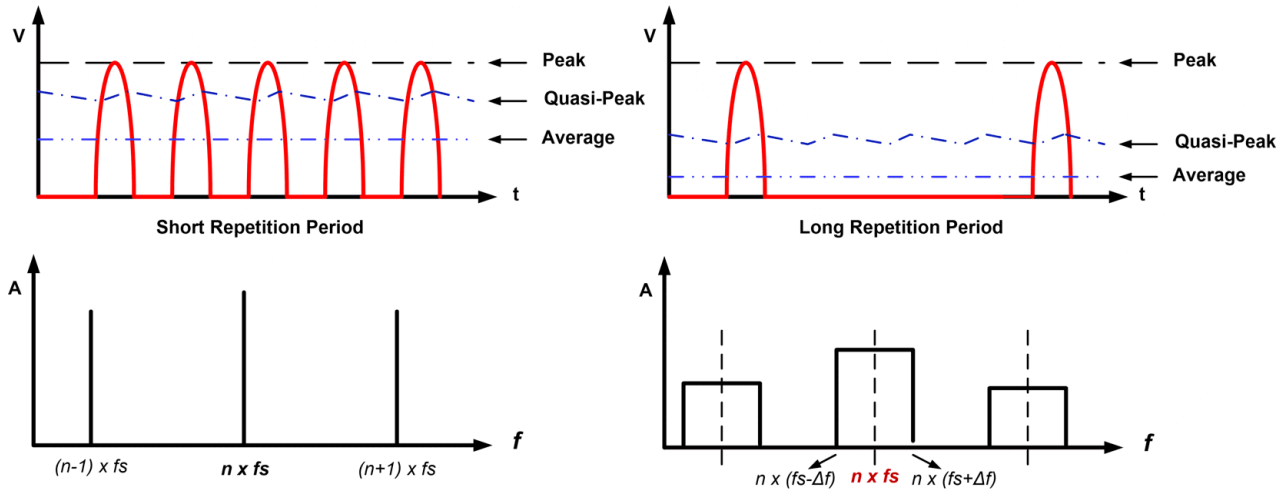

Figure 2-8. Benefits of Frequency Dithering

Figure 2-9 shows the comparison waveform with and without frequency dithering. Without frequency dithering, the average noise level is 2dB above the limit. With frequency dithering, like what we analyzed above, the noise shape change to a broad-band noise spectrum and the average noise level gets far below the limit.

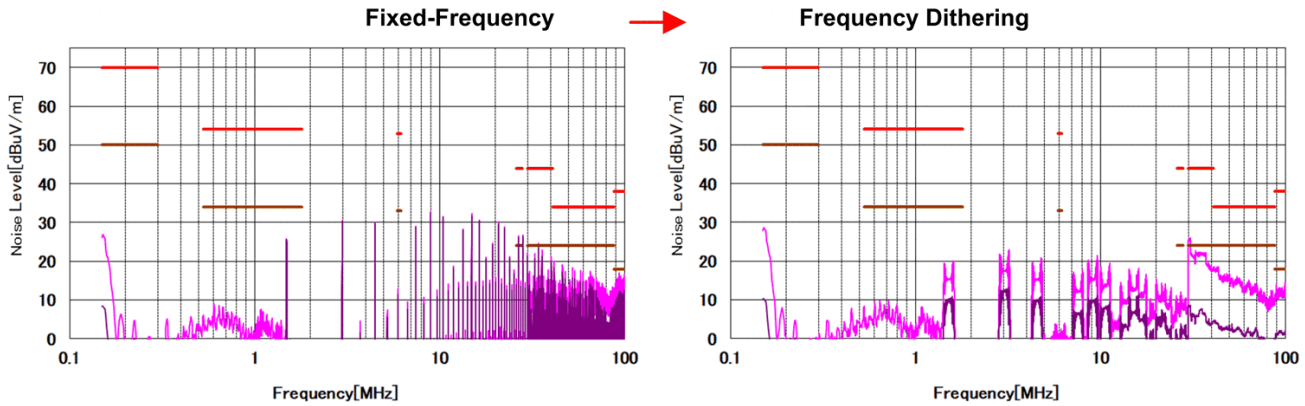

Figure 2-9. Conduction EMI Comparison with Frequency Dithering

2.3.4 Adding RC Snubbers at the Switching Node

The switching loop can be modeled as an LC circuit. It is formed by the input or output side decoupling capacitor and the high-side and low-side MOSFETs. For the buck-leg switching node SW1, the ringing occurs when the high side FET is on and the low side FET is off. For the boost-leg switching node SW2, the ringing occurs when the low side FET is off and the high side FET is on. Figure 2-10 shows the equivalent model of the switching loop during this transition state.

The inductance in the equivalent model (L_loop1 and L_loop2) corresponds to the total loop inductance of the switching loop, which includes PCB trace inductance, ESL of the decoupling capacitor and package inductance of the MOSFETs. The total capacitance of the loop is determined by the output capacitance of the low side MOSFET. Therefore, the switching node ringing frequency is determined by the parasitic loop inductance and the low side MOSFET output capacitance. For a given switching speed and given MOSFET, the maximum amplitude of the ringing is also determined by the parasitic loop inductance.

From the previous chapter, we know that the we can reduce the parasitic loop inductance by compact placement, by adding ground planes under the switching loop or by using symmetrical PCB layout. But in the real application, the component placement is limited by the PCB size.

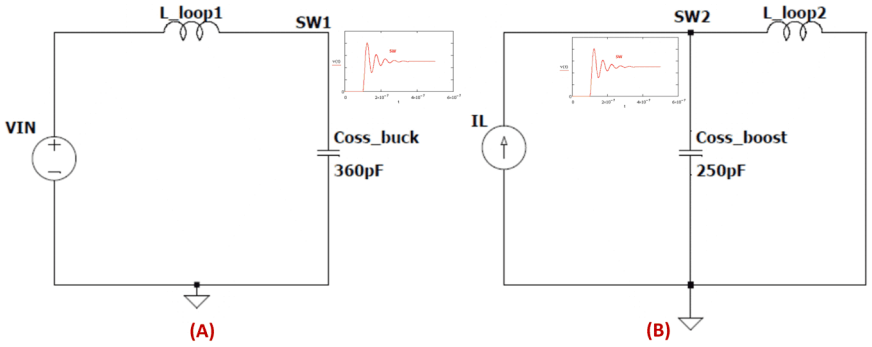

Figure 2-10. Equivalent Model of the Switching Loop

What we can do if the radiation EMI level still exceeds the requirement level and the layout cannot be improved anymore? Adding a RC snubber across the switching node and the power ground can help to reduce the radiation EMI levels. The RC snubber should be placed as close to the switching node and the ground plane as possible. Figure 2-11 shows the radiation EMI comparison result with and without RC snubber. The radiaton EMI is improved by around 6dBuV/m at 300MHz with RC snubber.

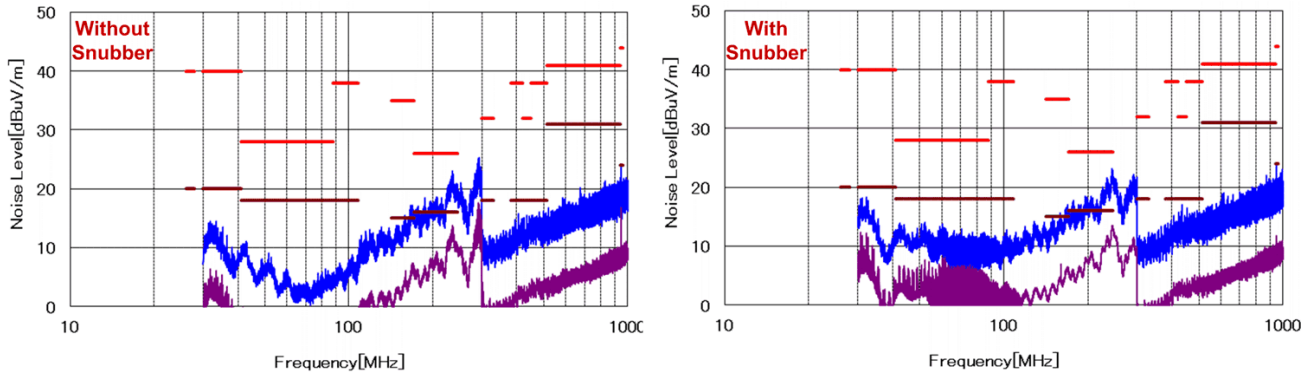

Figure 2-11. Radiation EMI Comparison with and without RC snubber

2.3.5 Adding Filters at the Input and Output Side

The discontinuous currents are present at the input and the output side of the buck-boost converter. Voltage ripple generated by the discontinuous current can be conducted to other systems via input and output cables or PCB traces. The selection of the input filter inductor and the output beads are based on the initial EMI noise test result.

When the converter works under the buck mode, generally CLC EMI filter should be added at the input side, see Figure 2-12. Many papers and articles write about this input filter design [3]. The typical procedure includes identify the noise level at the switching frequency, calculate the required attenuation, select the Lf and Cf, then calculate the damping capacitance Cd.

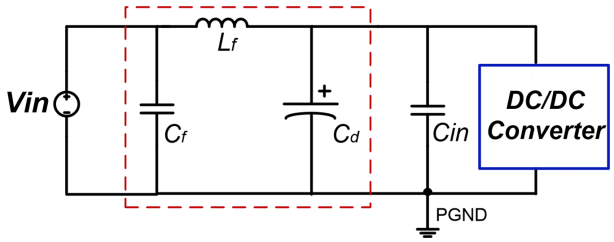

Figure 2-12. Simplified Input EMI Filter

When the converter works under the boost mode, ferrite beads are generally added at the output side. When selecting a bead, we should carefully study the impedance versus frequency characteristics when choosing a ferrite bead. Make sure the bead's resistive impedance is much higher than the reactive impedance in the noise frequency range. Figure 2-13 shows the Murata part BLM21PG300SN1's impedance versus frequency characteristic. We can see that this bead can provide optimum performance at noise frequencies from 100 MHz to 3 GHz range.

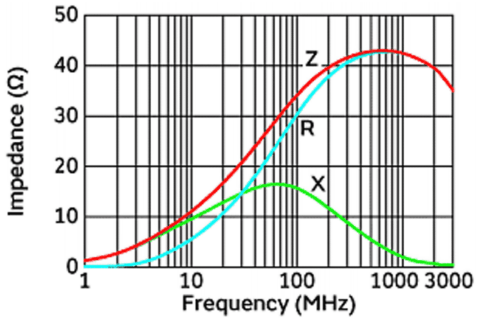

Figure 2-13. Impedance Characteristics of BLM21PG300SN1

3 Schematic and Test Result

Figure 3-1shows the schematic for the EMI test. One differential choke is added at the input side as the differential filter, two ferrite beads were added at the input side as the common mode filter.

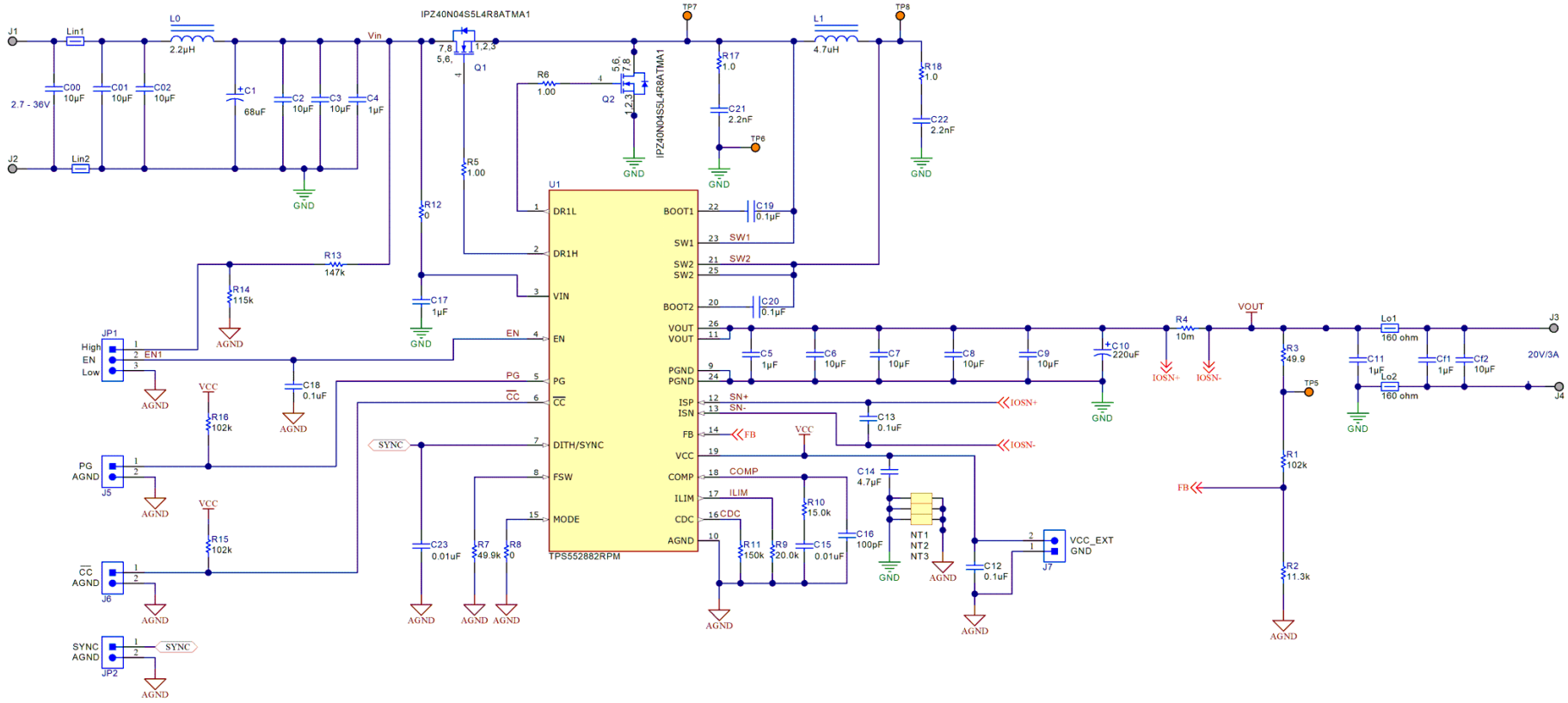

Figure 3-1. Schematic for the EMC Test

3.1 Test Result

Figure 3-2 shows the EMI test result under buck mode. Figure 3-3 shows the EMI test result under boost mode. It is clearly illustrated that both the conduction EMI and the radiation EMI passed the CISPR25 level 5 limit with more than 6-dB margin.

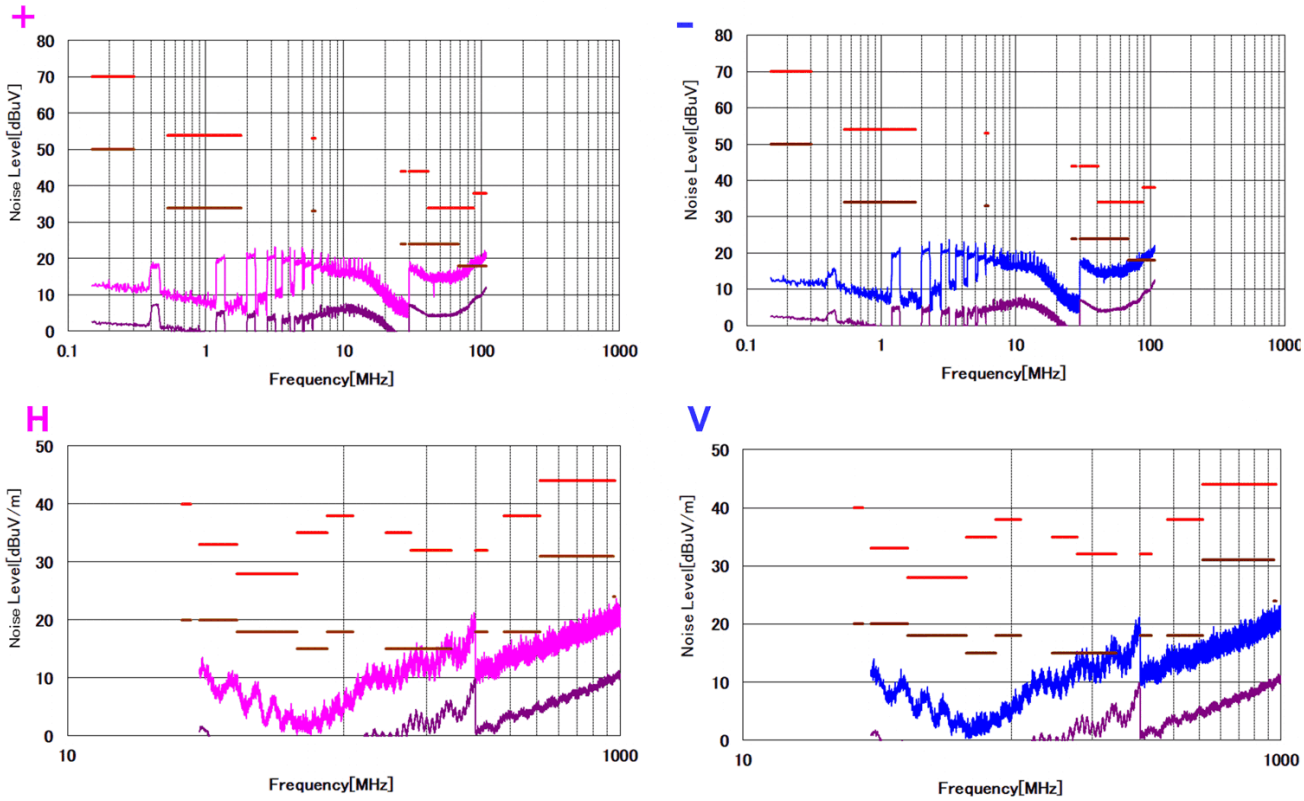

Figure 3-2. Buck Mode EMI Result (VIN = 12 V, VOUT = 5V / IOUT = 3A)

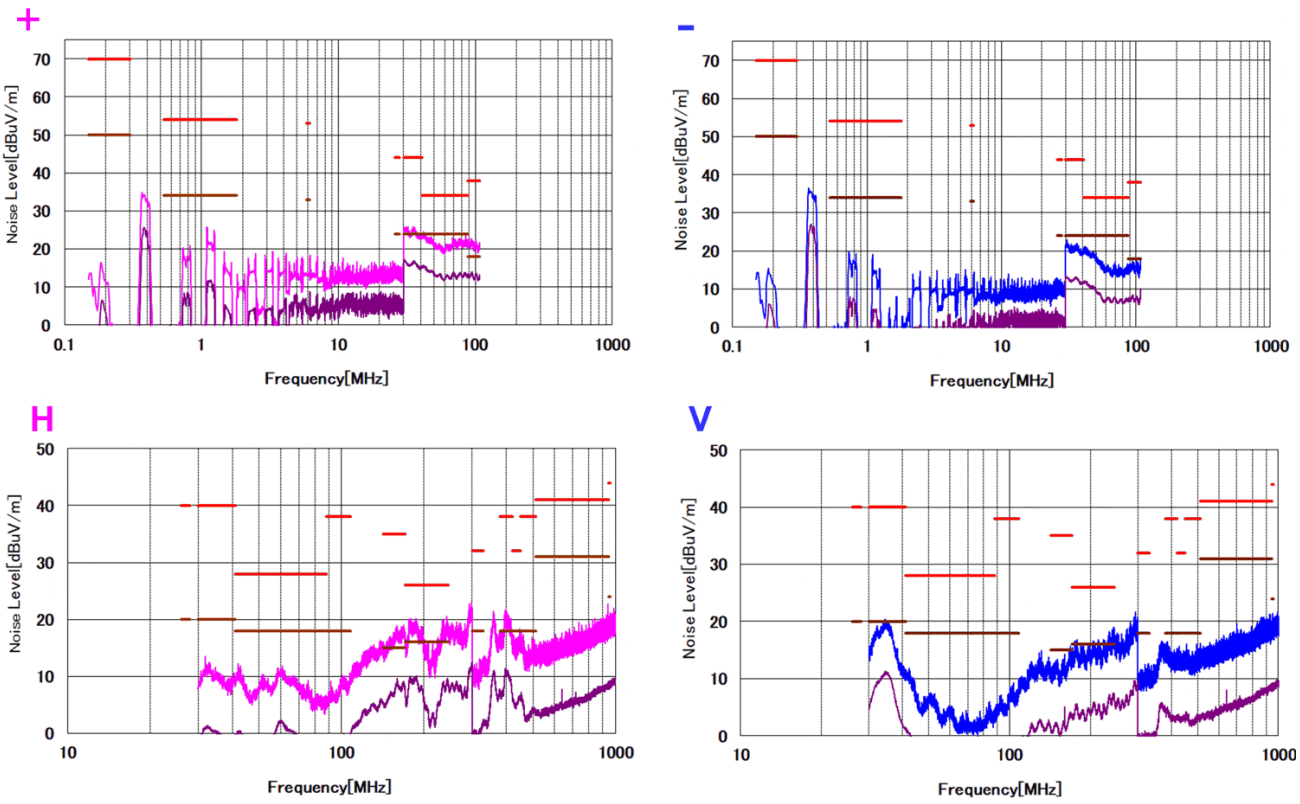

Figure 3-3. Boost Mode EMI Result (VIN = 12 V, VOUT = 20V / IOUT = 3A)

4 Summary

The major radiation sources in a buck-boost converter are the input and output switching loops. These critical loops should be as small as possible in order to reduce the radiation. We can reduce the switching loop by proper components placement. Putting a solid ground plane with minimum dielectric thickness under the switching loop can further reduce the equivalent switching loop. With the same component placement and same test condition, the radiated EMI is improved by more than 15dBuV/m with a 4-layer PCB. If the PCB size is not a limit, symmetrical placement of the decoupling capacitors can be adopted to achieve magnetic field cancellation. Frequency dithering technique is very helpful for the average EMI noise level reduction, it spread out the narrow band noise to a broad band noise, the average noise level gets much lower comparing to the no frequency dithering condition. For the high power and high frequency applications, adding a filter at the DC input side and output side also helps.

5 References

1. Texas Instruments, TPS55288 36-V, 16-A Buck-boost Converter with I2C Interface Data Sheet
2. Texas Instruments, Reducing Radiated EMI in TPS61088 Boost Converter Application Report
3. Texas Instruments, AN-2162 Simple Success With Conducted EMI From DC-DC Converters
4. Understanding the Effect of PCB Layout on Circuit Performance in a High Frequency Gallium Nitride Based Point of Load Converter

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265