Functional Safety Information

DRV8876-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for DRV8876-Q1 to aid in a functional safety system design. Information provided are:

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- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

DRV8876-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

Figure 1-1 shows the functional block diagram for reference.

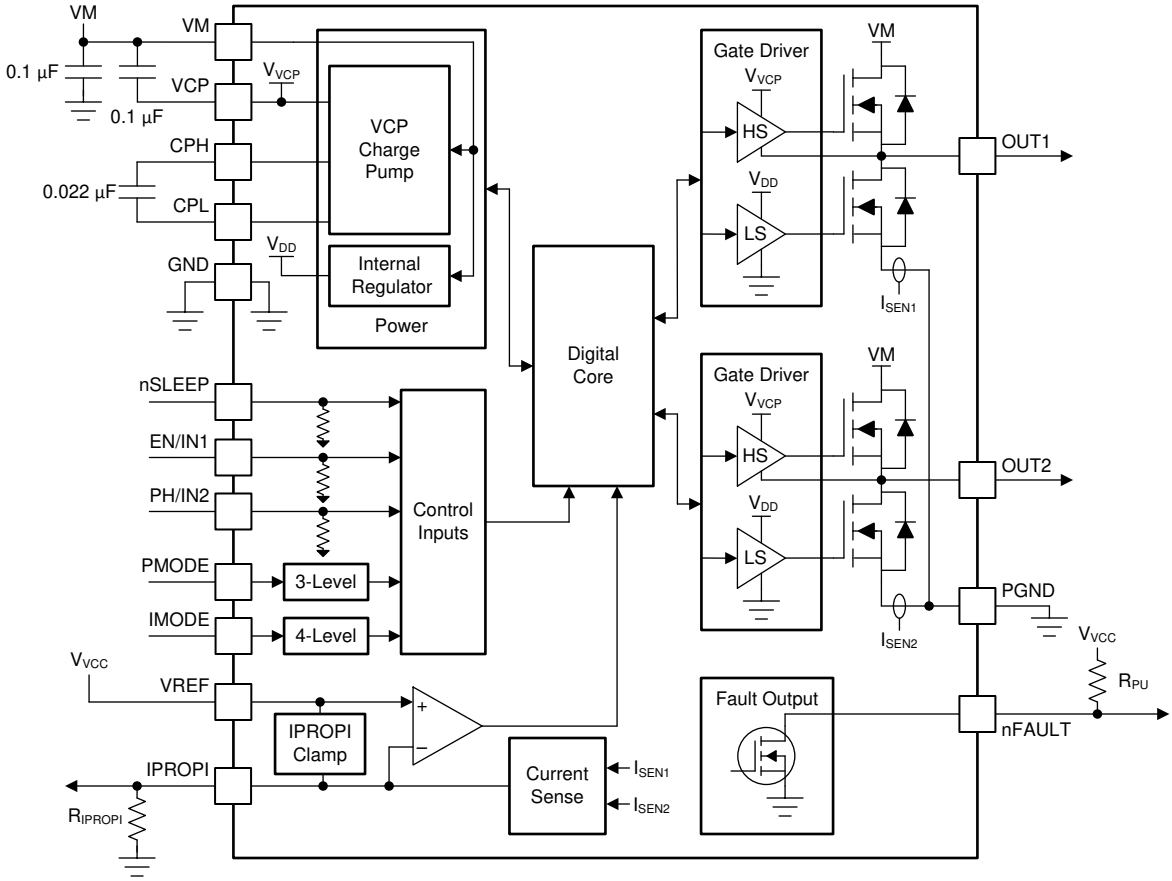

Figure 1-1. DRV8876-Q1 Device Block Diagram - HW variant

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for DRV8876-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	**17**
Die FIT Rate	**6**
Package FIT Rate	**11**

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: **0.730 W**
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	**CMOS, BICMOS Digital, analog / mixed**	**25 FIT**	**55°C**

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for DRV8876-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUTx is stuck LOW when commanded OFF	14%
OUTx is stuck OFF when commanded LOW	8%
OUTx ON resistance too high when commanded LOW	12%
Low side slew rate too fast or too slow	5%
OUTx is stuck HIGH when commanded OFF	14%
OUTx is stuck OFF when commanded HIGH	8%
OUTx ON resistance too high when commanded HIGH	17%
High side slew rate too fast or too slow	5%
Dead-time is too short	1%
Current sense feedback incorrect	3%
ITRIP current regulation incorrect	3%
Incorrect communication or fault indication	10%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the DRV8876-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4}
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 HTSSOP Package

Figure 4-1 shows the DRV8876-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the DRV8876-Q1 datasheet.

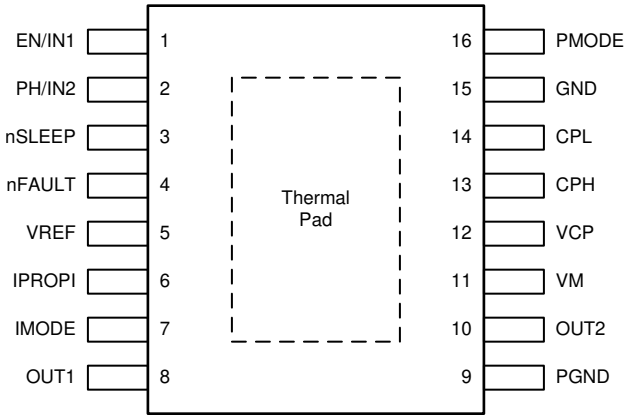

Figure 4-1. DRV8876-Q1 Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is used with external components consistent with the values described in the external component table of the datasheet.

Table 4-2. HW variant - Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/IN1	1	OUTx driver control will be lost	B
PH/IN2	2	OUTx driver control will be lost	B
nSLEEP	3	Device will be in sleep state with OUTx HiZ	B
nFAULT	4	Device will always be signaling fault	B
VREF	5	Sets current regulation limit I_{TRIP} = 0 A	B
IPROPI	6	Current sensing and regulation capability will be lost	B
IMODE	7	Device IMODE configuration may be misinterpreted	B
OUT1	8	OUTx HiZ, with device signaling fault	B
PGND	9	Intended operation	D
OUT2	10	OUTx HiZ, with device signaling fault	B

Table 4-2. HW variant - Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VM	11	Device will not power up	B
VCP	12	Device will be damaged with higher current draw from VM	A
CPH	13	Device will be damaged with higher current draw from VM	A
CPL	14	Device will be damaged with higher current draw from VM	A
GND	15	Intended operation	D
PMODE	16	Device PMODE configuration may be misinterpreted	B

Table 4-3. HW variant - Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/IN1	1	OUTx driver control will be lost	B
PH/IN2	2	OUTx driver control will be lost	B
nSLEEP	3	Device will be in sleep state with OUTx HiZ	B
nFAULT	4	Fault signaling will be lost	B
VREF	5	Undefined I_{TRIP} current	B
IPROPI	6	Current sensing and regulation capability will be lost	B
IMODE	7	Device IMODE configuration may be misinterpreted	B
OUT1	8	OUTx impedance will be higher - device will not be able to drive the load properly	B
PGND	9	Device will not power up	B
OUT2	10	OUTx impedance will be higher - device will not be able to drive the load properly	B
VM	11	Device will not power up	B
VCP	12	Charge pump unstable, possible damage to charge pump	A
CPH	13	OUTx HiZ, with device signaling fault	B
CPL	14	OUTx HiZ, with device signaling fault	B
GND	15	Device will not power up	B
PMODE	16	Device PMODE configuration may be misinterpreted	B

Table 4-4. HW variant - Pin FMA for Device Pins Shorted to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/IN1	1	2	OUTx driver control will be lost	B
PH/IN2	2	3	OUTx driver control will be lost	B
nSLEEP	3	4	Device will go into sleep state whenever nFAULT is asserted low, device damage may occur if nFAULT sinks excess current from nSLEEP signal	A
nFAULT	4	5	Device damage may occur if nFAULT sinks excess current from VREF signal	A
VREF	5	6	Current regulation capability will be lost, OUTx driver control will be lost	B
IPROPI	6	7	Current sensing and regulation capability will be lost	B
IMODE	7	8	Device will be damaged with higher current draw from VM	A
OUT1	8	9	OUTx HiZ with device signaling fault	B
PGND	9	10	OUTx HiZ with device signaling fault	B
OUT2	10	11	OUTx HiZ with device signaling fault	B
VM	11	12	OUTx HiZ with device signaling fault	B
VCP	12	13	Device will be damaged with higher current draw from VM	A
CPH	13	14	Device will be damaged with higher current draw from VM	A
CPL	14	15	Device will be damaged with higher current draw from VM	A

Table 4-4. HW variant - Pin FMA for Device Pins Shorted to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	15	16	Device PMODE configuration may be misinterpreted	B
PMODE	16	1	OUTx driver control will be lost	B

Table 4-5. HW variant - Pin FMA for Device Pins Shorted to VM (High Voltage Supply)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
EN/IN1	1	Device will be damaged with higher current draw from VM	A
PH/IN2	2	Device will be damaged with higher current draw from VM	A
nSLEEP	3	Device will be damaged with higher current draw from VM	A
nFAULT	4	Device will be damaged with higher current draw from VM	A
VREF	5	Device will be damaged with higher current draw from VM	A
IPROPI	6	Device will be damaged with higher current draw from VM	A
IMODE	7	Device will be damaged with higher current draw from VM	A
OUT1	8	OUTx HiZ with device signaling fault	B
PGND	9	Device will not power up	B
OUT2	10	OUTx HiZ with device signaling fault	B
VM	11	Intended operation	D
VCP	12	OUTx HiZ with device signaling fault	B
CPH	13	Device will be damaged with higher current draw from VM	A
CPL	14	Device will be damaged with higher current draw from VM	A
GND	15	Device will not power up	B
PMODE	16	Device will be damaged with higher current draw from VM	A

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