Application Report

Hermetic Package Reflow Profiles, Termination Finishes, and Lead Trim and Form

ABSTRACT

Hermetic microcircuits are still widely used in mission-critical aerospace, defense, and industrial applications. Customers occasionally have questions regarding board-level assembly of these packages. A general set of guidelines are addressed in this application note.

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Trademarks

1 Reflow Profiles

Board-level solder reflow profiles are dependent on numerous factors including, but not limited to, solder type, flux, package type, the number of components, the number of board layers, the board size, reflow oven type, and accuracy as well as pre- and post-cleaning processes. Because of the number of variables it is not possible to provide a single reflow profile that is representative of every board using a specific package type. Typically, manufacturing houses have reflow profiles in place and modify them for specific hardware.

TI suggests using the flux manufacturer's recommended profile as a starting point. Variations of course need to be comprehended based on the time required to volatize the flux prior to the solder reaching liquidus. In general, ceramic parts are compatible with ramp-up rates of < 3°C/s and ramp-down rates of < 6°C/s with a maximum peak temperature of 260°C.

A hermetic package will withstand three passes of reflow if the peak temperature and ramp rates are not exceeded.

Most metal lid packages use an 80%Au-20%Sn solder preform to attach the lid. Gold-tin solder will begin to soften at 270°C and has a eutectic point of 280°C. The package body temperature must not exceed 260°C at any time or the hermetic seal of the package will be damaged. Note that through-hole hermetic devices specify a maximum temperature for soldering as a lead-temperature of 300°C for 10 seconds. This is not a reflow temperature.

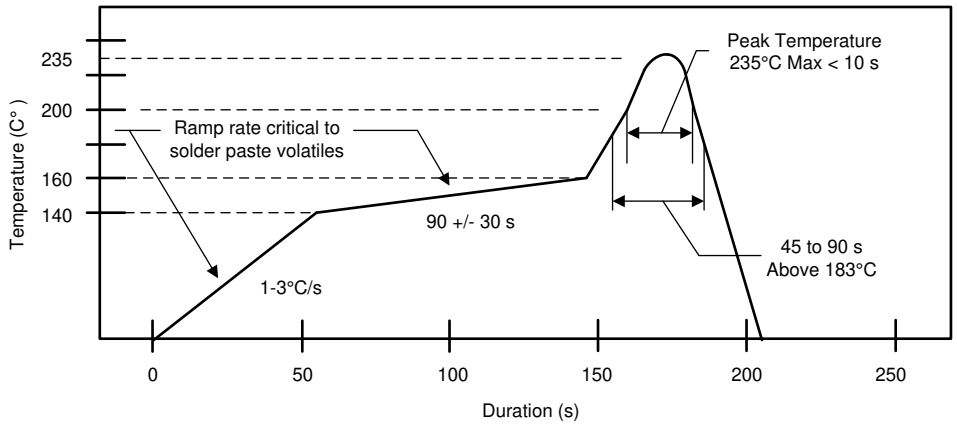

Figure 1-1. Starting Profile for Typical Pb/Sn Solder Paste

2 Critical Considerations for Gold-Plated Termination-Finishes

TI offers a variety of termination finishes for compliant hermetic packages, for example:

- Alloy-42 leads with Sn63Pb37 hot solder dip.
- Alloy-42 or Kovar leads with 50µ-in to 350 µ-in of nickel underplate and 60 µ-in to 225 µ-in of gold finish plate
- Alloy-42 or Kovar leads with 50µ-in to 350 µ-in of nickel underplate and SN63Pb37 hot solder dip

Table 2-1. MIL-PRF-38535 TABLE A-III Composition and Coating Thickness Requirements

Coating	Minimum	Maximum
Hot solder dip (for all round leads)	60 µ-in	Not Specified
Hot solder dip (for all shapes other than round leads which have ≤ 25 mil pitch)	150 µ-in	Not Specified
Hot solder dip (for all shapes other than round leads with > 25 mil pitch)	200 µ-in	Not Specified
Tin-lead plate (as plated)	300 µ-in	Not Specified
Tin-lead plate (fused)	200 µ-in	Not Specified
Gold plate	50 µ-in	225 µ-in
Nickel plate (electroplate)	50 µ-in	350 µ-in
Nickel plate (electroless)	50 µ-in	250 µ-in
Nickel cladding	50 µ-in	350 µ-in

The electronics industry currently recognizes a threshold level of 3% gold by weight that can be dissolved into eutectic tin-lead solder above which the solder-joint may exhibit gold embrittlement.

With the specified gold thickness it is recommended that gold-plated leads be pre-tinned (solder-dipped) before board mounting to scavenge the gold from the leads. If this is not done, there is a chance of gold-embrittlement of the board-level solder-joints. A flowing solder-pot or two passes in a static solder-pot is recommended. Solder-pot solder composition should be periodically monitored for gold content.

3 Considerations for Leadless Ceramic Chip Carrier Packages

The critical items for board-level solder process for a Leadless Ceramic Chip Carrier (LCCC) package are solder paste thickness and depth of package insertion into the paste during pick and place.

- If the paste under the package is too thin it will result in a poor solder joint.
- Too much solder paste can cause excess solder on the sides of the package.
- If the package is placed too far into the paste (too close to the board) it can cause excess solder on the sides of the package.
- The solder should adhere to the pads on the package backside and flow up the castellation.
- The package should be parallel to the board (no tilt).
- The package needs to be aligned to the pads.
- The circuit board pads should be sized to fit the pads on the underside of the package and allow for a fillet on the sides.
- Placement depth should be consistent.
- With mixed package types on the board the actual reflow temperature of the LCCC component should be measured (thermocouple on package via thermally conductive epoxy).

4 Lead Forming

Hermetic surface mount packages are typically sold non-formed as most customers have a preferred final form factor which can vary from customer to customer. Some use the default form factor available from third party service providers such as Fancort or Corfin. For reference, Fancort maintains a library of form factors on their website at Standard SMT Footprints. Fancort can also provide a lead-forming service or sell the fixtures for a customer to form in house. General information is found at Lead Forming Services. TI does not endorse or recommend these companies but only mentions them as example service providers.

For more information, contact TI Support at www.ti.com/support.

5 Ceramic Packaging

The following table is a snapshot for reference purposes and may not be current. For package specific information and application notes, see http://www.ti.com/support-packaging/packaging-information.html.

Package Group	Description	Designator
CBGA	Ceramic Ball Grid Array	GJN,GLE,GLG,GLK,GNM
CCGA	Ceramic Column Grid Array	NAA,NWE
CDBGA	Ceramic Dimpled Ball Grid Array	GFP,GGP,GGR,GGZ,GHF,GHM,GJM,GKG,ZGR, ZHM
CDIP	Ceramic Dual Inline Package	J,JG,JL,JNA,JNC,JND,JT,JTA,JTB,JTC,NAB,NAY, NAZ,NFE
CDIP-BB	Ceramic Dual Inline Package – Bottom Braze	JDE,JDG
CDIP-SB	Ceramic Dual Inline Package – Side Braze	JC,JD,JDC,JDD,JDJ,JDK,JDM,JDN,JN,JVA,JVB, JVD,JVE,JVF,NAK
CFCBGA	Ceramic Flip Chip Ball Grid Array	AAD,CDZ,CMA,CME,CMQ,CTF,CTJ,CTK,CUB, CUD,CUM,CYC,GDZ,GLL,GLP,GMA,GME, GTF,GTH,GTJ,GTK,GTQ,GUD,GUE,GUF,GUM, ZDZ,ZUF
CFP	Ceramic Flat Pack	FAA,HAJ,HAY,HBC,HBD,HBE,HBU,HBY,HD,HE,HF,HFD,HFG,HFH,HFL,HFN,HFP,HFQ, HFR,HFS,HG,HGA,HGF,HH,HKB,HKC,HKD,HKE,HKH,HKJ,HKK,HKN,HKP,HKQ,HKR,HKS, HKT,HKU,HKV,HKW,HKX,HKY,HR,HT,HV,HY, HZ,NAD,PHF,PHG,U,W,WA,WD,WH,WJ,WN
CFP	Ceramic Flat Pack - Gullwing Formed Leads	NAC
CLGA	Ceramic Land Grid Array	FVA, NAF,ZMA,ZMX
CPGA	Ceramic Pin Grid Array	GA,GB,GC,GE,GF,GFA,NAQ,NAR,NAT
CQFP	Ceramic Quad Flat Pack	NAU,NBA,NBB,NBC
CTO-92	Ceramic Transistor Outline 92	HTA
CZIP	Ceramic Zig-Zag Inline Package	SV
JLCC	J Lead Ceramic Chip Carrier	FJ,FZ,HJ,HJA

Package Group	Description	Designator
LCCC	Leadless Ceramic Chip Carrier	FD,FE,FFA,FFC,FFD,FFE,FFF,FFH,FFJ,FFK,FK, FKH,FNC,FPH,FPM,FQ,HL,HM,NAJ
TO-CAN	Transistor Outline [Metal] Can	K,LMC,LMD,LME,LMF,LMG,NDS,NDT,NDU, NDV,NEP,NEQ,NER

6 References

- MIL-PRF-38535 *General Specification for Integrated Circuits (Microcircuits) Manufacturing*
- MIL-STD-883 *Test Methods and Procedures for Microcircuits*

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