Functional Safety Information

TPS7B82-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS7B82-Q1 (DGN, DRV, and KVU packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

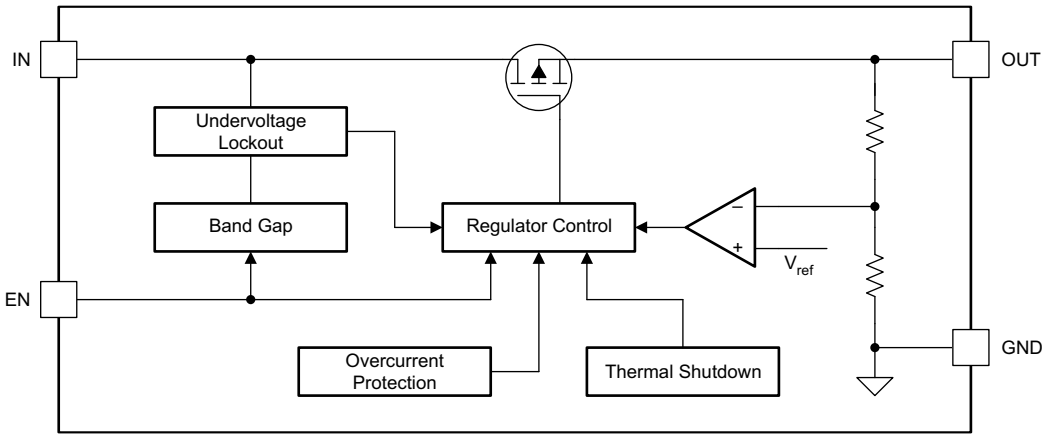

Figure 1-1. Functional Block Diagram

TPS7B82-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPS7B82-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)		
Package	HVSSOP-8 (DGN)	WSON-6 (DRV)	TO-252-5 (KVU)
Total Component FIT Rate	9	8	16
Die FIT Rate	5	6	4
Package FIT Rate	4	2	12

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 300 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	Power Amplifier and Regulator =< 1Watt - (LDO)	40 FIT	70°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS7B82-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No Output	45%
Output high (following Input)	15%
Output not in specification	35%
Short circuit on any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS7B82-Q1 (DGN, DRV, and KVU packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2, Table 4-6 and Table 4-10.)
- Pin open-circuited (see Table 4-3, Table 4-7 and Table 4-11)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8 and Table 4-12)
- Pin short-circuited to VBAT (see Table 4-5, Table 4-9 and Table 4-13)

Table 4-2 through Table 4-13 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 DGN Package

Figure 4-1 shows the TPS7B82-Q1 pin diagram for the DGN package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS7B82-Q1 data sheet.

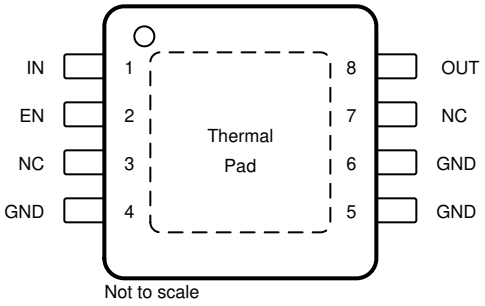

Figure 4-1. Pin Diagram (DGN) Package, Top View:

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No power supplied to device resulting in no output voltage.	B
EN	2	Device stuck in shutdown mode resulting in no output voltage.	B
NC	3	No effect. Normal Operation.	D
GND	4	No effect. Normal Operation.	D
GND	5	No effect. Normal Operation.	D
GND	6	No effect. Normal Operation.	D
NC	7	No effect. Normal Operation.	D
VOUT	8	Device not operational with output being pulled to GND. Current limit is triggered, and device may repeat entering and exiting thermal shutdown depending on power dissipation.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No power supplied to device resulting in no output voltage.	B
EN	2	Device will flip between shutdown mode and normal mode due to noise on EN voltage. Could result in no output voltage.	B
NC	3	No effect. Normal Operation.	D
GND	4	Floating GND pin could result in incorrect voltage regulation or no output voltage.	B
GND	5	Floating GND pin could result in incorrect voltage regulation or no output voltage.	B
GND	6	Floating GND pin could result in incorrect voltage regulation or no output voltage.	B
NC	7	No effect. Normal Operation.	D
VOUT	8	Output disconnected from the load.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	EN	2	EN pulled to IN supply. No shutdown mode possible. Device will be powered on as long as input supply is present.	D
EN	2	NC	3	No effect. Normal Operation.	D
NC	3	GND	4	No effect. Normal Operation.	D
GND	5	GND	6	No effect. Normal Operation.	D
GND	6	NC	7	No effect. Normal Operation.	D
NC	7	VOUT	8	No effect. Normal Operation.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No effect. Normal Operation.	D
EN	2	EN pulled to VBAT. No shutdown mode possible. Device will be powered on as long as VBAT is present.	C
NC	3	No effect. Normal Operation.	D
GND	4	VBAT may be discharged if other GND connections on device are still tied to GND. If all pins are floated to VBAT this could result in VOUT seeing VBAT voltage.	B
GND	5	VBAT may be discharged if other GND connections on device are still tied to GND. If all pins are floated to VBAT this could result in VOUT seeing VBAT voltage.	B
GND	6	VBAT may be discharged if other GND connections on device are still tied to GND. If all pins are floated to VBAT this could result in VOUT seeing VBAT voltage.	B
NC	7	No effect. Normal Operation.	D
VOUT	8	VOUT pin could be damaged and load being powered by TPS7B82-Q1 will see VBAT voltage.	A

4.2 DRV Package

Figure 4-2 shows the TPS7B82-Q1 pin diagram for the DRV package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS7B82-Q1 data sheet.

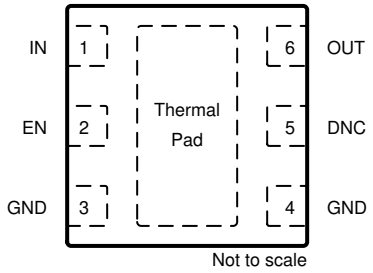

Figure 4-2. Pin Diagram (DRV Package, Top View)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No power supplied to device resulting in no output voltage.	B
EN	2	Device stuck in shutdown mode resulting in no output voltage.	B
GND	3	No effect. Normal Operation.	D
GND	4	No effect. Normal Operation.	D
DNC	5	No effect. Normal Operation.	D
VOUT	6	Device not operational with output being pulled to GND. Current limit is triggered, and device may repeat entering and exiting thermal shutdown depending on power dissipation.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No power supplied to device resulting in no output voltage.	B
EN	2	Device will flip between shutdown mode and normal mode due to noise on EN voltage. Could result in no output voltage.	B
GND	3	Floating GND pin could result in incorrect voltage regulation or no output voltage.	B
GND	4	Floating GND pin could result in incorrect voltage regulation or no output voltage.	B
DNC	5	No effect. Normal Operation.	D
VOUT	6	Output of device disconnected from the load.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	EN	2	EN pulled to IN supply. No shutdown mode possible. Device will be powered on as long as input supply is present.	D
EN	2	GND	3	Device stuck in shutdown mode resulting in no output voltage.	B
GND	4	DNC	5	No effect. Normal Operation.	D
DNC	5	VOUT	6	VOUT can fall out of regulation or increased quiescent current could be observed.	C

Table 4-9. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No effect. Normal Operation.	D
EN	2	EN pulled to VBAT. No shutdown mode possible. Device will be powered on as long as VBAT is present.	C
GND	3	VBAT may be discharged if other GND connections on device are still tied to GND. If all pins are floated to VBAT this could result in VOUT seeing VBAT voltage.	B
GND	4	VBAT may be discharged if other GND connections on device are still tied to GND. If all pins are floated to VBAT this could result in VOUT seeing VBAT voltage.	B
DNC	5	VOUT can fall out of regulation or increased quiescent current could be observed.	C
VOUT	6	VOUT pin could be damaged and load being powered by TPS7B82-Q1 will see VBAT voltage.	A

4.3 KVU Package

Figure 4-2 shows the TPS7B82-Q1 pin diagram for the KVU package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS7B82-Q1 data sheet.

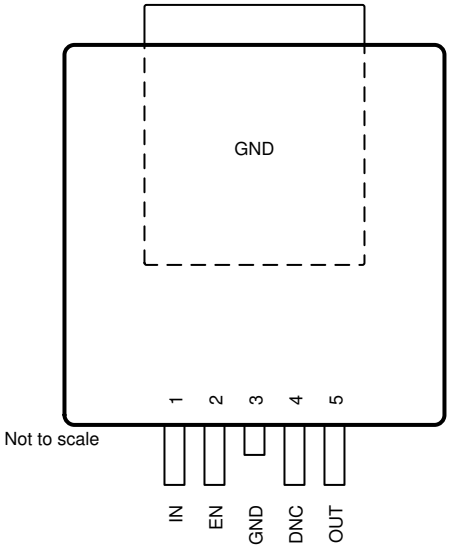

Figure 4-3. Pin Diagram (KVU Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No power supplied to device resulting in no output voltage.	B
EN	2	Device stuck in shutdown mode resulting in no output voltage.	B
GND	3	No effect. Normal Operation.	D
DNC	4	No effect. Normal Operation.	D
VOUT	5	Device not operational with output being pulled to GND. Current limit is triggered, and device may repeat entering and exiting thermal shutdown depending on power dissipation.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No power supplied to device resulting in no output voltage.	B
EN	2	Device will flip between shutdown mode and normal mode due to noise on EN voltage. Could result in no output voltage.	B
GND	3	Floating GND pin could result in incorrect voltage regulation or no output voltage.	B
DNC	4	No effect. Normal Operation.	D
VOUT	5	Output of device disconnected from the load.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	EN	2	EN pulled to IN supply. No shutdown mode possible. Device will be powered on as long as input supply is present.	D
EN	2	GND	3	Device stuck in shutdown mode resulting in no output voltage.	B
GND	3	DNC	4	No effect. Normal Operation.	D
DNC	4	VOUT	5	VOUT can fall out of regulation and increased quiescent current could be observed.	C

Table 4-13. Pin FMA for Device Pins Short-Circuited to VBAT

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	1	No effect. Normal Operation.	D
EN	2	EN pulled to VBAT. No shutdown mode possible. Device will be powered on as long as VBAT is present.	C
GND	3	VBAT may be discharged if other GND connections on device are still tied to GND. If all pins are floated to VBAT this could result in VOUT seeing VBAT voltage.	B
DNC	5	VOUT can fall out of regulation and increased quiescent current could be observed.	C
VOUT	6	VOUT pin could be damaged and load being powered by TPS7B82-Q1 will see VBAT voltage.	A

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