Functional Safety Information

TPS2H160-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for TPS2H160-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

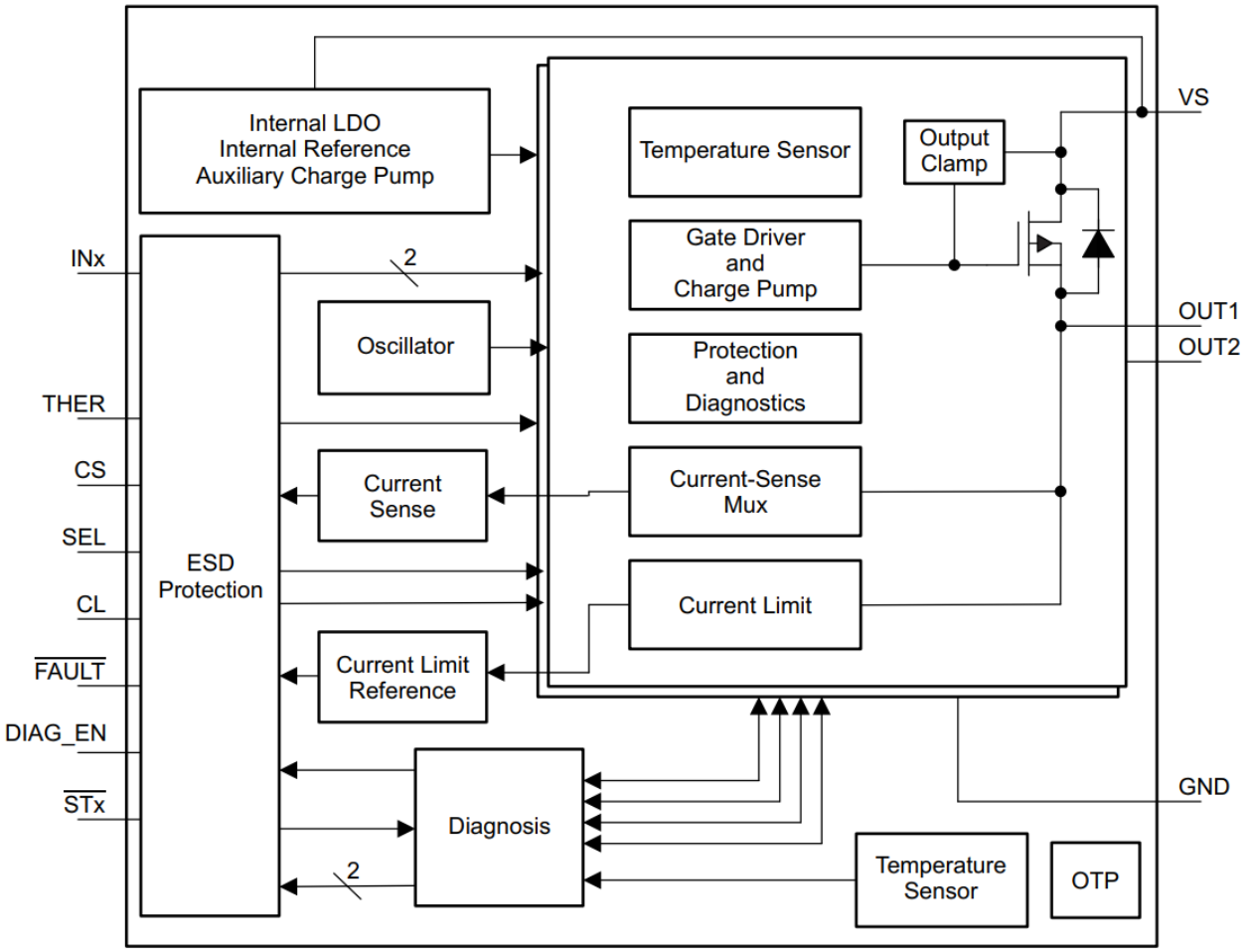


Figure 1-1. Functional Block Diagram

TPS2H160-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS2H160-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	6
Package FIT Rate	10

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 500 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	Digital, Analog, Mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS2H160-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT1,2 open (HiZ)	20%
OUT1,2 stuck on (VS)	10%
OUT1,2 not in specification voltage or timing	45%
Diagnostics not in specification	10%
Protect functions fails to trip	5%
Pin to Pin short any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS2H160-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply

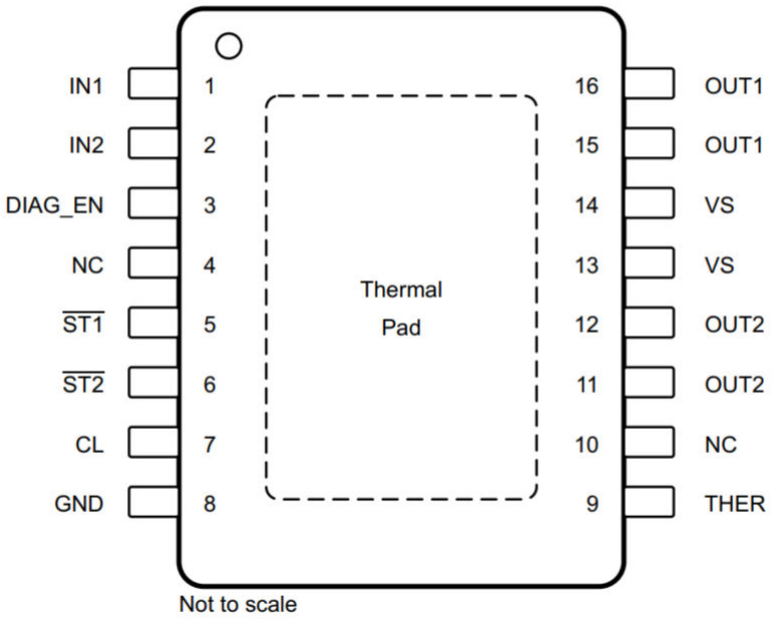
Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS2H160-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS2H160-Q1 data sheet.

PWP PowerPAD™ Package
16-Pin HTSSOP With Exposed Thermal Pad
TPS2H160-Q1 Version A Top View



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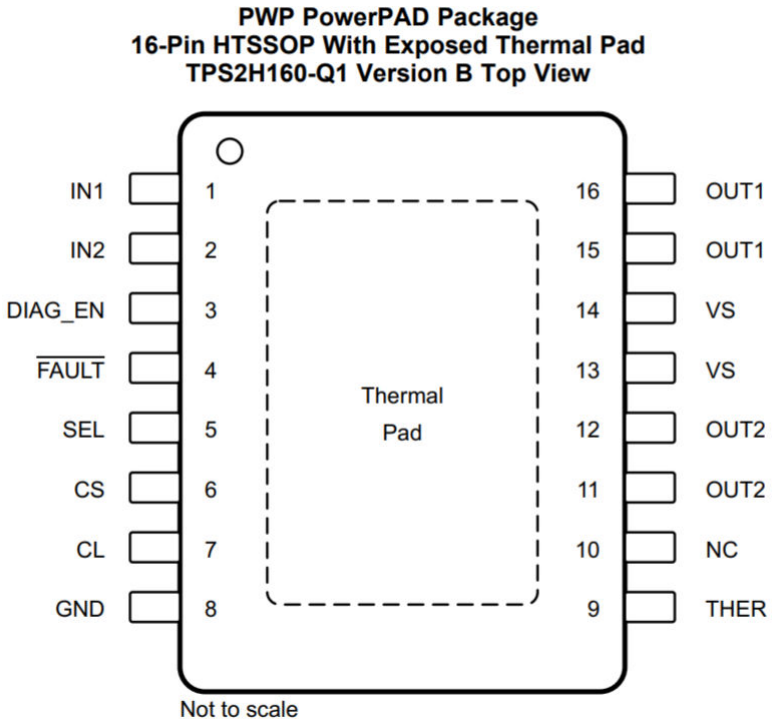

Figure 4-1. Pin Diagram

The pin FMA is provided under the assumption that the device is operating under the specified ranges within the *Recommended Operating Conditions* section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
INx	1,2	Shutdown of corresponding channel	B
DIAG_EN	3	Diagnostics will be disabled	B
NC	4,10	Pin 4 is NC for Version A only. No effect	D
FAULT	4	Version B only: Fault status reported may be erroneous	B
STx	5,6	Version A only: Status being reported may be erroneous	B
SEL	5	Version B only: If DIAG_EN is high then channel 1's sense current output always on SNS	B
CS	6	Version B only: Sense current not valid from CS pin	B
CL	7	Device will default to internal current limit	C
GND	8	Resistor/diode network will be bypassed if present	B
THER	9	Device will default to "auto-retry" mode when encountering thermal fault	B
OUTx	11,12,15, 16	Current limit of device will engage	B
VS	13,14	Device will have no input supply and therefore not function	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
INx	1,2	Corresponding channel will be shutdown and INx will be pulled down internally	B
DIAG_EN	3	Diagnostics will be disabled with device as pin will be pulled down internally	B
NC	4,10	Pin 4 is NC for Version A only. No effect	D
FAULT	4	Version B only: Fault signal not reported	B

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
STx	5,6	Version A only: STx pin cannot pull high and diagnostics cannot be reported	B
SEL	5	Version B only: Pin pulled low internally, however wrong SNS current potentially reported on CS if DIAG_EN is high	B
CS	6	Correct CS current cannot be read	B
CL	7	Channel 1 and 2 will not be able to provide output current	B
GND	8	Loss of ground detection engages and device shuts off	B
THER	9	Internally pulled down and device will default to "auto-retry" mode when encountering thermal fault	B
OUTx	11,12,15,16	No effect. If configured, open load detection will trigger	B
VS	13,14	Device will have no input supply and therefore not function	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN1	1	IN2	IN1 signal will affect IN2 signal and vice versa	B
IN2	2	DIAG_EN	IN2 signal will affect DIAG_EN signal and vice versa	B
DIAG_EN	3	NC	Version A only. No effect	D
DIAG_EN	3	FAULT	Version B only. Signal of DIAG_EN could affect FAULT signal and vice versa	B
NC	4	ST1	Version A only. No effect	D
FAULT	4	SEL	Version B only. FAULT status could affect SEL signal and vice versa	B
ST1	5	ST2	Version A only. False ST1 status could be reported on ST2 and vice versa	B
SEL	5	CS	Version B only. Signal on SEL could affect signal on CS pin and vice versa	B
ST2	6	CL	Version A only. If ST2 is high then and channel 1 and channel 2 will not be able to provide output current. If ST2 is low the internal current limit will be set	B
CS	6	CL	Version B only. Voltage level on CS could cause erroneous current limit to be set on device	B
CL	7	GND	Device will default to internal current limit	B
THER	9	NC	No effect	D
NC	10	OUT2	No effect	D
OUT2	11	OUT2	No effect	D
VS	13	VS	No effect	D
VSx	12,15	VOUTx	Output will be pulled supply voltage. Short-to-battery detection will be triggered if configured	B
OUT1	15	OUT1	No effect	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
INx	1,2	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
DIAG_EN	3	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
NC	4,10	Pin 4 is NC on Version A only. Pins not internally connected	D
FAULT	4	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
SEL	5	Version B only. Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to supply (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
STx	5,6	Version A only: Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
CS	6	Version B only: Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
CL	7	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
GND	8	Supply power will be bypassed and device will not turn on	B
THER	9	Potential violation of absolute maximum rating of pin and possible breakdown of ESD cell	A
OUTx	11,12,15,16	Output will be pulled supply voltage. Short-to-battery detection will be triggered if configured	B

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