Functional Safety Information

TPS6281x-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS62810-Q1, TPS62811-Q1, TPS62812-Q1, TPS62813-Q1 (VQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards.
- Component failure modes and their distribution (FMD) based on the primary function of the device.
- Pin failure mode analysis (Pin FMA).

Figure 1-1 shows the device functional block diagram for reference.

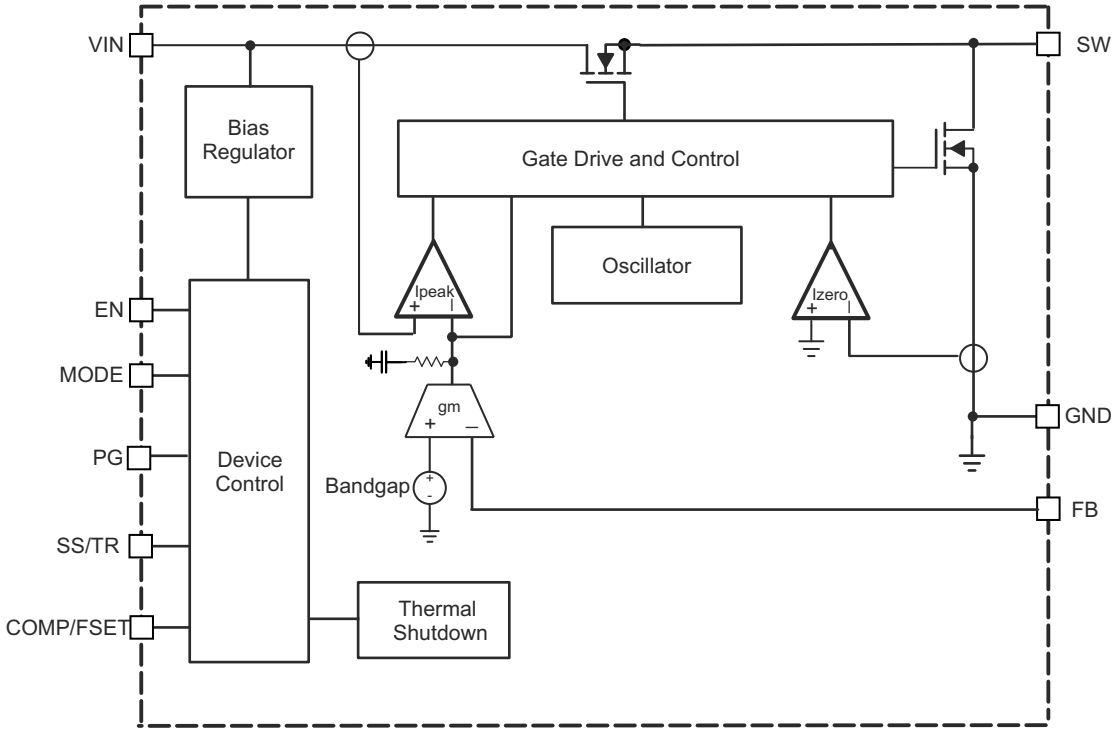

Figure 1-1. Functional Block Diagram

TPS6281x-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS6281x-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11.
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2.

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	9
Die FIT Rate	5
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile motor control
- Power dissipation: 500 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOSDigital, analog / mixed	25 FIT	55 °C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS6281x-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	35%
SW output not in specification – voltage or timing	45%
SW power HS or LS FET stuck on	10%
PG false trip or fails to trip	5%
Short circuit any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS6281x-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to GND (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TPS6281x-Q1 datasheet.

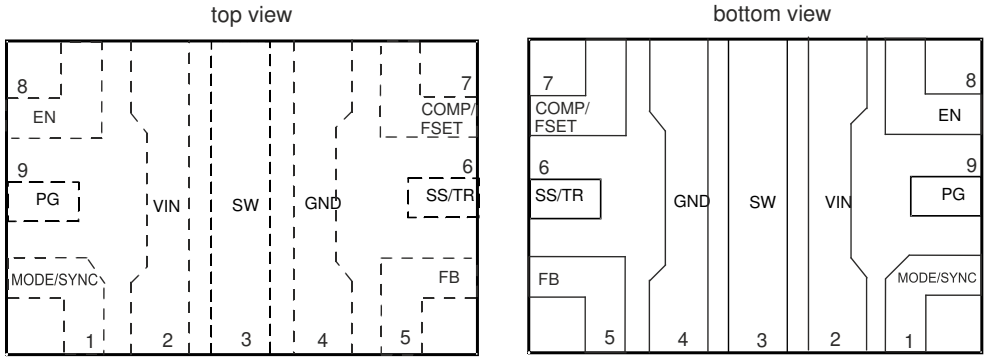

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption the device is running in the typical application, please refer to the '*Simplified Schematics*' on the 1st page in the TPS62810-Q1 datasheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to GND

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	Intended functionality.	D
VIN	2	Device does not power up.	B
SW	3	Potential device damage.	A
GND	4	No effect.	D
FB	5	Output voltage regulated to V_{IN} (100% mode).	B
SS/TR	6	Device not functional.	B
COMP/FSET	7	Intended functionality.	D
EN	8	Intended functionality.	D
PG	9	Intended functionality.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	Undetermined device operation.	B
VIN	2	Device does not power up.	B
SW	3	Device not functional, open loop operation.	B
GND	4	Device not functional.	B
FB	5	Undetermined output voltage behavior; open loop operation.	B
SS/TR	6	Intended functionality.	D
COMP/FSET	7	Intended functionality.	D
EN	8	Undetermined device operation; device might power up or not.	B
PG	9	Intended functionality.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	PG	Device runs FPWM mode once PG is high impedance.	B
FB	5	SS/TR	Undetermined device operation, V_{OUT} spikes up to V_{IN}	B
SS/TR	6	COMP/FSET	Undetermined device operation.	B
EN	8	PG	Device does not power up.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
MODE/SYNC	1	Intended functionality: Forced PWM.	D
VIN	2	Intended functionality.	D
SW	3	Potential device damage.	A
GND	4	Device does not power up.	B
FB	5	Potential device damage.	A
SS/TR	6	Intended functionality.	D
COMP/FSET	7	Intended functionality.	D
EN	8	Intended functionality.	D
PG	9	Potential device damage.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2020) to Revision C (December 2020) **Page**

- Fixed typo in Functional Safety Failure In Time (FIT) Rates section..... 3
- Changed "automotive control" to "motor control" in Functional Safety Failure In Time (FIT) Rates section.....3

Changes from Revision A (April 2020) to Revision B (September 2020) **Page**

- Added Table 2-2 3

Changes from Revision * (February 2020) to Revision A (April 2020) **Page**

- Added Pin Failure Mode Analysis.....5

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