Application Report

Extend Battery Life with < 100 nA IQ Buck Converter Achieving < 150 µV Voltage Ripple

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ABSTRACT

This document discusses different architectures for implementing buck converters for a battery-powered application, and the trade-offs for each. Architectures to be discussed include (A) buck converter + LDO, (B) forced pulse width modulation (FPWM) buck converter, and (C) buck converter + PI filter. Measurements have been taken to demonstrate the performance of each in output voltage noise, system efficiency for light and full loads, and input quiescent current. This document aids in determining which architecture is most suitable for an individual application, and helps clarify the differences in adaptive off-time and DCS-Control™ buck converter topologies.

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Trademarks

1 Introduction

Many battery-powered products such as wireless security cameras, video doorbells, and smart locks, are designed to have the option of running entirely off battery power, or with a battery and no other input power alternative. This allows users to install devices in any place of their choosing, regardless of the availability of a power socket nearby, and provide a more complete and discrete security coverage of their home.

Two challenges faced in the design of the system are reducing the amount of power lost in the power tree itself, and generating the power rails with minimal noise to meet peripheral input voltage noise requirements and improve performance. For example, a wireless security camera powered with two AA batteries requires less than 127 µA average system current (including both power-on and standby modes) to achieve two years of battery life. This can be calculated for any battery capacity and desired lifetime using Equation 1, which uses a 30% safety margin for the total battery capacity.

To achieve longer battery life, wireless or battery-powered cameras require a very low quiescent current (I_Q) and high efficiency at both full and light loads. These cameras typically employ motion detection, human interface, wireless communications monitoring, or any combination of the three to minimize time spent in power-hungry states. Because most of the device lifetime is spent in low-power states, quiescent currents, subsystem shutdown currents, and high efficiency are very important, as these standby currents can have significant impacts on overall battery life.

$$I_{avg} = \frac{0.7 \times \text{Battery Capacity}}{\text{Desired Lifetime}} \quad (1)$$

High voltage accuracy on the power rails is also a requirement, especially on rails that are powering core supply voltages, high speed I/O lines, and analog supplies. For HD video processing and streaming, the MPU is clocked at a very high speed, and employs a strict jitter budget. A noisy power supply to these high-speed lines induces jitter, thereby increasing bit error rate and degrading the quality of the high-speed signal. One example of this requirement is on the image sensor analog voltage, where it is necessary to ensure power supply noise is minimized to achieve a very high contrast ratio.

This document explores three different architectures for implementing high-efficiency, low-ripple buck converters for a battery-powered application, and the trade-offs for each. Possible solutions shown include: buck converter + LDO, forced pulse width modulation (FPWM) buck converter, and buck converter + PI filter. The performance of each is evaluated with respect to output voltage ripple, system efficiency at full and light loads, and I_Q.

2 Highlighted Products

Architecture A is implemented with the buck converter TLV62568 and the LDO TPS7A05.

TLV62568 is a high-efficiency, cost-effective buck converter utilizing an adaptive off-time with peak current control topology. The device operates at typically 1.5-MHz frequency PWM at moderate to heavy load currents. Based on the V_{IN}/V_{OUT} ratio, a simple circuit sets the required off time for the low-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current. The current of the high-side switch is sensed for peak current control, and implements a switch current limit to prevent the device from drawing excessive current from a battery, or input voltage rail. Once the high-side switch current limit is reached, the high-side switch is turned off, and the low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

TPS7A05 is an ultra-small, low quiescent current LDO that can source 200 mA with excellent transient performance. This device has an output range of 0.8 V to 3.3 V with a typical 1% accuracy. This LDO offers foldback current limit, shutdown, and thermal protection.

Architecture B is implemented with the FPWM version of the same buck converter from Architecture A, TLV62568A. As such, the control topology and functionality are essentially the same,but with the difference of TLV62568A staying in PWM mode at light loads while the TLV62568 goes into pulse frequency modulation (PFM) operation at light loads.

Architecture C is implemented with buck converter TPS62841, which has an ultra-low nominal I_Q of 60 nA, high light-load efficiency, and utilizes DCS-Control™. DCS–Control is a high-performance control scheme that combines the advantages of hysteretic and voltage mode controls. This combination allows for excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM modes with minimum output voltage ripple. It includes an AC loop that senses the output voltage and directly feeds this information into a fast comparator stage. An additional voltage feedback loop is used to achieve accurate DC load regulation, and an internally compensated regulation network achieves fast and stable operation with small, external components and low ESR capacitors. In PFM, or Power-Save Mode, the switching frequency varies linearly with the load current.

3 Buck Converter Architectures

Architecture A: Buck Converter + LDO

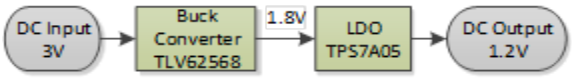


Figure 3-1. Architecture A Block Diagram

The first architecture to be discussed is a common solution, where a buck converter is followed by an LDO to reduce output voltage ripple in order to meet required output voltage accuracy.

The benefit of using this topology is that this solution keeps noise on sensitive rails low compared to a buck converter alone, due to the power supply rejection ratio (PSRR) of the LDO. When several LDOs are cascaded off a single buck converter to create multiple power rails, there is an added benefit.The magnitude of rejection, and the frequency of the output voltage ripple,are almost the same since there is only one switching converter sourcing the rails, rather than multiple switching converters sourcing the rails. With multiple switching converters, there is no correlation between output voltage frequency and magnitude, while the PSRR of an LDO is constant at a particular switching frequency and adds no switching elements.

One thing worth noting when designing with this topology is the noise-filtering capability of the LDO. An LDO with high PSRR can be chosen for noise-sensitive rails. However, this PSRR changes with respect to the switching frequency and output current. Figure 3-2 shows an example of this for the TPS7A05, the LDO used in Architecture A. In general, an LDO has better noise attenuation at lower switching frequencies, (such as when the converter is in PFM operation) and worse noise attenuation at higher switching frequencies (such as when the converter is operating at nominal switching frequency). This being said, the PSRR at high frequencies can be improved by increasing the output capacitor value.

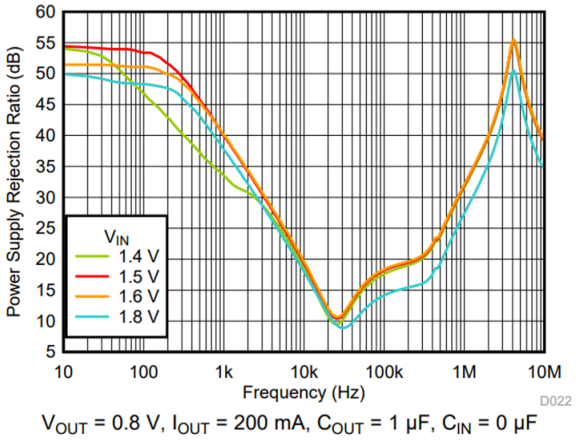


Figure 3-2. PSRR Curve of TPS7A05 at 200 mA Load Current and 0.8 V Output Voltage

One other thing to be aware of is the efficiency of the LDO, which can be calculated as shown in Equation 2. With higher voltage drop comes lower system efficiency, causing the power tree to draw more current from the battery at all load levels and ultimately decrease the battery life. As shown in Equation 3 and Equation 4, higher voltage drop also causes a higher temperature within the LDO IC itself, which is something to be especially aware of in designs that need to meet outdoor operating temperature requirements.

$$\text{LDO Efficiency} = \frac{I_O V_O}{(I_O + I_Q) V_I} \approx \frac{V_O}{V_I} \tag{2}$$

$$\text{IC Temperature} = T_A + R_{\theta JA} P_D \tag{3}$$

$$\text{LDO IC Temperature} = T_A + R_{\theta JA} I_O (V_I - V_O) \tag{4}$$

One other LDO to consider for use with this architecture is the TPS7A02, which has an ultra-low nominal I_Q of 25 nA, even in dropout. TPS7A02 is also optimized for excellent transient performance, and features a smart enable circuit with an internally controlled pulldown resistor to help minimize the external components used to pulldown the enable pin.

Architecture B: FPWM Buck Converter

Figure 3-3. Architecture B Block Diagram

The second architecture is a simple solution for applications concerned with noise. An efficient switching converter is forced to stay in PWM mode at light loads, rather than enter the power-saving PFM mode. In PFM mode, the converter only operates in short bursts when the output voltage falls below the nominal output voltage. This saves power by only turning on and switching when the minimum output voltage threshold is crossed, which reduces switching losses.

For buck converters that operate in both PFM and PWM modes, varying ripple voltage and frequency can be seen in dynamic load conditions as the buck converter changes operating mode from PFM to PWM, or vice versa. This behavior is not seen in the FPWM device, as it is forced to stay in PWM mode regardless of the load applied. As such, the benefit of a FPWM buck converter is that the switching frequency does not change, giving a fairly constant ripple for a fixed output capacitor, and improving the transient response across load variations. Additionally, the system efficiency at full load is much higher than the previous cascaded architecture, since no LDO is present.

The disadvantage of this architecture is a high I_Q and low light-load efficiency. Both of these disadvantages are direct results of the FPWM mode. Because the device remains in PWM mode regardless of the load conditions, the device continues to switch at high frequency and draw higher current even at no load, which causes a high I_Q. For the same reason, the light-load efficiency is extremely low since the current drawn by the buck converter is much higher than the output current at light loads.

Architecture C: Buck Converter + PI Filter

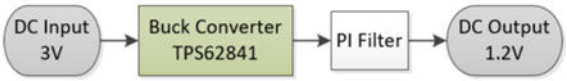


Figure 3-4. Architecture C Block Diagram

The third and final architecture to be discussed is a high-performance solution where a noise-sensitive rail is powered by an efficient switching converter to generate the desired voltage. As shown in Figure 3-4, it is followed by a ferrite bead PI filter to attenuate the switching noise. In this configuration, the buck converter can operate in the power-saving PFM mode, which allows for higher efficiency in light load conditions as previously discussed.

Implementing this architecture results in the lowest and most consistent output voltage ripple for full load conditions, which makes it the most ideal for peripherals with tight power supply noise requirements. Because these peripherals have the most stringent power supply regulation requirements when they are powered and actively processing data, full load noise levels are more important than light load noise levels, as light loads typically correspond to a peripheral in standby or shutdown mode.

In addition to low noise, this architecture provides high efficiency at all load levels. Similar to Architecture B, this topology is comprised of a single buck converter and no LDO, so the system efficiency is much higher than a power architecture using one or more LDOs. Unlike Architecture B, the noise requirement is handled externally by the buck converter with a PI filter, which allows the converter to operate in PFM mode and increases efficiency in light load conditions.

There are some considerations to take in the process of designing with this architecture. It is necessary to calculate the frequency and magnitude of the output voltage ripple of the buck converter for operating load conditions of the peripherals in order to design the PI filter, and there are further calculations in choosing the ferrite bead and passives around it. Implementing the PI filter is not quite as simple as implementing an

LDO, which requires choosing an adequate PSRR at the nominal switching frequency of the buck converter. Additionally, the PI filter has a more limited bandwidth for rejection, and has slight variations in settling time, which is a function of the filter values.

For this design, a ferrite bead is used and the following values chosen for the PI filter:

- C_{IN} = 0.1 µF
- C_{OUT} = 10 µF
- R_{DAMP} = 0.33 Ω
- C_{DAMP} = 47 µF

The PI filter design is done using equations and criteria from TIDA-01579.Figure 3-5 shows the filter circuit and the equivalent circuit of the ferrite bead.

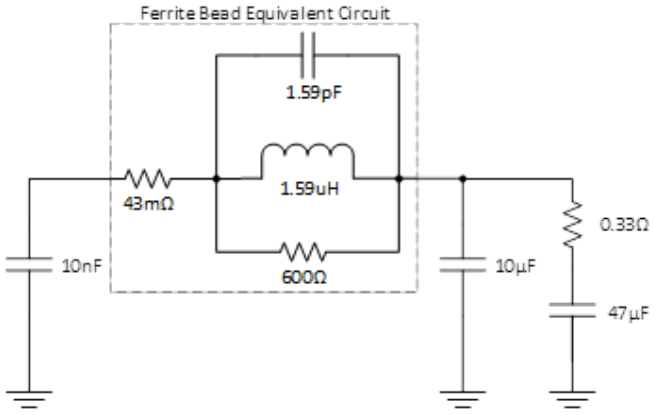


Figure 3-5. PI Filter Circuit Diagram

4 Testing Setup

In order to compare the three architectures, the tests conducted on each are as follows:

- System efficiency at both light load (10 µA) and full load (200 mA).
- System input current at light load (10 µA) and full load (200 mA), and no load (IC enabled)
- Ripple voltage and ripple frequency at both light load (10 µA) and full load (200 mA)
- Ripple voltage transient response with dynamically switching load between 50 µA and 200 mA at 1 kHz
- Thermal imaging test

The setup for testing, shown in Figure 4-1, consists of:

- The test board
- Agilent DC Supply E3633A
- Keithley Sourcemeter 2450
- Tektronix Mixed Domain Oscilloscope MDO3024, with a bandwidth of 200 MHz and sampling rate of 2 GSa/s
- Keysight 6-1/2 DMM 34461A
- Kikusui Electronic Load PLZ164WA

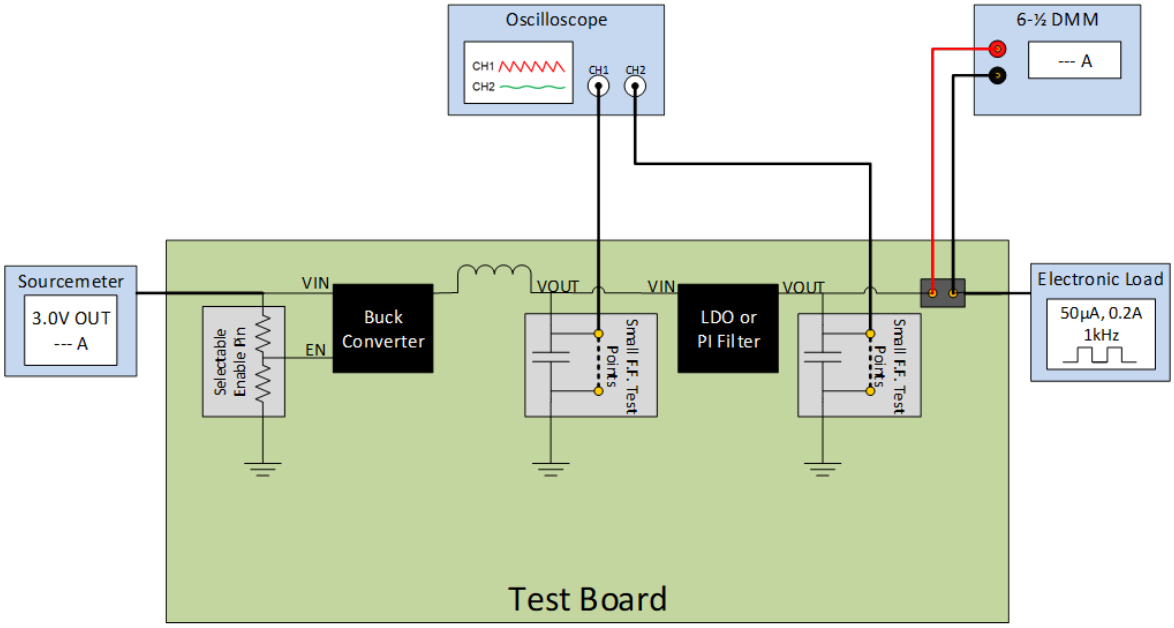


Figure 4-1. Test Setup Diagram

In order to test and demonstrate these architectures, a test board with all three architectures was designed and fabricated. The board is shown in Figure 4-2, including the dimensions of each architecture on the board for form factor comparison. Note that all components on the board shown are on the top side of the board for direct comparison – the board area can be reduced by placement of components on both sides of the board.

Some ripple measurements taken were at or beneath the noise floor of the oscilloscope used, which was observed to be -86 dB (or 142 µVpp). These results are denoted as "Noise Floor" in the results table.

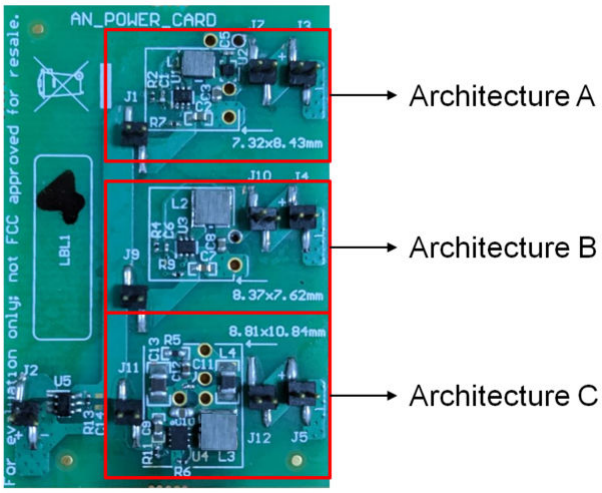
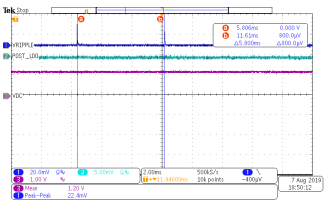
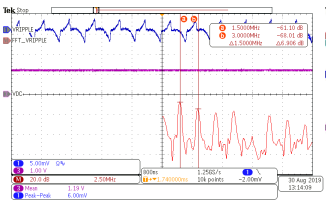
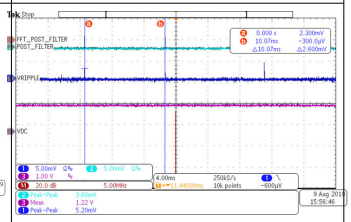
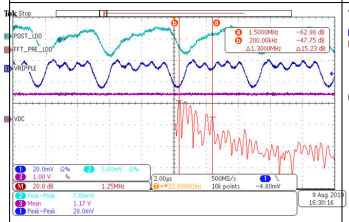
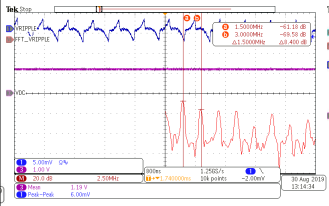
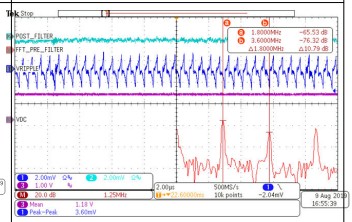
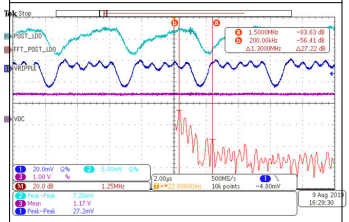
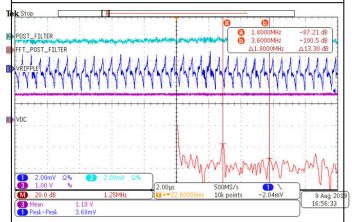
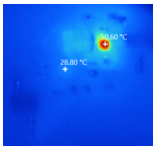
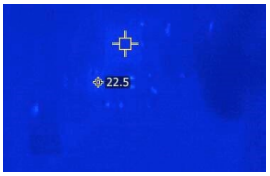
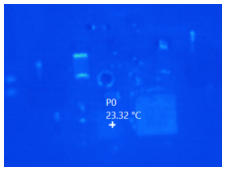
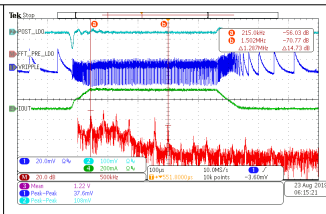
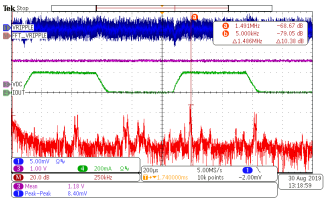
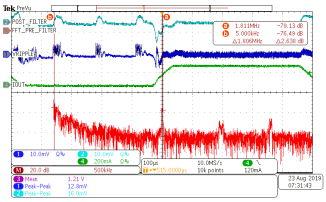
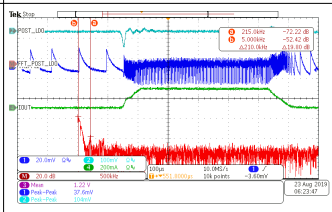
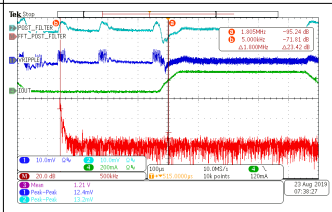


Figure 4-2. Test Board Image

5 Testing Results

PARAMETER	ARCHITECTURE A	ARCHITECTURE B	ARCHITECTURE C
I_Q (Load = 0 A, Device Enabled)	34 µA	2.7 mA	75 nA
Light Load (I_{LOAD} = 10 µA)			
System Efficiency	10%	0.1%	93%
Stage 1 Ripple	22.4 mV 1.87% Accuracy  Architecture A at 10 µA load. Both pre- and post-LDO ripples shown in dark blue and light blue, respectively. LDO rejects > 50 dB at 20 Hz PFM frequency	6.0 mV 0.50% Accuracy  Architecture B at 10 µA load. Ripple (dark blue) and FFT plot of ripple (red) showing expected PWM ripple at 1.5 MHz	5.20 mV 0.43% Accuracy  Architecture C at 10 µA load. Both pre-and post-PI filter ripples shown in dark blue and light blue, respectively. PI filter rejects only 3 dB at 100 Hz PFM frequency
Stage 2 Ripple	Noise Floor <0.01% Accuracy	N/A	3.60mV 0.30% Accuracy
Full Load (I_{LOAD} = 200 mA)			
System Efficiency	61%	91%	88%
Stage 1 Ripple	28.0 mV 2.33% Accuracy  FFT plot for ripple before LDO with 6.5 MHz bandwidth; cursors at low frequency 200 kHz peak and nominal switching frequency 1.5 MHz peak	6.0 mV 0.50% Accuracy  FFT plot shown for FPWM ripple with 6.25 MHz bandwidth; cursors at nominal switching frequency 1.5 MHz and first harmonic 3 MHz peaks	3.68 mV 0.31% Accuracy  FFT plot for ripple before PI filter with 6.25 MHz bandwidth; cursors at nominal switching frequency 1.8 MHz and first harmonic 3.6 MHz peaks
Stage 2 Ripple	7.6 mV 0.63% Accuracy  FFT plot for ripple after LDO with 6.5 MHz bandwidth; cursors in same spots showing expected 22 dB rejection by TPS7A05 at 1.5 MHz	N/A	Noise Floor <0.01% Accuracy  FFT plot for ripple after PI filter with 6.25 MHz bandwidth; cursors in same spots showing ripple after PI filter reaches noise floor of oscilloscope (85–90 dB)

PARAMETER	ARCHITECTURE A	ARCHITECTURE B	ARCHITECTURE C
Thermal Images Taken after 20 minutes on with 200 mA load current	 Infrared image showing TLV62568 heating to 28.8°C and TPS7A05 heating to 50.6°C after 20 minutes	 Infrared image showing TLV62568A heating to 22.5°C after 20 minutes	 Infrared image showing TPS62841 heating to 23.3°C after 20 minutes
Transient - Switching Load (Square wave, 50uA-200mA, 1kHz)			
Stage 1 Ripple	 Dynamically changing operation mode (PFM-PWM-PFM) with load change. FFT plot before LDO with 4 MHz bandwidth, showing several frequency spikes as PFM frequency changes to PWM	 Output ripple continues to be PWM as load changes, with minimal overshoot and undershoot at load step. FFT plot with 2.5 MHz bandwidth shows ripple at 1.5 MHz, as expected	 Dynamically changing operation mode (PFM-PWM) with load change. FFT plot before PI filter with 4.25 MHz bandwidth, showing ripple primarily at very low frequencies (PFM) and switching frequency (1.8 MHz)
Stage 2 Ripple	 FFT plot after LDO with 4 MHz bandwidth shows higher overshoot and undershoot values (low frequency) and strong noise attenuation by LDO	N/A	 FFT plot after PI filter with 4.25 MHz bandwidth, showing undershoot and overshoot present, though smaller than values in Architecture A, and very strong noise attenuation by PI filter
Overshoot (at output of architecture)	24 mV	3 mV	6 mV
Overshoot Settling Time	125 µs	60 µs	166 µs
Undershoot (at output of architecture)	76 mV	3 mV	8 mV
Undershoot Settling Time	129 µs	29 µs	96 µs

6 Results Summary

The results and observations for each architecture are summarized below. Pros and cons are listed, with regards to battery-powered devices targeting low I_Q, high efficiency at all load levels, and high output voltage accuracy.

Architecture	Pros	Cons
A: Buck Converter + LDO	• Noise reduction at select, typically lower, frequencies (high speed peripherals OFF) • Cascaded LDOs with single switching converter give similar ripple rejection	• Low light and full load efficiency • Limited ripple rejection across a higher frequency bandwidth, requiring a larger output capacitor • Thermal performance
B: FPWM Buck Converter	• Fixed output ripple voltage across load variations • Better transient response for large load changes • High full load efficiency • Simple solution	• Extremely low light load efficiency • I_Q (FPWM devices typically in mA range of I_Q)
C: Buck Converter + PI Filter	• Very high light & full load efficiency • Strong noise attenuation at higher switching frequencies (high speed peripherals ON)	• Dependency of PI filter on load conditions/range • Limited low frequency rejection for PFM voltage ripple

7 Further Reading

See *TIDA-01579* for more information on the choice of passives, PI filter design, and layout considerations for wireless camera power trees.

Relevant end equipment pages to look through, with reference diagrams, reference designs, and more applicable at a system level:

- Wireless Security Camera
- Video Doorbell
- Electronic Point of Sale
- Motion Detector

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2019) to Revision A (May 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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