Application Report
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Understanding Flip Chip QFN (HotRod™) and Standard QFN Performance Differences

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ABSTRACT

DC/DC converters are evaluated on key performance metrics like thermal performance, efficiency, size, and noise. The package technology used can influence the performance in these metrics. Many recently released DC/DC converters use Flip Chip Quad Flat No-lead (QFN) or HotRod™ (HR) QFN package technology to maximize their performance. However, HR QFN package technology typically lacks the large thermal pad present on the bottom of standard QFN packages. A common question for end equipment where thermal performance is a key concern due to high ambient temperatures is whether the HR QFN package can meet the thermal requirements. Examples include Active Antenna Systems (AAS), Macro Remote Radio Units (RRU), and data center switches. This application report compares the performance of the HR QFN and standard QFN packages using measurements taken with the TPS54824 and TPS54A24.

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Trademarks

1 Introduction

Standard QFN packages use bond-wires to connect the silicon die to the leadframe. Bond-wires add parasitic resistance and inductance between the die and the leadframe. Many DC/DC converters are now being designed using the HR QFN package technology, which eliminates bond-wires and minimizes the parasitic resistance and inductance. This is done by flipping the die and soldering it directly to the leadframe. Externally, the package looks similar to the standard bond-wire QFN. This type of packaging is ideal for DC/DC converters because low resistance and inductance help achieve the best performance. Low resistance improves efficiency, and low inductance reduces overshoot and ringing when the power MOSFETs switch. This application report focuses on the measured performance differences between the TPS54824 and TPS54A24. Refer to Effects of IC Package on EMI Performance and How a DC/DC Converter Package and Pinout Design Can Enhance Automotive EMI Performance for more details on the differences between the HR and standard QFN packages. Table 1 summarizes the differences between the two package technologies.

Table 1. Summary of Differences Between the Two Package Technologies

CHARACTERISTIC	HotRod QFN	STANDARD QFN
Package size	Reduced size because less clearance is needed for package interconnects	Larger size because of spacing required for bond-wires to connect between the die and pin
Package parasitic from pin to die	Lower parasitic inductance and resistance because the die is soldered directly to the leadframe	Bond-wires add parasitic inductance and resistance
Power loss	Reduced conduction power loss because of lower parasitic resistance. Lower parasitic inductance can also allow faster switching speeds to reduce switching loss.	Higher power loss because of added parasitic resistance
Thermal pad	No thermal pad, but low impedance connection between the die and the package provides a path for heat to flow out through each pin of the IC	Yes
Thermal performance	Lower power loss can make up for higher thermal impedance, resulting in similar thermal performance	Thermal pad can help make up for additional power loss
Noise	Expect lower noise due to lower parasitic inductance in the package interconnects	Slightly higher noise because of higher parasitic inductance

The TPS54824 and TPS54A24 are synchronous buck converters typically used with a nominal input voltage or 5 V or 12 V. The TPS54824 is in a HR QFN package and supports up to 8 A load current. The TPS54A24 is in a standard QFN package and supports up to a 10 A load current. The same die is used in both parts. The only differences are the package technology and the current limit.

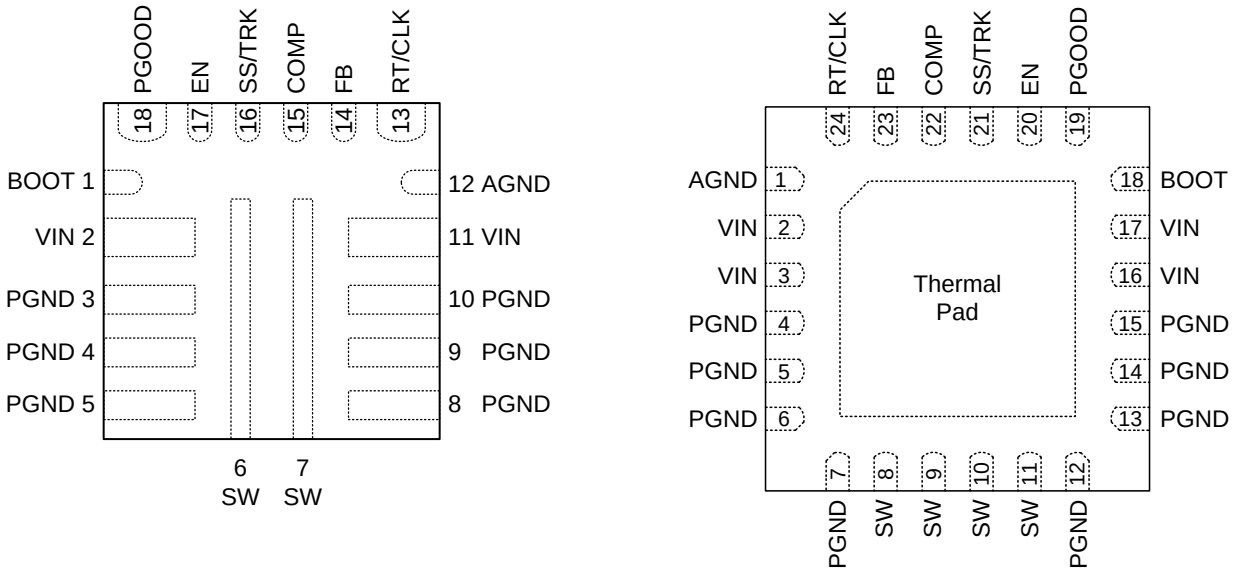

Figure 1. Topside View of the TPS54824 and TPS54A24 Pinouts

Figure 1 shows the pinout of both packages drawn approximately to scale. The pinouts are mirror images of each other across the y-axis because the die is flipped between the two package technologies. The HR QFN package has the active side of die facing down, and the standard QFN package has the active side of die facing up.

2 Device Datasheet Specification Comparison

Table 2. Summary of Specification Differences in Datasheets Related to the Package

SPECIFICATION	TPS54824 (HR QFN)	TPS54A24 (STANDARD QFN)
Package size	**3.5-mm x 3.5-mm**	4.0 mm-x 4.0-mm
Thermal pad	No	**Yes**
JEDEC Standard θ_{JA}	57.1°C/W	**37.5°C/W**
High-side MOSFET (HS FET) $R_{DS(on)}$	**14.1 mΩ**	21 mΩ
Low-side MOSFET (LS FET) $R_{DS(on)}$	**6.1 mΩ**	8 mΩ

Table 2 summarizes the key specification differences that result from the different package technologies. These differences can be found in the datasheet. The HR QFN package is smaller because it requires less clearance between the die and the edge of the package, making it much closer to the size of the die. However, the HR QFN package lacks a thermal pad to aid in heat dissipation. Instead, the low impedance connections between the die and the HR QFN package pins provide a path for heat to conduct out of every IC pin.

The standard QFN has lower junction-to-ambient thermal resistance (θ_{JA}) than the HR QFN when using the JEDEC standard PCB. However, this can be misleading, as the JEDEC standard rules give the standard QFN package with thermal pad an advantage: The standard QFN package is simulated with an array thermal vias in the thermal pad. The HR QFN package does not have a pad for thermal vias, so the simulation is done with no thermal vias. In a real PCB layout, thermal vias can be placed near the HR QFN package to improve heat dissipation. See the Optimizing the Layout for the TPS54424/TPS54824 HotRod QFN Package for Thermal Performance Application Note for more details on how to optimize the TPS54824 HR QFN layout for thermal performance.

Additionally, the JEDEC standard calls for each pin to be connected to a 0.25 mm-wide trace routed 25 mm towards the perimeter. This reduces the effectiveness of conducting heat out of every pin of the IC. In a real PCB, the power pins are typically tied together with large copper pours. Figure 2 shows the footprint used for the TPS54824 JEDEC standard θ_{JA} simulation. The measured thermal performance with similar EVM PCB layouts in the next section gives a better comparison.

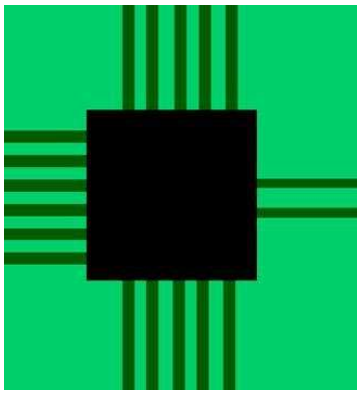

Figure 2. TPS54824 (HR QFN) JEDEC Standard PCB Footprint for Thermal Parameters (Dark Green = Traces)

Lastly, the bond-wires in the standard QFN package, as mentioned earlier, add resistance in series with the power MOSFETs. This increases the effective $R_{DS(on)}$ of the MOSFETs, which increases the conduction power loss in the IC and lowers the efficiency. A copper bond-wire with a length of 1 mm and a 50.8 µm diameter has an estimated resistance of 8.6 mΩ. Assuming two bond-wires per pin gives bond-wires for VIN, 16 for PGND, and eight for SW. Putting these bond-wires in parallel results in an estimated additional resistance of 1.1 mΩ to the VIN pin, 1.1 mΩ to the SW pin, and 0.5 mΩ to the PGND pin. The estimated increase to the effective HS FET is $R_{DS(on)}$ 2.2 mΩ, and the LS FET resistance is 1.6 mΩ. The TPS54A24 has an additional 4 mΩ resistance added to the HS FET, due to the silicon die layout being optimized for the HR QFN package. Re-optimizing the silicon die layout for the standard QFN package can reduce this added resistance.

3 Device Measured Performance Comparison

The part performance was measured using the standard EVM available on ti.com. Figure 3 and Figure 4 show the top-side layout for the two EVMs. The TPS54A24EVM-058 and TPS54824EVM-779 were modified to match. The following are the two important changes made to each EVM to match them.

1. TPS54A24EVM-058: L1 changed to CMLE063T-1R0MS
2. TPS54824EVM-779: R7 changed to 100 kΩ for 500 kHz fsw

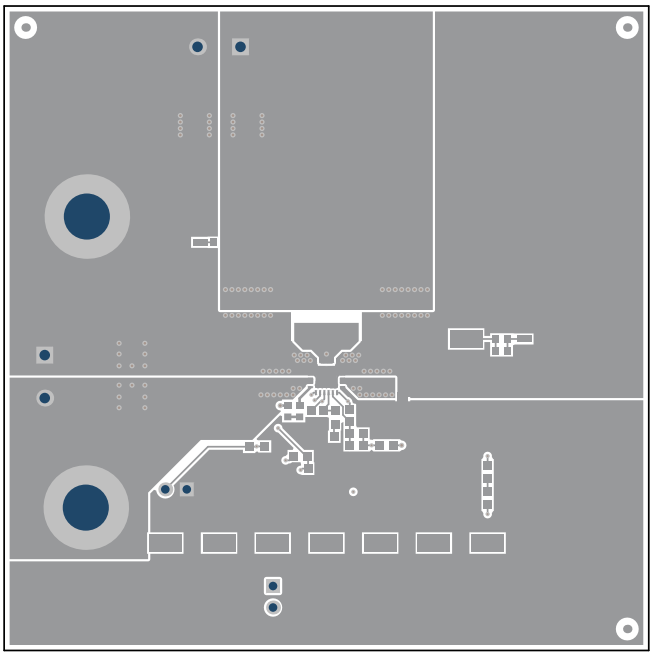

Figure 3. TPS54A24EVM-058 Top-Side Layout (Standard QFN)

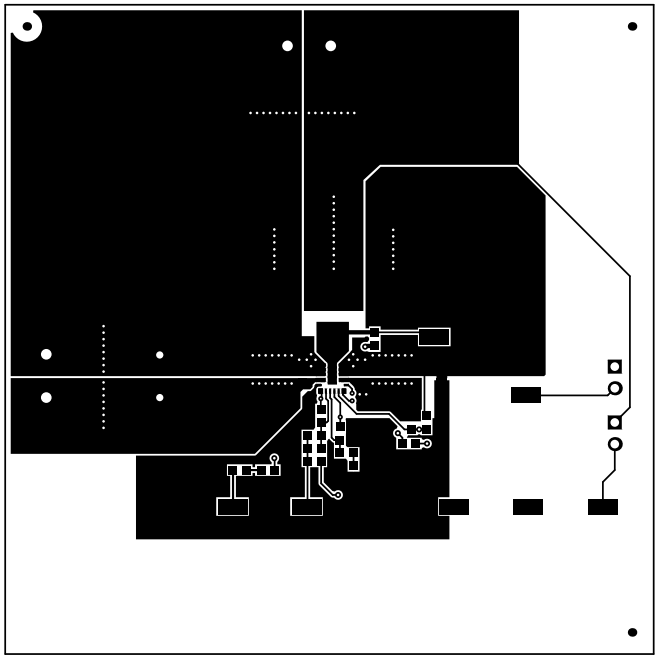

Figure 4. TPS54824EVM-779 Top-Side Layout (HR QFN)

Figure 5 and Figure 6 compare the power loss of the two EVMs. The power loss number includes loss in the inductors. At both of the input voltages tested, the HR QFN had lower power loss than the standard QFN. The difference is more significant at 5 V input, where the switching losses are lower and the part operates at a higher duty cycle. With the higher duty cycle, the conduction loss in the HS FET is higher. This gives the HR QFN package, and its lower conduction losses, a larger advantage.

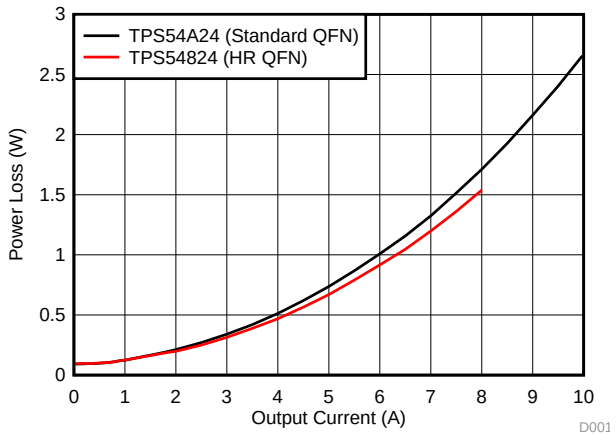

Figure 5. Power Loss Comparison, V_{IN} = 5 V

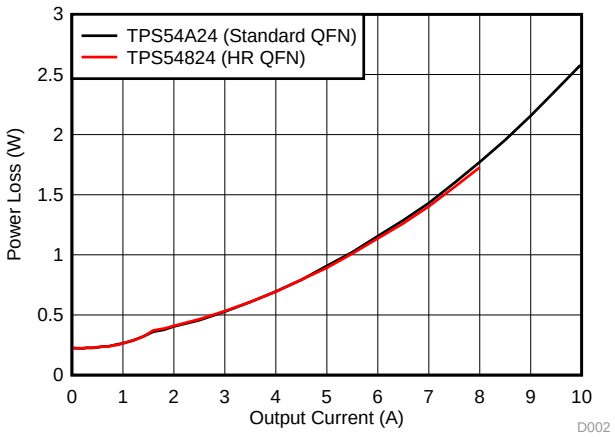

Figure 6. Power Loss Comparison, V_{IN} = 12 V

Figure 7 and Figure 8 compare the thermal performance of the two EVMs. There was at least a 10-minute soak time before each measurement to ensure thermal equilibrium was reached. In this comparison, the package with the best thermal performance depends on the input voltage. With a 5-V input, the HR QFN operated at a lower temperature because it had much lower power loss. With 12-V input, the better thermal performance of the standard QFN package outweighed the reduced conduction power loss in the HR QFN package.

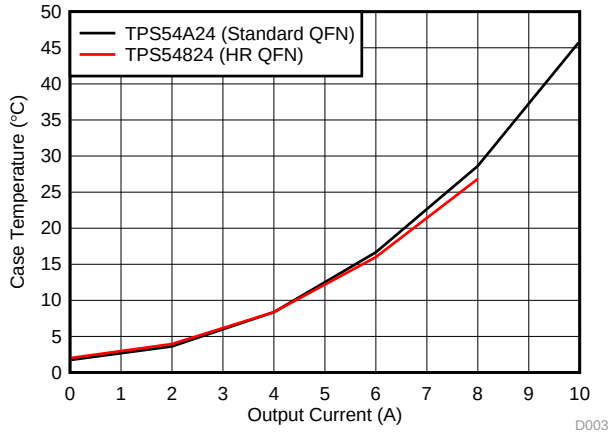

Figure 7. Case Temperature Rise Comparison, V_{IN} = 5 V

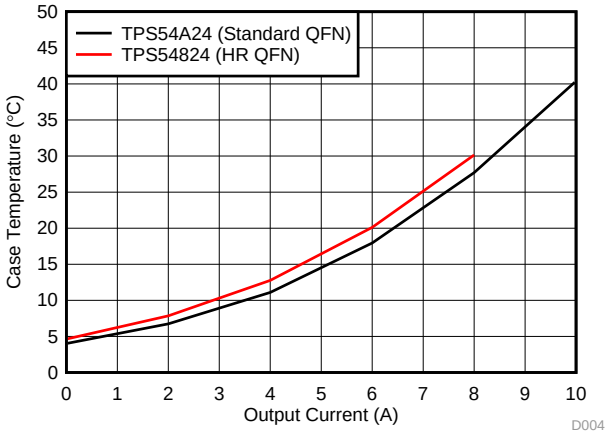

Figure 8. Case Temperature Rise Comparison, V_{IN} = 12 V

Figure 9 and Figure 10 compare the SW node ringing with V_{IN} = 12 V and I_{OUT} = 8 A. This measurement was taken with a 1-GHz oscilloscope and a 1-GHz differential probe touching the pins of the IC. The measured peak overshoot is the same on both parts at 15.6 V. However, the bond-wires of a standard QFN have more inductance, so the stress on the die is higher. The HR QFN has lower inductance, so the measured voltage is much closer to the stress on the die.

The parasitic loop inductance for each package can be estimated from the SW overshoot ringing frequency. This is the same method used to select values for an RC snubber given in Calculate an RC Snubber in Seven Steps. First, the parasitic capacitance is estimated by adding a capacitor between the SW and PGND pins, then measuring the change in the SW overshoot ringing frequency. With the estimated parasitic capacitance, the parasitic inductance is calculated from the original SW overshoot ringing frequency. The HR QFN package has an estimated 1 nH loop inductance, and the standard QFN package has an estimated 1.4 nH loop inductance. The lower loop inductance of the HR QFN package can help reduce radiated noise and lower voltage stress on the die.

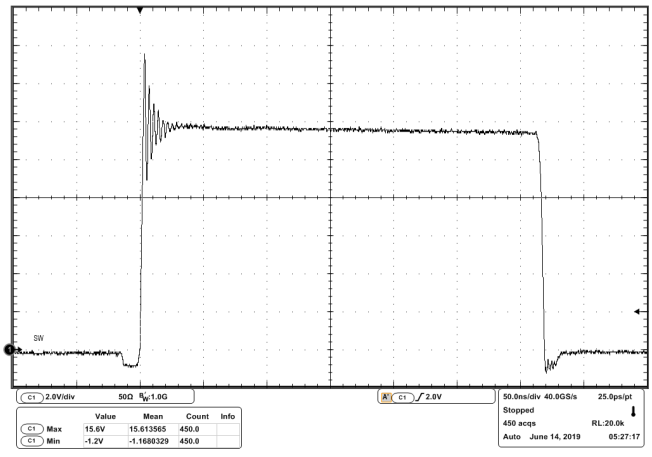

Figure 9. TPS54824 (HR QFN) SW Pin Measurement

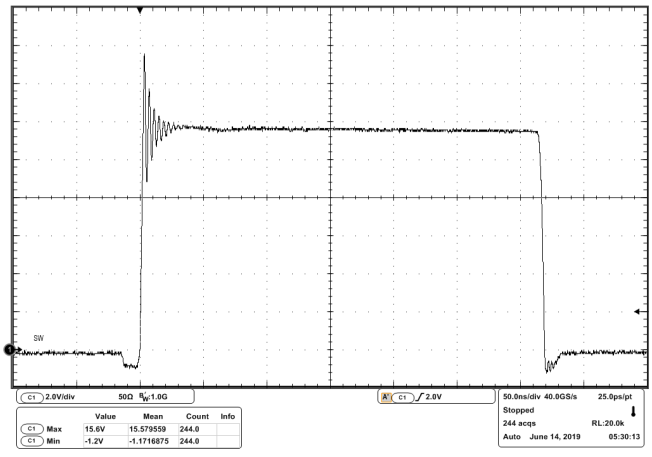

Figure 10. TPS54A24 (Standard QFN) SW Pin Measurement

Table 3 summarizes the differences in performance. All measurements in this table are for 1.8 V output, 8 A load, and 500 kHz f_{SW} unless otherwise noted.

Table 3. Summary of Measured Performance Differences

MEASUREMENT	TPS54824 (HR QFN)	TPS54A24 (STANDARD QFN)
Total power loss (includes inductor power loss) (V_{IN} = 12 V)	**1.82 W**	1.86 W
Total power loss (includes inductor power loss) (V_{IN} = 5 V)	**1.61 W**	1.80 W
Case temperature rise (V_{IN} = 12 V)	30.1°C	**27.7°C**
Case temperature rise (V_{IN} = 5 V)	**26.8°C**	28.6°C
SW node Max Voltage (V_{IN} = 12 V)	15.6 V	15.6 V
Estimated switching loop inductance	**1 nH**	1.4 nH

4 Summary

This comparison validates that the TPS54824 HR QFN package has smaller size, higher efficiency, and lower switching loop inductance. The HR QFN achieves higher efficiency by minimizing parasitic resistance. The lower loop inductance of the HR QFN can reduce radiated noise and reduce switching loss by enabling faster switching speeds. When comparing these parts, the package with the best thermal performance depends on the input voltage. With 5-V input, minimizing the conduction loss is more important than minimizing the switching loss, so the HR QFN operates at a lower temperature. With 12-V input, the switching losses become a larger portion of the total loss, so the TPS54A24 standard QFN operates at a lower temperature. The best package technology for best thermal performance also depends on the PCB design rules used in the application. Depending on these rules, the standard QFN package thermal pad can make it easier to design a layout for the best thermal performance. Finally, most HR QFN packages have unique designs, so the performance compared to a standard QFN can vary.

5 References

- Texas Instruments, TPS54824 4.5-V to 17-V (19-V Maximum) Input, 8-A Synchronous SWIFT™ Step-Down Converter Datasheet (SLVSDC9)
- Texas Instruments, TPS54A24 4.5-V to 17-V Input, 10-A Synchronous SWIFT™ Step-Down Converter Datasheet (SLVSEQ0)
- Texas Instruments, TPS54824EVM-779 8-A, SWIFT™ Regulator Evaluation Module User's Guide (SLVUAX8)
- Texas Instruments, TPS54A24EVM-058 10-A, SWIFT™ Regulator Evaluation Module User's Guide (SLVUBM5)

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