Application Note

Open Load Detection in Motor Drivers

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ABSTRACT

Protection and diagnostics are the highest priorities of any system board. The demand of diagnostic features to make the system robust and reliable is increasing day by day. Open load detection (OLD) is a protection diagnostic which determines a load's (motors, solenoids, relays, LEDs, and resistors) connectivity to the power-stage of an motor integrated or gate driver. This article presents various types of OLD diagnostics, features and implementation in TI's motor drivers.

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1 Introduction

The OLD diagnostic detects if the output terminals (OUT1 and OUT2) are disconnected from the loads to cater to a safer and more robust system. OLD can be done in different diagnostics. Below is a list describing each OLD diagnostic and in which motor drivers the OLD diagnostics are implemented:

- **Passive Open Load Detection:** The passive OLD, which is also called offline open load diagnostic, is carried out before the FETs are in operation. All of the FETs are in Hi-Z state, while a minimal amount of diagnostic current flows through the load for a short amount of time to test the load's connection to the FETs. The diagnostic current must be very small to avoid load rotation. For the diagnostic current to flow, a command is sent by the user to the motor driver to activate the passive OLD and initiate the diagnostic current flow from four OLD current sources and through either four OLD resistors or internal blocking diodes. For each FET in each half-bridge, there is one OLD current source and resistor or internal blocking diode. The passive OLD circuit implementation found in the brushed DC motor integrated drivers is similar to the implementation found in the stepper motor integrated drivers. In these two types of drivers, the drivers provide the necessary hardware to conduct passive OLD diagnostics. In low-side integrated drivers, only the low-side OLD current sources, one for each output, are required to sense if an OLD event has occurred. Note that there are no OLD resistors or internal blocking diodes. The passive OLD integrated drivers and in Brushless DC (BLDC) motor gate drivers operates similarly as both types of drivers use the OLD resistors instead of the internal blocking diodes found in BDC motor gate drivers. Passive OLD in BLDC gate drivers is dependent on the capacitance between the load phase pins to ground. Additionally, not all load connections are supported in BLDC gate driver passive OLD. The details of passive OLD integrated drivers are presented in Section 2. Passive OLD can be found in the following types of drivers:
  - **Integrated Drivers**
    - **Stepper Motor Drivers**
    - **Brushed DC Motor Drivers**
    - **Low-Side Drivers**
  - **Gate Drivers**
    - **Brushed DC Motor Drivers**
    - **Brushless DC**
- **Active Open Load Detection:** The active OLD, which is also called online OLD, is carried out while the FETs driving the load are turned ON. Active OLD ensures that the load is connected to the driver during the operation. While the load is in operation, the current flowing through the FETs is monitored to ensure that the load is connected. Active OLD can be found in Integrated Drivers such as Stepper and BDC Drivers, as well as in Gate Drivers such as BLDC motor gate drivers.In stepper motor integrated drivers, if the winding current in any coil drops below the open load current threshold (IOLD) and the current regulation (ITRIP) level set by the indexer, an OLD event is detected. In some BDC motor drivers, if the current flowing through the load drops below the IOLD during continuous and PWM operation, an OLD event is detected. In other BDC motor drivers, such as DRV8873, DRV8873-Q1 and the DRV842x-Q1 devices, the active OLD diagnostic monitors the body diode voltage of current re-circulation only through high-side FETs (asynchronous rectification) to detect an OLD event. In BLDC gate drivers, the current re-circulation flowing into the body diode of the high-side or low-side FET is monitored to check the status of the load's connection to the driver. Active OLD is presented in Section 3. Active OLD can be found in the following types of drivers:
  - **Integrated Drivers**
    - **Stepper Motor Drivers**
    - **Brushed DC Motor Drivers**
  - **Gate Drivers**
    - **Brushless DC Motor Drivers**

- **Low-Current Active Open Load Detection:** In low-current active OLD, the current OLD threshold is around 10x less than the active OLD diagnostic. This smaller current threshold gives a flexibility to user to detect a smaller motor nominal current. The details on the low-current active OLD are presented in Section 4. Low-current active OLD can be found in the following types of drivers:
  - **Integrated Gate Drivers**
    - **Brushed DC Motor Drivers**
- **Negative-Current Active Open Load Detection:** In negative-current active OLD, the current OLD threshold is negative. This unique active OLD diagnostic utilizes the current re-circulating through the body diode of the re-circulation FET (synchronous rectification) to detect an OLD event. In this diagnostic, the current re-circulation flowing into the FET is monitored to check the status of the load's connection to the driver. Since it accounts for the negative-current across this FET, it prevents the false OLD flag seen in active OLD since active OLD does not account for negative current flow. The details about this OLD diagnostic are presented in Section 5. Negative-current active OLD can be found in the following types of drivers:
  - **Integrated Gate Drivers**
    - **Brushed DC Motor Drivers**

The OLD diagnostics are dependent on the type of load connection to the output terminal(s). The load connections can be classified into three configurations:

1.1 Load Connected to Supply

In this configuration, the unidirectional motor or solenoid / relay load is connected between an output (for example OUT1) and the supply (for example VM) as shown in Figure 1-1 (Passive OLD) and Figure 1-2 (Active OLD). This configuration is used for unidirectional control of loads. During the passive OLD, there is no current flow to the load. During the active OLD, the load's current flows from VM to OUT1 to GND when the low-side FET is turned ON.

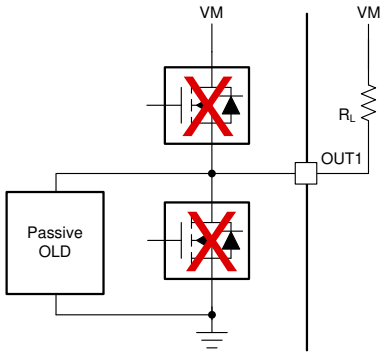

Figure 1-1. Passive OLD for Load Connected to VM

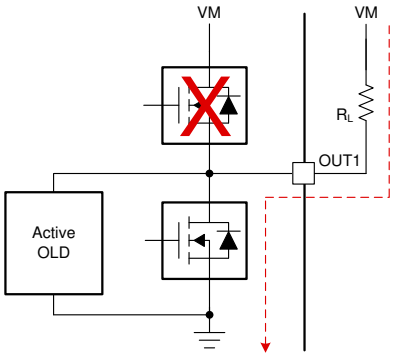

Figure 1-2. Active OLD for Load Connected to VM

1.2 Load Connected to Ground (GND)

In this configuration, the unidirectional motor or solenoid / relay load is connected between an output (for example OUT1) and the GND as shown in Figure 1-3 (Passive OLD) and Figure 1-4 (Active OLD). This configuration is used for unidirectional control of loads. During the passive OLD, there is no current flow to the load. During the active OLD, the load's current flows from OUT1 to GND when the high-side FET is turned ON.

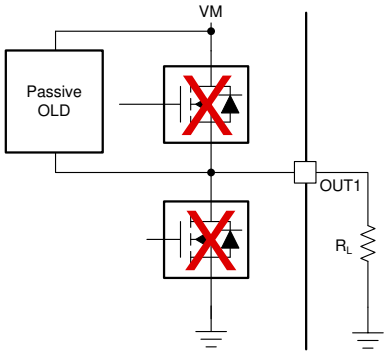

Figure 1-3. Passive OLD for Load Connected to GND

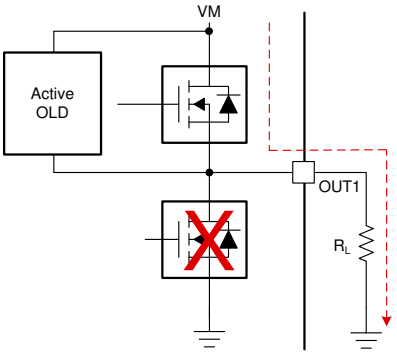

Figure 1-4. Active OLD for Load Connected to GND

1.3 Load Connected to H-Bridge

In this configuration, the bidirectional motor or solenoid / relay load is connected between two outputs (for example OUT1 and OUT2) as shown in Figure 1-5 (Passive OLD) and Figure 1-6 (Active OLD). This configuration is widely used for bidirectional control of loads. This configuration gives flexibility to change the direction of the load by opposing the voltage polarity at OUT1 and OUT2. During the passive OLD, there is no current flow to the load. During active OLD, the load's current flows VM to either OUT1 or OUT2, then to the other output and finally to GND when a half-bridge's high-side FET and the other driven half-bridge's low-side FET are turned ON. To drive in the opposite polarity, those FETs are turned OFF and the FETs that were OFF are now turned ON.

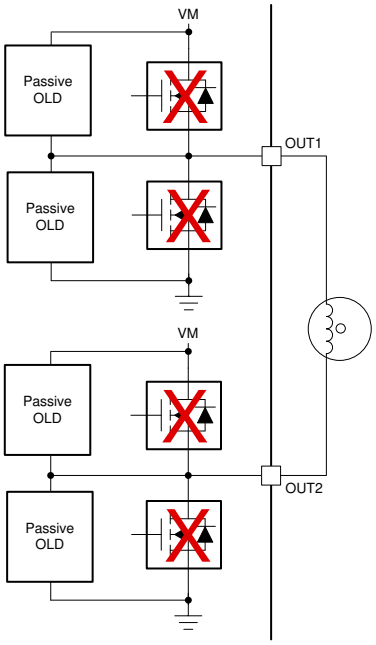

Figure 1-5. Passive OLD for Load Connected in H-Bridge Configuration

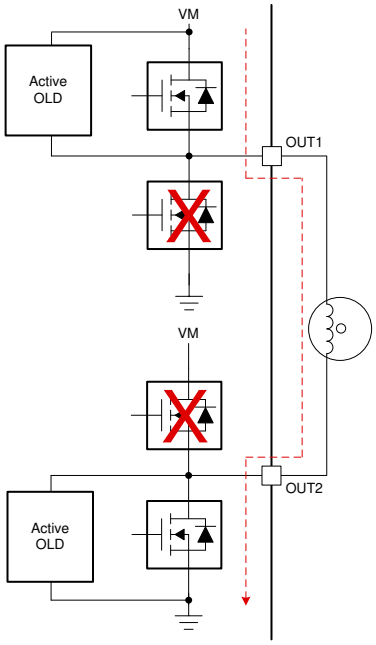

Figure 1-6. Active OLD for Load Connected in H-Bridge Configuration

2 Passive Open Load Detection

The passive OLD is also referred to as the offline OLD, where the OLD is carried out before the FETs are turned ON. This diagnostics feature ensures that the load is connected to the driver before driving the load. Passive OLD cannot be utilized at the same time as other OLD diagnostics. Load connections to supply, to GND, and in an H-bridge can be detected with passive OLD integrated drivers.

Figure 2-1 shows the circuit implementation of the passive OLD in BDC and stepper motor integrated drivers. For gate drivers, the circuit implementation is similar, with the difference being the FETs are not integrated. The FETs must be in Hi-Z state. Internal source / sink current sources drive current into the load connected between, for example, OUT1/SH1/DL1 and OUT2/SH2/DL2 during a set deglitch time and are limited by the load's resistance. The diagnostic current is very low (~100 µA for DRV8847) such that it doesn't rotate the load. If the load is connected between OUT1/SH1/DL1 and OUT2/SH2/DL2, a low-impedance path is created, causing the diagnostics current to be high and operate in saturation. However, if the load is disconnected from the either of OUT1/SH1/DL1 and OUT2/SH2/DL2, a high-impedance path is created, causing the current to be reduced to zero. The voltage at the comparators inputs that share the same node as the current sources fluctuates with the current variation. When the comparator positive terminals are greater than the negative reference voltage terminals, the comparator outputs are high. These comparator outputs are the OLD flags. Passive OLD is not enabled if any other fault other than OCP/OLD are present.

For BDC gate drivers, the motor driver provides the necessary hardware to conduct passive OLD diagnostics of the external FETs and the load. The differences between this passive OLD diagnostic and the passive OLD diagnostic found in integrated and BLDC gate drivers are: BDC gate driver passive OLD recommends the VDS comparator thresholds should be adjusted to 1-V or greater to ensure enough headroom for the internal blocking diode forward voltage drop and the internal OLD pull-up and pull-down circuits replace the OLD resistors with internal blocking diodes, as shown in Figure 2-2.

Figure 2-3 shows the circuit implementation of the passive OLD in BLDC gate drivers. The load phase pin to ground capacitances must discharge before passive OLD is enabled. Single phase high-side and low-side loads are not supported in BLDC gate drivers, as shown in Figure 2-4.

In integrated low-side drivers, only low-side OLD current sources are required to detect if a passive OLD event has occurred.

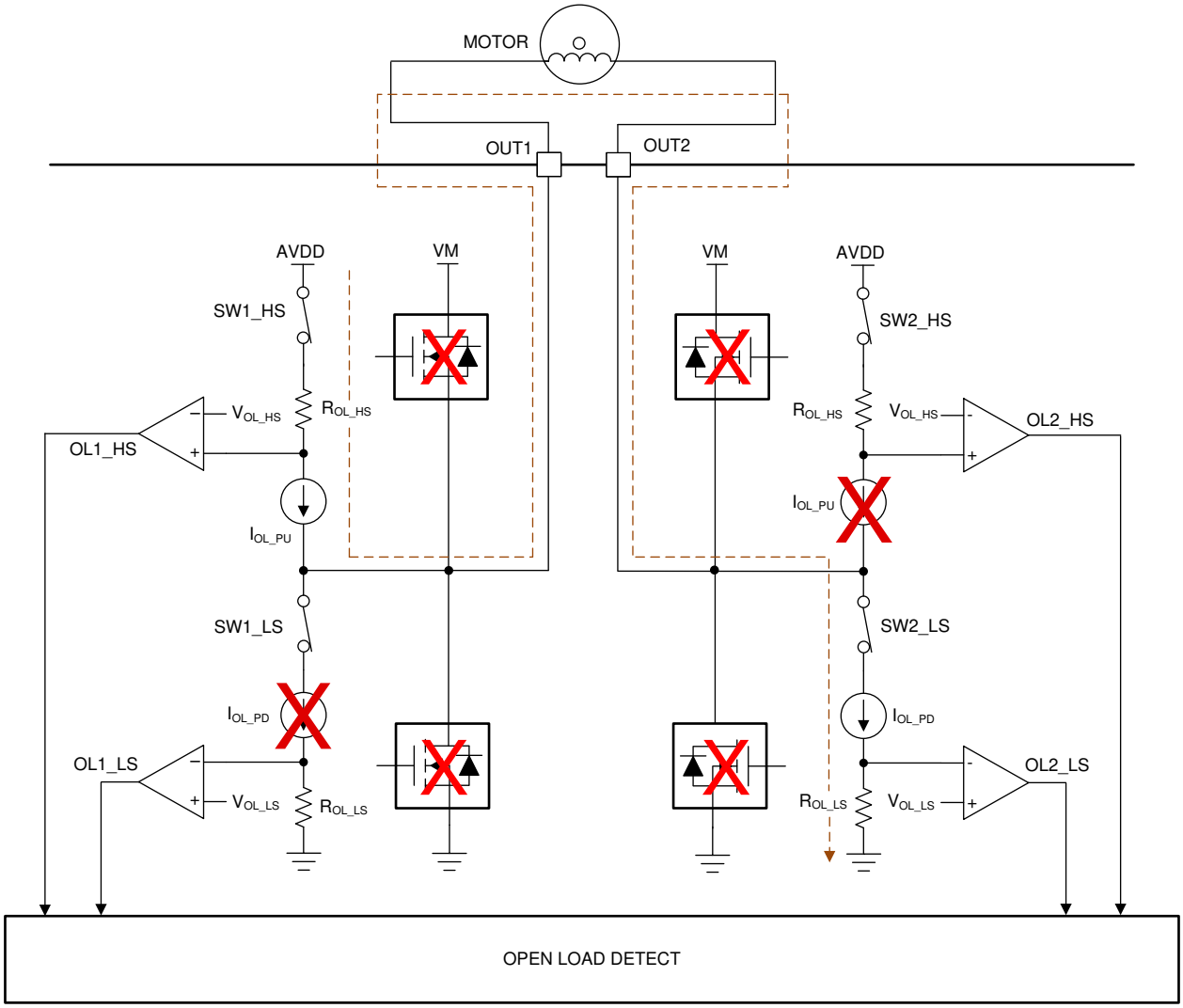

Figure 2-1. Passive OLD Circuit in an Integrated Driver

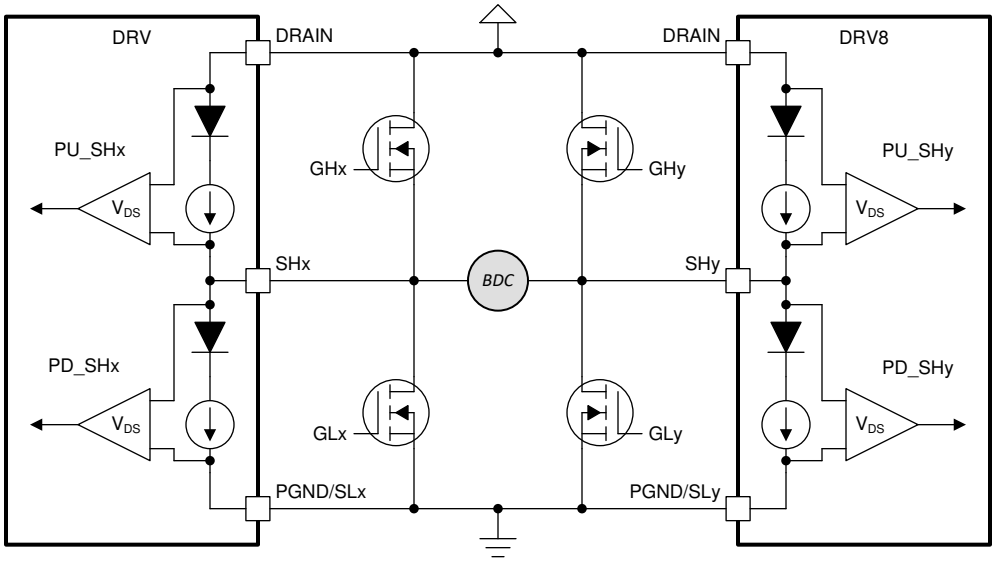

Figure 2-2. Passive OLD Circuit in a Brushed DC Gate Driver

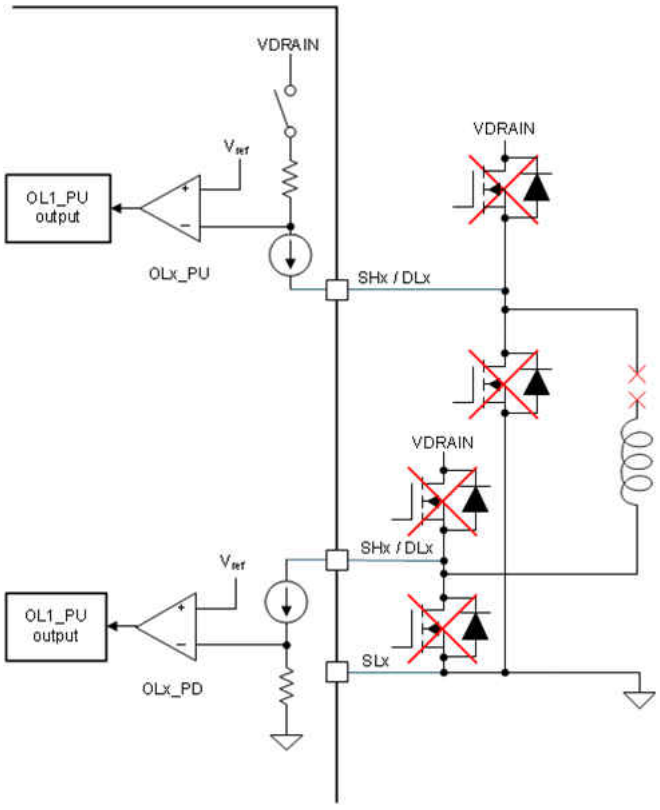

Figure 2-3. Passive OLD Circuit in a Brushless DC Gate Driver

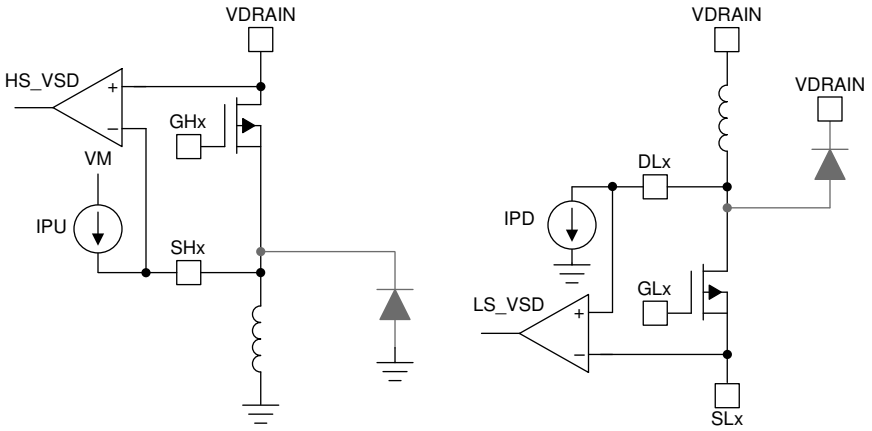

Figure 2-4. Passive OLD Load Configurations not supported in a Brushless DC Gate Driver

2.1 Circuit Operation and Detection

This section presents the circuit implementation of the passive OLD diagnostic of the DRV8847 device. Note that the values of the parameters utilized as an example are from the device's datasheet. The H-bridge OLD sequence consists of turning ON the high-side switch (SW1_HS) of OUT1's half-bridge and the low-side switch (SW2_LS) of OUT2's half-bridge together. Depending on how OUT1 and OUT2 connect to the load, there can be three cases that can cause at least one comparator output to be set to "1"": H-bridge open, H-bridge short, or load connected in the H-bridge. Note that at least one passive OLD comparator being set to “1” does not mean a passive OLD event has occurred. Only in the H-bridge open case does a passive OLD flag occur. This case also applicable for drivers that have passive OLD diagnostic and can drive a unidirectional load tied to supply or GND through a single half-bridge, such as the DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1 devices of the DRV89XX-Q1 device family. For integrated drivers, the conditions which set the passive OLD comparator outputs to "1" are when $V_{OLx\_HS}(+) > V_{OLx\_HS}$ and when $V_{OLy\_LS}(-) < V_{OLy\_LS}$ for an H-bridge open case, where x is for half-bridge x and y is for half-bridge y. For gate drivers, the conditions which set the passive OLD comparator outputs to "1" are when $V_{OLx\_PU}(+) > V_{REF}$ and when $V_{OLy\_PD}(-) < V_{REF}$.

2.1.1 H-Bridge Open

If no load is connected between OUT1 and OUT2, then no current flows from the internal regulator (AVDD). This OLD example will show why an OLD flag occurs when the H-bridge is open. The voltages on the positive terminal of high-side comparator of OUT1's half-bridge (OL1_HS) and the negative terminal of low-side comparator of OUT2's half-bridge (OL2_LS) will be as follows:

High-side comparator of OUT1's half-bridge (OL1_HS)

Since no current is flowing from AVDD, the voltage on OUT1 (which is also the positive terminal of OL1_HS is clamped to AVDD (for example 4.2 V). OL1_HS has positive input that can be called $V_{OL1\_HS}(+)$ and negative input V_{OL_HS}. The V_{OL_HS} is also called the OLD threshold voltage. Since $V_{OL1\_HS}(+)$ (4.2 V) is greater than V_{OL_HS} (2.3 V), the OL1_HS output is set to "1".

Low-side comparator of OUT2's half-bridge (OL2_LS)

Since no current flows through the SW2_LS switch, the negative terminal of OL2_LS ($V_{OL2\_LS}(-)$) is pulled down to 0.0 V (GND). OL2_HS has positive input V_{OL_LS}. Since V_{OL_LS} (1.2 V) is greater than $V_{OL2\_LS}(-)$ (0.0 V), the OL2_LS output is set to "1". If both OL1_HS and OL2_LS are set to "1", it signifies an OLD.

2.1.2 H-Bridge Short

If there is a short between OUT1 and OUT2, then a short circuit current (I_{SC}) flows from AVDD. A successful OLD flag in an H-bridge short depends on the I_{SC}. I_{SC} will depend on AVDD, on the high-side resistor (R_{OL_HS} = 12 kΩ) and on the low-side resistor (R_{OL_LS} = 15 kΩ). The I_{SC} equation is as follows:

$$I_{SC} = \frac{V_{AVDD}}{15k\Omega + 12k\Omega} = \frac{V_{AVDD}}{27k\Omega} \quad (1)$$

Hence the I_{SC} is calculated using Equation 1 as,

$$I_{SC} = \frac{V_{AVDD}}{27k\Omega} = \frac{4.2V}{27k\Omega} = 155.56\mu A \quad (2)$$

This OLD example will show how an OLD flag cannot occur when there is a short on the H-bridge. The voltage changes due to an H-bridge short on the positive terminal of OL1_HS ($V_{OL1\_HS}(+)$) and on the negative terminal of OL2_LS (V_{OL1_HS}) will be as follows:

High-side comparator of OUT1's half-bridge (OL1_HS)

I_{SC} (155.56 µA) is flowing from AVDD. Therefore, the voltage on the positive terminal of OL1_HS is calculated as,

$$V_{OL1\_HS}(+) = V_{AVDD} - I_{SC} \times 12k\Omega \quad (3)$$

Using Equation 3, the $V_{OL1\_HS}(+)$ is calculated as,

$$V_{OL1\_HS}(+) = 4.2V - 155.56\mu A \times 12k\Omega = 2.33V \quad (4)$$

Since $V_{OL1\_HS}(+)$ (2.33 V) is greater than V_{OL1_HS} (2.3 V), the output of OL1_HS is set to "1".

Low-side comparator of OUT2's half-bridge (OL2_LS)

The pull down current of I_{SC} (155.56 µA) is flowing from AVDD to the SW2_LS switch. Therefore, the voltage on the negative terminal of OL2_LS ($V_{OL2\_LS}(-)$) is calculated as,

$$V_{OL2\_LS}(-) > I_{SC} \times 15k\Omega \quad (5)$$

Using Equation 5, the $V_{OL2\_LS}(-)$ value is,

$$V_{OL2\_LS}(-) = 155.56\mu A \times 15k\Omega = 2.33V \quad (6)$$

Since $V_{OL2\_LS}(-)$ (2.33 V) is greater than V_{OL_LS} (1.2 V), the output of OL2_LS is set to"0". The output of OL1_HS is set to "1" and the output of OL2_LS is set to "0". Therefore, this case is not considered as an OLD.

2.1.3 Load Connected in H-Bridge

The OLD monitoring when there is a load to the H-bridge will depend on the load resistance (R_L). The load's current (I_L) for a load connected between OUT1 and OUT2 is calculated as,

$$I_{LOAD} = \frac{V_{AVDD}}{12k\Omega + R_L + 15k\Omega} = \frac{V_{AVDD}}{R_L + 27k\Omega} \quad (7)$$

This OLD example will trigger an OLD event. The voltages at the positive terminal of OL1_HS ($V_{OL\_HS}(+)$) and the negative terminal of OL2_LS (V_{OL_HS}) will be as follows:

High-side comparator of OUT1's half-bridge (OL1_HS)

If $V_{OL\_HS}(+)$ is greater than V_{OL_HS} (2.3 V), the output of OL1_HS is set to "1". The voltage comparison between $V_{OL\_HS}(+)$ and V_{OL_HS} required for the output of OL1_HS to be set to "1" is determined as:

$$V_{OL\_HS} < V_{AVDD} - I_{LOAD} \times 12k\Omega \quad (8)$$

Putting Equation 7 into Equation 8,

$$V_{OL_{HS}} < V_{AVDD} - \frac{V_{AVDD} \times 12k\Omega}{R_L + 27k\Omega} \quad (9)$$

Solving Equation 9 for the load resistance (R_L), R_L is expressed as,

$$R_L > \frac{V_{AVDD} \times 12k\Omega}{V_{AVDD} - V_{OL\_HS}} - 27k\Omega \quad (10)$$

By using the values of V_{AVDD} and V_{OL_HS} in Equation 10, the load resistance (R_L) is calculated as (-)473.7 Ω. Since the value of the resistance is negative, V_{OL_HS}(+) is greater than V_{OL_HS} (2.3 V) and the output of OL1_HS is is set to "1".

Low side comparator of OUT2's half-bridge (OL2_LS)

If the voltage at negative terminal of OL2_LS (V_{OL_LS}(-)) is less than V_{OL_LS} (1.2 V), then the output of OL2_LS is set to "1". Hence, the voltage comparison between V_{OL_LS}(-) and V_{OL_LS} required for the output of OL2_LS to be set to "1" is calculated as:

$$V_{OL\_LS} > I_{LOAD} \times 15k\Omega \quad (11)$$

Putting Equation 7 to Equation 11,

$$V_{OL\_LS} > \frac{V_{AVDD} \times 15k\Omega}{R_L + 27k\Omega} \quad (12)$$

Solving Equation 12 for R_L, R_L is expressed as,

$$R_L > \frac{V_{AVDD} \times 15k\Omega}{V_{OL\_LS}} - 27k\Omega \quad (13)$$

Using the values of V_{AVDD} and V_{OL_LS} in Equation 13, R_L has to be greater than 25.5 kΩ for OL2_LS to be set to "1". Since the output of OL1_HS is always set to "1", the OLD status is solely dependent on the output of OL2_LS. If the R_L is less than 25.5 kΩ, then an OLD flag will not occur.

2.2 Circuit Operation and Detection in DRV824x

This section presents the circuit implementation of the passive OLD diagnostic of the DRV824x-Q1 device. DRV824x has the dedicated comparator for passive OLD which is called OLP_CMP.

The user can determine the impedance on the OUTx node using off-state diagnostics in the STANDBY state when the power FETs are off. With these diagnostics, it is possible to detect the following fault conditions passively:

- Output short to VM or GND < 100 Ω
- Open load > 1K Ω for full-bridge load or low-side load
- Open load > 10K Ω for high-side load, VM = 13.5 V

The OLP combinations and truth table for a no fault scenario vs. fault scenario for a full-bridge load in PH/EN or PWM modes is shown in Table 2-1.

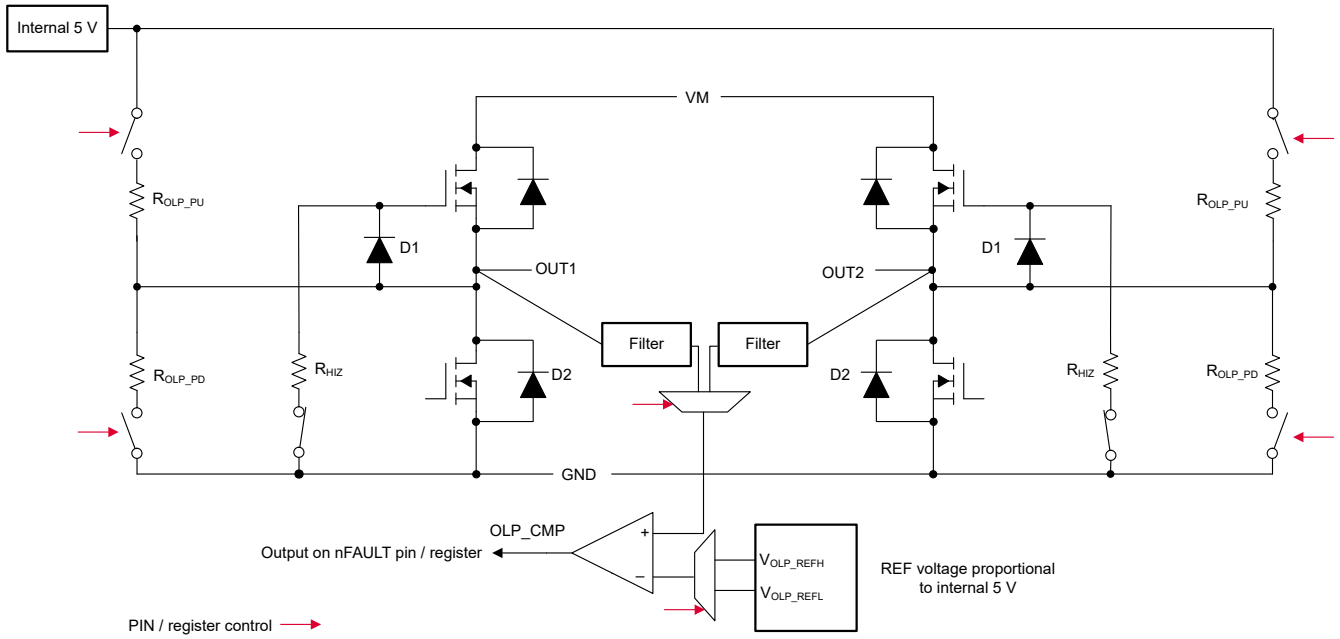

Figure 2-5. OLP Combinations

Table 2-1. DRV824x-Q1 Off-State Diagnostics Table PH/EN or PWM Mode

User Inputs				OLP Set-Up				OLP CMP Output			
nSleep	DRVOFF	EN/IN1	PH/IN2	OUT1	OUT2	CMP REF	Output Selected	Normal	Open	GND Short	VM Short
1	1	1	0	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFH}	OUT1	L	H	L	H
1	1	0	1	R_{OLP_PU}	R_{OLP_PD}	V_{OLP_REFL}	OUT2	H	L	L	H
1	1	1	1	R_{OLP_PD}	R_{OLP_PU}	V_{OLP_REFL}	OUT2	H	H	L	H

Example for test procedure is following. First execute test with first row. nSLEEP=1, DRVOFF=1, EN/IN1=1 and PH/IN2=0. If OLP CMP output is Low, output condition is expected as Normal or GND short. Then try next row as nSLEEP=1, DRVOFF=1, EN/IN1=0 and PH/IN2=1. If OLP CMP output is High, output is expected as normal. If OLP CMP output is Low, output is expected as GND short.

3 Active Open Load Detection

The active OLD is the diagnostic that is carried out during load operation (current through the load is not zero). This diagnostic feature ensures that the load is connected to the driver during operation. However, it cannot detect if the load's terminals are disconnected from the power-stage before the load operation begins.

Figure 3-1 shows the operation of the active OLD diagnostic. (Refer to DRV89XX-Q1 device family for more details). If any of the FETs are turned ON and the current flowing in the particular FET is less than the OLD's current threshold (I_{OLD}) for time magnitude larger than the OLD deglitch time (t_{OLD}), then an OLD is detected.

In stepper motor integrated drivers, the active OLD depends on the winding current in any of the coils. If the winding current in any coil drops below the open load current threshold (I_{OLD}) and also on the I_{TRIP} level set by the indexer, an open-load condition is detected.

In DRV8873, DRV8873-Q1 and the DRV824x-Q1 devices, the active OLD is based on the voltage in a high-side FET's body diode during the current re-circulation. The current re-circulation occurs through the high-side FET's body diode in asynchronous rectification. In the gate drivers, the active OLD is based on the voltage in both the high-side or low-side FET's body diode during the current re-circulation.

Figure 3-2 shows the flow of current during forward drive and during current re-circulation. The high-side FET of OUT1 is in operating state. The voltage across the body diode of the current re-circulation high-side FET is compared with the fixed reference OLD threshold voltage (V_{OL_HS}) to detect the OLD event.

In gate drivers, each half-bridge's (phase's) active OLD is enabled independently. For OLD to occur, a load needs to be connected across an H-bridge configuration. An OLD occurs when the voltage drop across the body diode of the current re-circulation FET does not exhibit overshoot greater than the V_{OLA} over VM during the current-re-circulation time. An OLD does not occur if the energy stored in the load is high enough to cause an overshoot greater than the V_{OLA} over VM. The overshoot is caused by the negative-current flowing through the body diode of the current re-circulation FET.

Active OLD in DRV8873-Q1, DRV8873 and in BLDC gate drivers, when compared to the negative-current OLD diagnostic, are different since the former will flag the OLD in asynchronous rectification while the latter will flag the OLD in synchronous rectification.

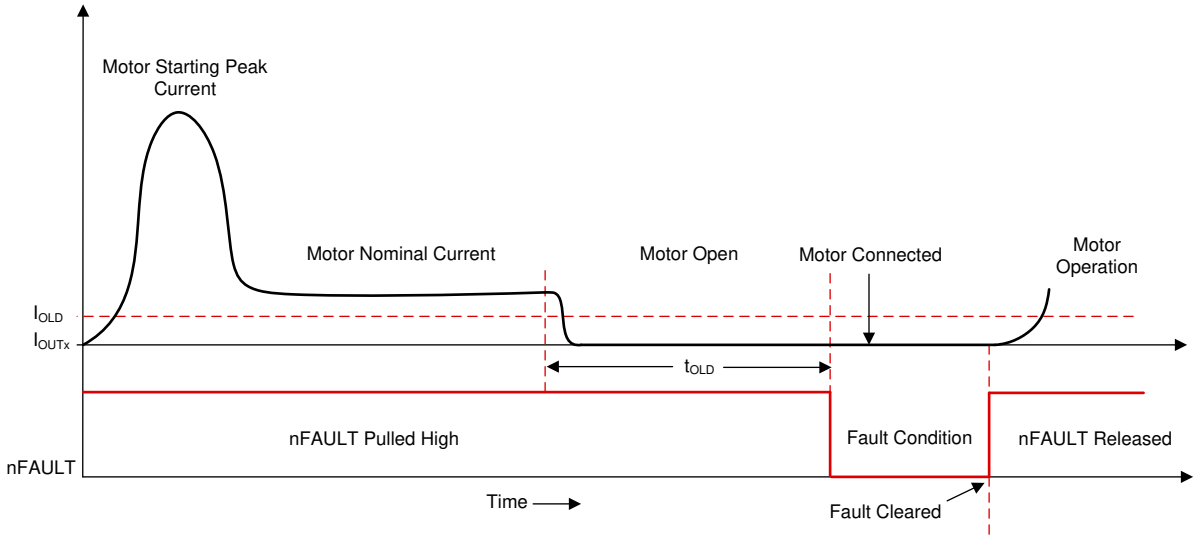

Figure 3-1. Active OLD Operation

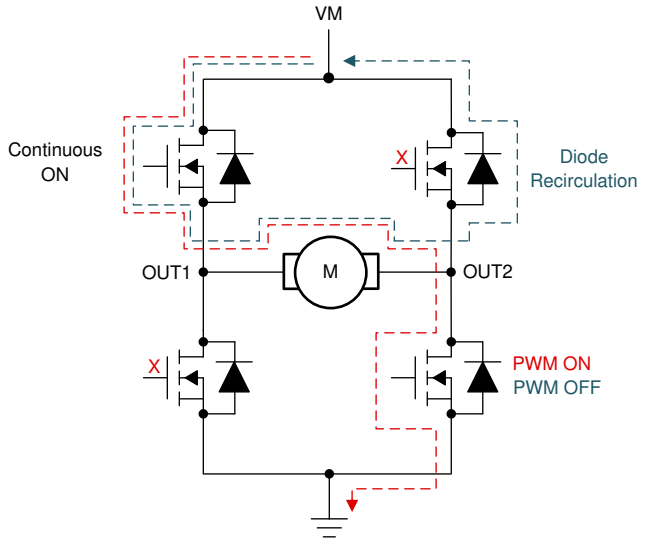

Figure 3-2. Forward Drive and Braking in Asynchronous Rectification

3.1 Circuit Operation and Detection

Figure 3-3 shows the circuit implementation of the active OLD in integrated drivers. The high-side FET of the OUT1 channel and low-side FET of the OUT2 are in the operating state. A reference voltage generator generates equivalent reference voltages for the OLD comparators' negative input terminals, while the positive terminals reflect the actual voltage in the FETs. As shown in Figure 3-3, the outputs of OL1_HS and OL2_LS are set to "1" when the output voltages (V_{OUT1_HS} and V_{OUT2_LS}) become greater than the reference voltage (V_{OL_REF}) of the comparators,

$$V_{OL\_REF} < V_{OUT1\_HS}$$
$$V_{OL\_REF} < V_{OUT2\_LS} \quad (14)$$

In this example, the reference-FET is any of the four FETs tied to the current reference sources (I_{OL_REF}). The V_{OL_REF} is determined by I_{OL_REF} and the on-state resistance of the reference-FET ($R_{DS(ON)\_REF}$). Now, the V_{OUT1_HS} and the V_{OUT2_LS} are determined by the current and on-state resistances ($R_{DS(ON)}$) through the FETs that drive the load. When an OLD event occurs, the current through the FETs must be greater than the OLD current threshold. For these equations, the current through the FETs is called I_{OL}. Hence, by putting all of these parameters in Equation 14, the equation V_{OL_REF} equation is modified to,

$$I_{OL\_REF} \times R_{DS(ON)\_REF} < I_{OUTx} \times R_{DS(ON)} \quad (15)$$

Hence, the I_{OLD} can be calculated as,

$$I_{OUTx} > I_{OL\_REF} \times \left(\frac{R_{DS(ON)\_REF}}{R_{DS(ON)}} \right) = I_{OLD} \quad (16)$$

Equation 16 shows that the OLD depends on the on-state resistance ratio of the reference-FETs to the FETs driving the load.

Putting the values of on-state resistance ratio (450:1) and the reference generator pull-down current (20 µA), the OLD current threshold can be calculated as,

$$I_{OUTx} > \left(20 \times 10^{-6}\right) \times \left(\frac{450}{1} \right) = I_{OLD} = 9\,mA \quad (17)$$

Hence, if current through the load is greater than 9 mA while OLD is active, an OLD event is registered.

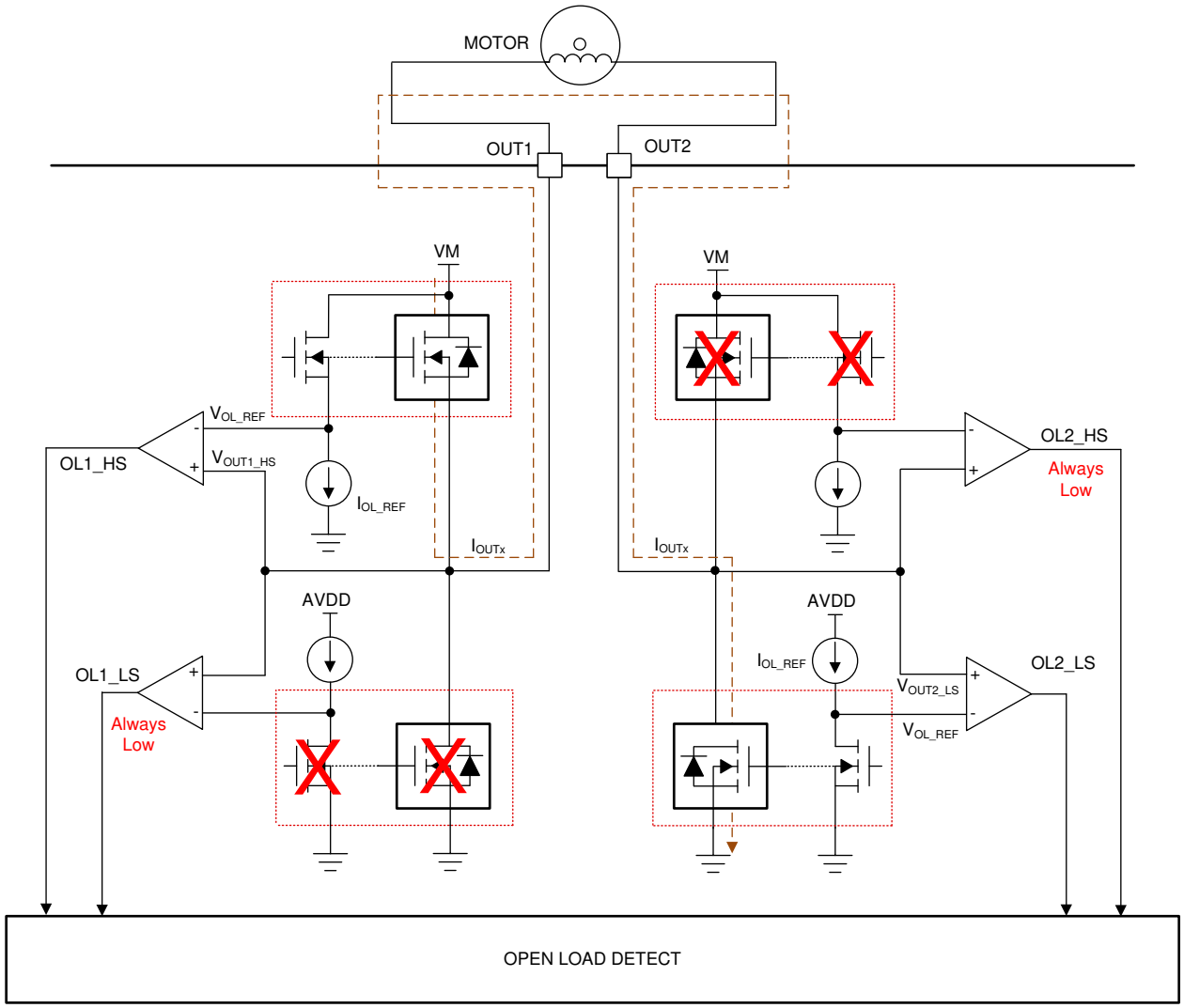

Figure 3-3. Active OLD Circuit in Brushed DC Motor Integrated Drivers

As for the circuit implementation in DRV8873, DRV8873-Q1 and the DRV824x-Q1 devices, Figure 3-4 shows the circuit implementation of the active OLD of DRV8873/DRV8873-Q1. For the OL1_HS comparator, if the drain-to-source voltage across the high-side driving FET is less than the V_{OL_HS} OLD threshold, OLD1_HS output is set to "1" and an OLD is detected. For the OL2_HS comparator, if the body diode voltage (V_D) is less than the V_{OL_HS} OLD threshold, OLD2_HS output is set to "1" and an OLD is detected. Due to the current re-circulation through the body diode (I_{OL}), the body diode voltage (V_D) depends on I_{OUTX} for an OLD to occur.

There is a dependency on the operating conditions and on external circuitry, such as the output capacitors, that can cause an OLD to be reported even though the load is present. This case might occur during a direction change or for small load currents respectively small PWM duty cycles.

Figure 3-5 shows the circuit implementation for the active OLD of DRV824x-Q1. Device can detect an open load detection in the ACTIVE state during high-side recirculation. This includes high-side load connected directly to VM or through a high-side FET on the other half-bridge. During a PWM switching transition, the inductive load current re-circulates into VM through the HS body diode when the LS FET is turned OFF. The device looks for a voltage spike on OUTx above VM during the brief dead time, before the HS FET is turned ON. To observe the voltage spike, this load current needs to be higher than the pull down current (IPD_OLA) on the output asserted by the FET driver. Absence of this voltage spike for "3" consecutive re-circulation switching cycles indicates a loss of load inductance or increase in load resistance and is detected as an active open detection fault.

Finally, when using active OLD in gate drivers, capacitors must be placed between the load phase nodes and GND. These capacitor are required for BLDC motors and both bi-directional and unidirectional BDC motors at the phase nodes. If a solenoid load is connected, the capacitors are not required. Capacitors must be sized as:

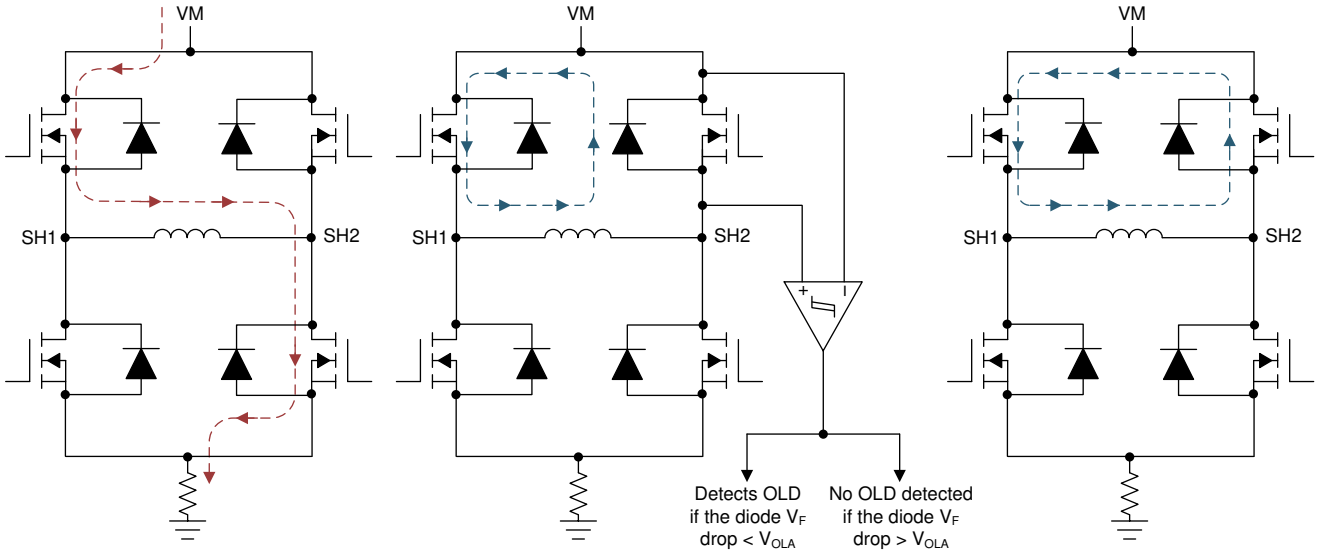

Figure 3-4. Circuit for Active OLD in a DRV8873-Q1 and in a DRV8873 device

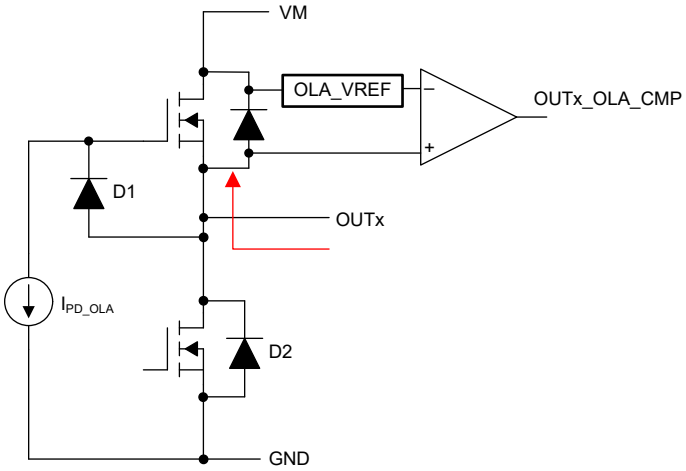

Figure 3-5. Circuit for Active OLD in a DRV824x-Q1 device

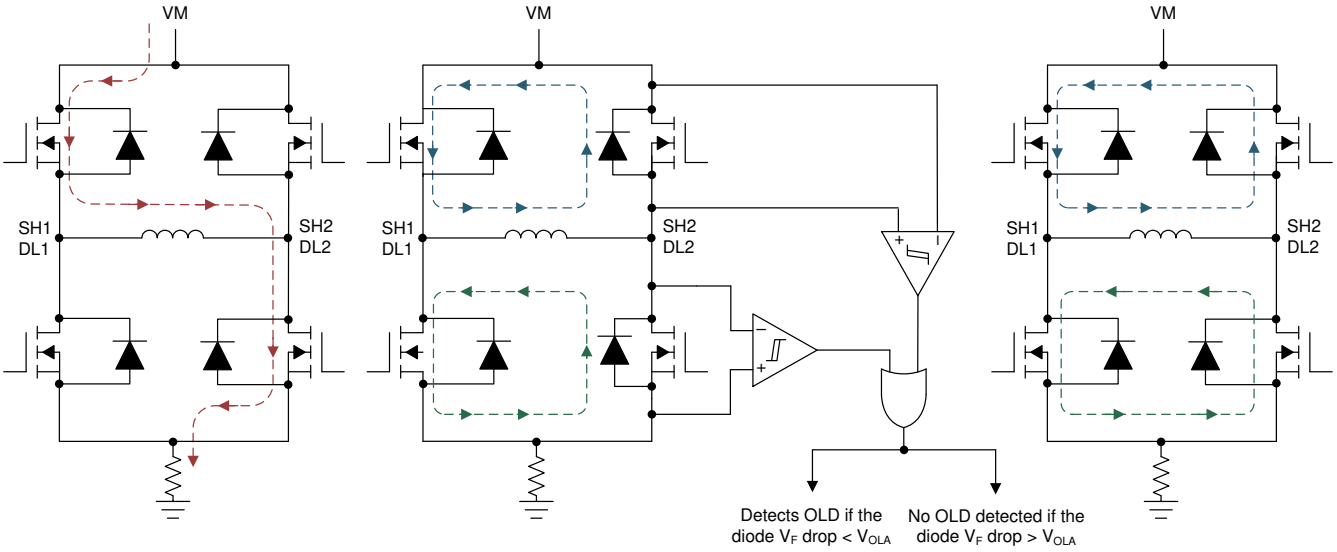

Figure 3-6. Circuit for Active OLD in a BLDC Gate Driver

$$C_{phase} \geq \frac{V_{TH} \times C_{rss}}{V_{OLA(min)}} - C_{oss} \quad (18)$$

Where V_{TH} is the threshold voltage of the FETs and $V_{OLA(min)}$ in the DRV8343-Q1 and DRV8340-Q1 is 150 mV. The values of the FET C_{rss} and C_{oss} should be used for 0 V V_{DS}. Derating of C_{phase} must be considered when selecting the capacitance.

4 Low-Current Active Open Load Detection

Low-current active OLD, found in the DRV89xx-Q1 devices, is designed for loads with a smaller motor nominal current than the I_{OLD} of active OLD. Figure 4-1 shows that the low-current active OLD threshold (I_{OLD_LOW}) replaces the I_{OLD} from the active OLD. In low-current active OLD, I_{OLD_LOW} is around 10 times less than the active OLD's current OLD threshold. With I_{OLD_LOW} being 10 times less than I_{OLD} permits for more flexibility in OLD when utilizing a load that requires a small nominal current to trigger an OLD event. If a low-side FET is turned ON and the current flowing in that low-side FET is less than the I_{OLD_LOW} for at least the OLD deglitch time (t_{OLD}), then an OLD event has occurred.

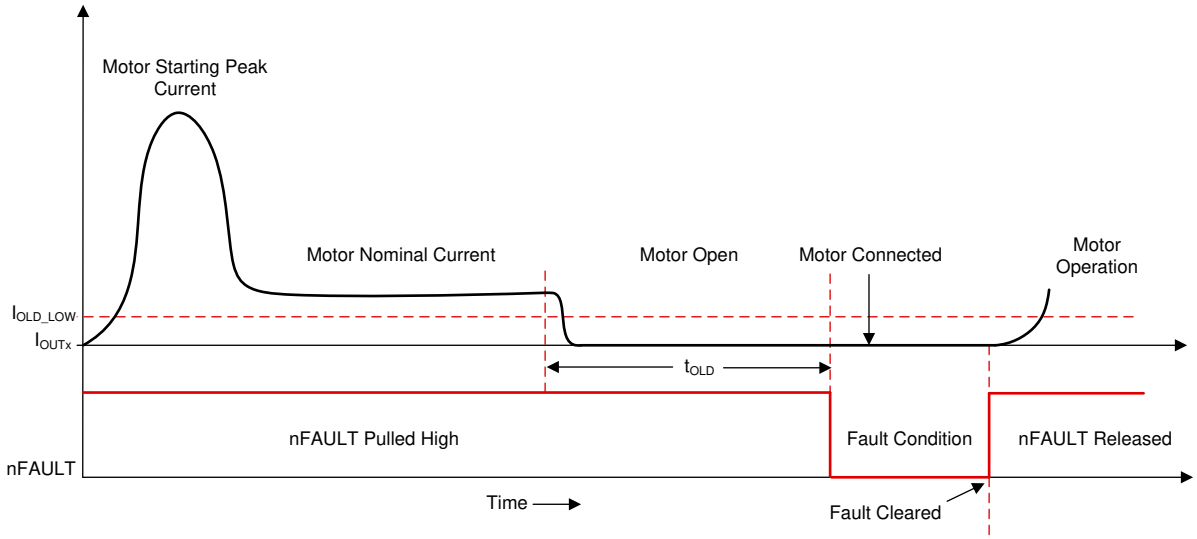

Figure 4-1. Low-Current Active OLD Operation

The low-current active OLD has trade offs that must be considered:

- In the DRV89xx-Q1 devices, this OLD is only applicable for the current flowing in the low-side FETs, meaning it cannot be detected using the high-side FETs.
- If low-current active OLD is used, the overcurrent protection threshold for the low-side FET is also reduced by 11 times.
- The $R_{DS(ON)}$ of the low-side FET will increase by 11 times, hence the thermal performance has to be monitored. However, given the current across the low-side FET is expected to be low, the thermal dissipation of the low-side FET is expected to be limited.

5 Negative-Current Active Open Load Detection

In negative-current active OLD, found in the DRV89xx-Q1 devices, the current OLD threshold is negative (I_{OLD_NEG}). The negative current re-circulation occurs through the current re-circulation FET in synchronous rectification. Figure 5-1 shows the operation of the H-bridge when forward driving and when using synchronous rectification. If negative-current active OLD is not utilized, the device can show a false OLD since the current re-circulating through the current re-circulation FET is negative and it is less than the positive current OLD threshold the other active OLD diagnostics use. When the negative-current active OLD is enabled, this negative flow of current through the current re-circulation FET does not show false OLD event due now utilizing a negative-current active OLD current setting (I_{OLD_NEG}).

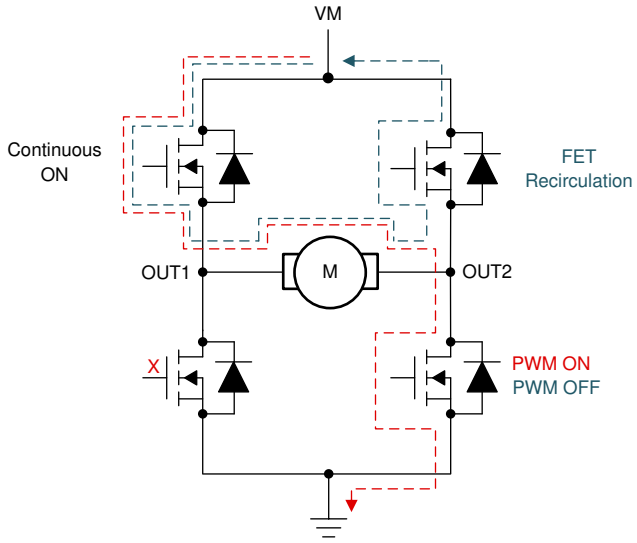

Figure 5-1. Forward Drive and Braking in Synchronous Rectification

Figure 5-2 shows the waveforms of false OLD when the negative-current active OLD is not active in an H-bridge configuration. In synchronous rectification with high-side current re-circulation, one of the driving FETs is always turned ON and the other driven half-bridge's low-side and high-side FETs operate in a complimentary manner. Initially, for the first PWM cycle, all OLD diagnostics are disabled to show the currents in the different FETs during the load operation. If the active OLD diagnostic is enabled in the second PWM cycle, then the device registers a false OLD flag during the high-side FET current re-circulation due to the negative current. This false flag will cause both of the switching high-side and low-side FETs to be turned OFF. Since the fault causes OUT2_HS to turn OFF, the high-side FET's body diode instead of the high-side FET conducts to complete the current re-circulation path back to the supply.

This false OLD flag is eliminated by enabling the negative-current OLD. Figure 5-3 the negative-current active OLD current setting (I_{OLD_NEG}) is enabled for the current re-circulation FET of the switching half-bridge. Since the current threshold is negative and greater than the current re-circulating through the current re-circulation FET, the false OLD flag is prevented and the FETs of the switching half-bridge are not disabled in the second PWM cycle. With setting the current threshold to a negative value, the OLD flags where the load is disconnected during synchronous rectification can be detected. There is no tradeoff to enabling the negative-current active OLD.

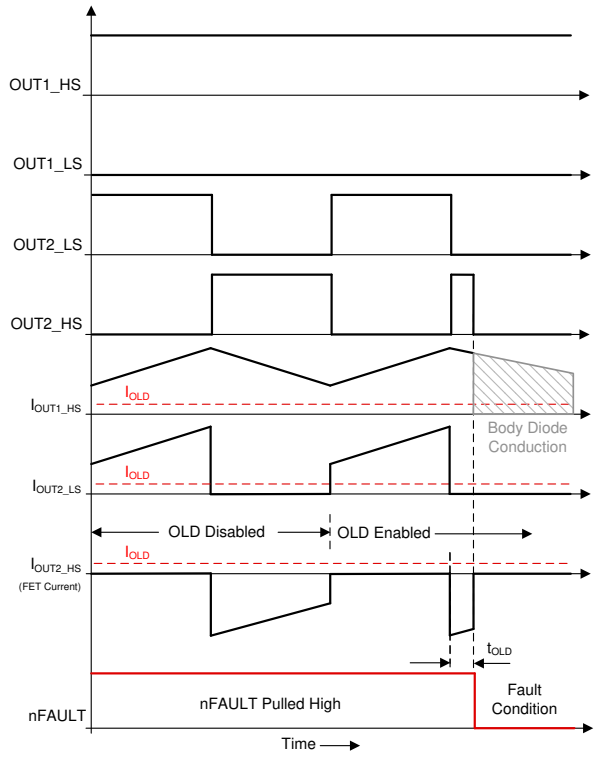

Figure 5-2. False OLD Flag with Negative-Current OLD Disabled

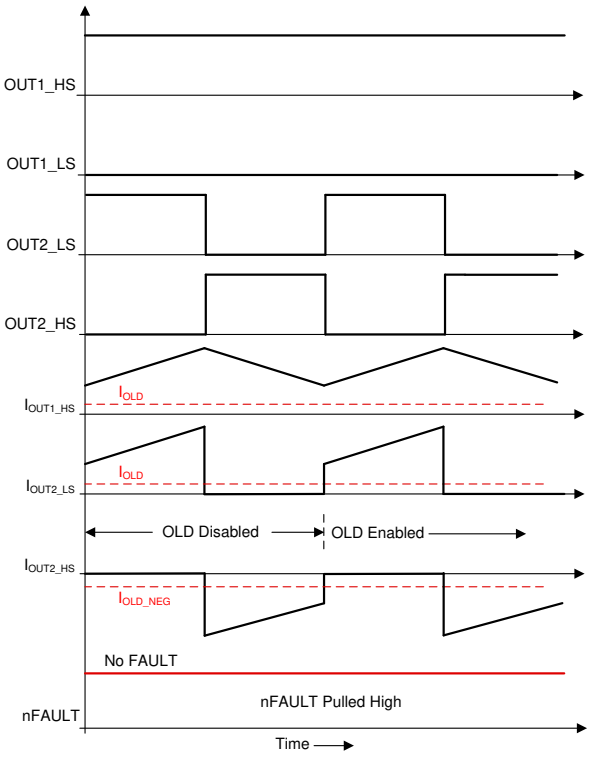

Figure 5-3. No False OLD Flag with Negative-Current OLD Enabled

6 Summary

This application report has presented different load connections found in OLD diagnostics, such as the half-bridge load connected to supply, the half-bridge load connected to ground and the H-bridge load, along with five types of OLD diagnostics: passive, active, low-current active, and negative-current active OLDs.

The passive OLD diagnostic is suited for the applications which require to check the connectivity of the driver to the load before powering the driver. In such applications, there can be hazard of the open wire connecting to other low-voltage circuitry, which can cause potential damage to this circuitry, or to power lines, which can cause an overcurrent event. Passive OLD in low-side integrated drivers only requires low-side OLD current sources to detect a passive OLD event. BLDC gate drivers require the load phase pin to ground capacitances to discharge before the passive OLD is enabled.

The active, low-current active, and negative-current active OLD diagnostics are suited for applications where the driver current is to be monitored while the load is running. The active OLD can operate in both continuous and in PWM operation. The DRV8873, DRV8873-Q1 and the DRV824x-Q1 devices can only detect an active OLD during high-side asynchronous rectification. BLDC gate drivers require the active load to be connected in an H-bridge configuration. The low-current active OLD sets a 10x current OLD threshold to give a larger flexibility to detect loads with smaller load nominal currents than the I_{OLD}. The negative-current active OLD changes the I_{OLD} to I_{OLD_NEG} to account for the negative high-side or low-side FET current re-circulation in synchronous rectification and prevent a false active OLD flag.

7 References

- Texas Instruments, *DRV8847 Dual H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8889-Q1 Automotive H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8899-Q1 Automotive H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8860 Eight Serial Interface Low-Side Driver* Data Sheet
- Texas Instruments, *DRV8806 Quad Serial Interface Low-Side Driver* Data Sheet
- Texas Instruments, *DRV89xx-Q1 Automotive Multi-Channel Half-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8873-Q1 Automotive H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8873 Automotive H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8343-Q1 Automotive H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV8340-Q1 Automotive H-Bridge Motor Driver* Data Sheet
- Texas Instruments, *DRV824x-Q1 Automotive H-Bridge Motor Driver* Data Sheet

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2020) to Revision C (April 2022)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2
• Added new Section 2.2	10
• Updated Section 3	11
• Updated Section 3.1	12
• Updated Section 6	18

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