Application Report
SLVAE38A–January 2018–Revised April 2019

MOSFET Driver Circuit Design Guide for TPS512xx

Edwin Zang, Jason Wang

ABSTRACT

The driver circuit parameters are critically important for a controller. A better selection of parameters not only increases the system safety, but also improves the efficiency. First, this application report talks about MOSFET parameters and the turning on/off procedure. Then, the IC driver capability and bootstrap circuit are introduced. Lastly, the document uses the TPS51285B as an example to explain how to adjust driver parameters.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

When the controller IC of TPS512xx (including TPS51225, TPS51275, TPS51285, TPS51220, and others) is applied in a circuit, the selection of MOSFET and driver parameters are necessary. The more reasonable MOSFET and driver parameters have a better effect on efficiency, system safety, and EMI. Driver parameters for the controller include bootstrap resister, bootstrap cap, and gate resister.

2 MOSFET

2.1 MOSFET Parameters

This section mainly introduces the parameters of MOSFET and how they affect circuit performance. The MOSFET CSD87330Q3D *CSD87330Q3D Synchronous Buck NexFET Power Block Data Sheet* is introduced as an example.

BV_{DSS}, I_{DSS}, I_{GSS}, $V_{GS(th)}$, and $Z_{DS(on)}$ are easily understood. Enough BV_{DSS} (drain to source voltage) is required. A lower $Z_{DS(on)}$ is better because it consumes lower power loss. I_{DSS} and I_{GSS} are leakage current, which is always very small.

Dynamic characteristics including Qg, parasitic cap, and rising time are more important for circuit. These parameters affect switching time and switching loss. Figure 1 shows the switching model of the MOSFET and the most important parasitic components that influence switching performance.

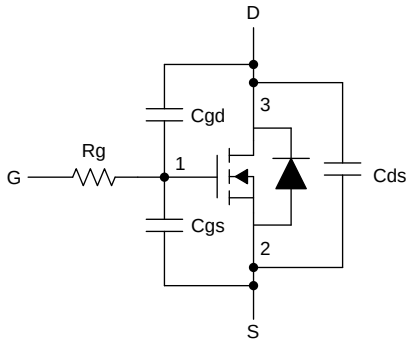


Figure 1. MOSFET Model

There is a parasitic cap, C_{GD}, between the drain and gate. C_{GS} is between the gate and source. C_{DS} is between the drain and source. In the MOSFET data sheet, these capacitors are not mentioned directly. Their values are given indirectly by C_{ISS}, C_{OSS}, and C_{RSS} capacitor values. Equation 1, Equation 2, and Equation 3 show how to calculate these values.

$$C_{GD} = C_{RSS} \quad (1)$$

$$C_{GS} = C_{ISS} - C_{RSS} \quad (2)$$

$$C_{DS} = C_{OSS} - C_{RSS} \quad (3)$$

When the switch mode operation of the MOSFET is considered, the goal is to switch between the lowest and highest resistance states of the device. The switching time between two states is influenced by the parasitic cap. Ultimately, the switching performance of the MOSFET is determined by how quickly the voltages can be charged across these capacitors. If the parasitic cap is larger, it needs a stronger driver and takes more time to charge the cap. It consumes more switching loss, and the efficiency is lower. Therefore, in high speed switching applications, the most important parameters are the parasitic capacitances of the MOSFET.

MOSFET also gives a parameter Qg that indicates MOSFET switch performance from practical turning on or off side. In the MOSFET EC table, Qgd, Qgs, Qg(th), and Qoss are also given. Qg is the total gate charge. If Qg is larger, it needs a stronger driver and more charge. Figure 2 shows the relationship between Qg and Vgs voltage and how much charge the gate of MOSFET requires at different gate voltage. For example, if V_{GS} wants to get 5 V, the gate of MOSFET need to be charged about 4 nc. $V_{GS,miller}$ voltage can also be derived from Figure 2. In this example, it is about 2.5 V.

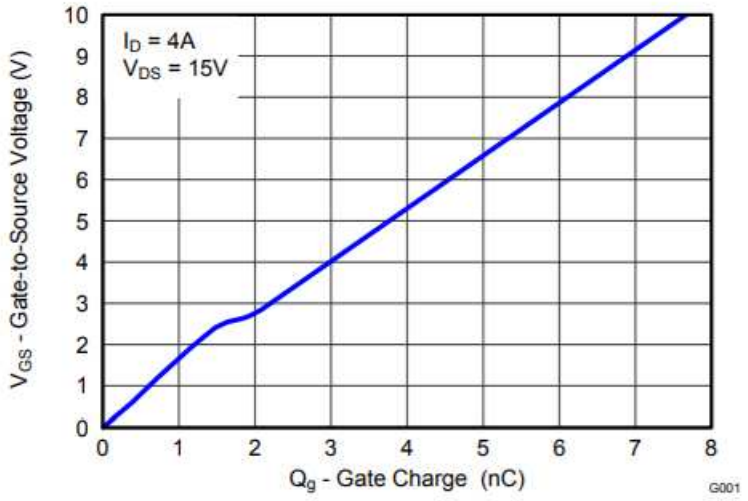


Figure 2. MOSFET Gate Charge

The next important parameter to mention is the gate resistance, RG. This parasitic resistance describes the resistance associated by the gate signal distribution within the device. Its importance is critical in high speed switching applications because it is located between the driver and the input capacitor of the device, directly impeding the switching times and the dv/dt immunity of the MOSFET.

Rising time is introduced in turning on procedure.

2.2 MOSFET Turnon and Turnoff Procedure

Figure 3 shows the MOSFET turning on procedure. The left side shows a simple driver circuit and MOSFET. It also gives current direction when the MOSFET turns on. The right side gives the waveforms of V_{GS}, I_G, V_{DS}, and I_D.

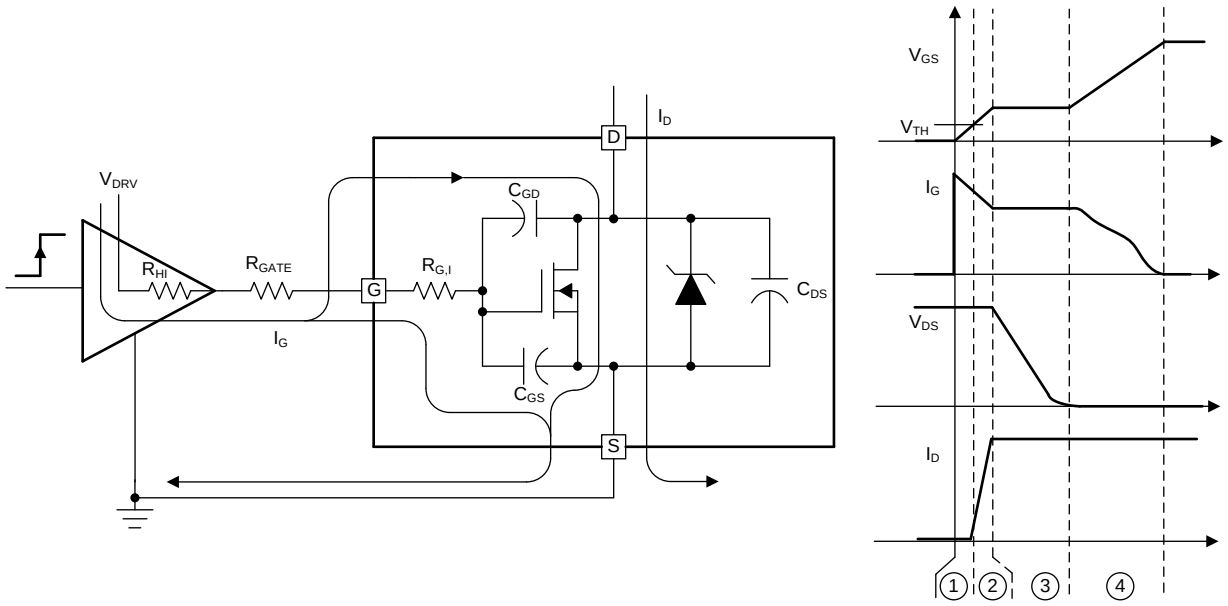


Figure 3. Turnon Procedure

In the first interval, the input capacitance of the device is charged from 0 V to V_{TH}. During this interval, most of the gate current is charging the C_{GS} capacitor. At this time, a small current is flowing through the C_{GD} capacitor. As the voltage increases at the gate terminal, the C_{GD} voltage of the capacitor has to be slightly reduced. This period is called the turnonon-on delay. In the MOSFET data sheet, $t_{d(on)}$ indicates this time. During this time, it cannot produce switching loss, because there is no current that goes through the MOSFET. Qg(th) is the required charge of MOSFET gate. If C_{GS} is large, then Qg(th) requires an increased charge.

Once the gate is charged to the threshold level, the MOSFET is ready to carry current. In the second interval, the gate voltage is rising from V_{TH} to the Miller plateau level, $V_{GS,Miller}$. This is the linear operation of the device when the current is proportional to the gate voltage. On the gate side, the current is flowing into the C_{GS} and C_{GD} capacitors, just like in the first time interval and the V_{GS} voltage is increasing. On the output side of the device, the drain current is increasing, while the drain-to-source voltage keeps at the previous level. Qgs is the required charge when the gate voltage rises from 0 to $V_{GS,Miller}$. This interval time depends on the C_{ISS}. Switching loss is produced during this interval and the value is the area that voltage and current overlap. Normally, the voltage and current depends on external conditions. So to reduce switching loss largely, use a smaller C_{RSS} and Qgd MOSFET.

Entering into the third interval of the turnon procedure, the gate is charged to the sufficient voltage $V_{GS,Miller}$ to carry the entire load current. That now allows the drain voltage to fall. While the drain voltage falls across the device, the gate-to-source voltage stays steady. This is the Miller plateau region in the gate voltage waveform. All the gate current available from the driver is diverted to discharge the C_{GD} capacitor to facilitate the rapid voltage change across the drain-to-source terminals. The drain current of the device stays constant since it is now limited by the external circuitry, that is, the DC current source. C_{RSS} and Qgd are the main influences on this interval. Switching loss is also produced in this interval.

The last step of the turnon is to fully enhance the conducting channel of the MOSFET by applying a higher gate drive voltage. The final amplitude of V_{GS} determines the ultimate on-resistance of the device during its on-time. Therefore, in this fourth interval, V_{GS} is increased from $V_{GS,Miller}$ to its final value, V_{DRV}. This is accomplished by charging the C_{GS} and C_{GD} capacitors, so the gate current is now split between the two components. While these capacitors are being charged, the drain current is still constant, and the drain-to-source voltage is slightly decreasing as the on resistance of the device is being reduced.

Tr is the rising time which includes last three intervals.

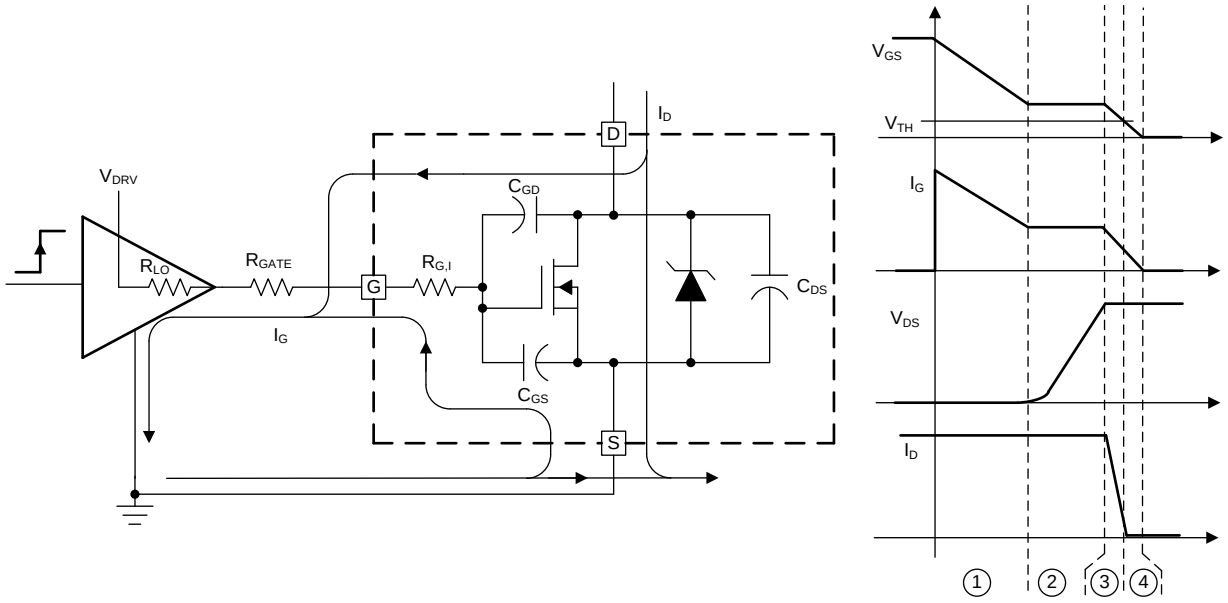


Figure 4. Turnoff Procedure

The description of the turnoff procedure for the MOSFET transistor is basically back tracking the turnon steps from the previous section. Figure 4 shows the turnoff procedure. It is not introduced here in detail. Q_{OSS}, td(off), and tf indicate the turnoff parameters.

3 Controller IC

3.1 IC Driver Resistance

In the *Ultra-Low Quiescent (ULQ) Dual Synchronous Step-Down Controller with 5 V and 3.3 V LDOs Data Sheet* EC table, the high-side MOSFET driver and low-side MOSFET driver resistance are showed as Figure 5, along with test conditions. Driver resistance indicates the driver capability.

MOSFET DRIVERS				
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –50 mA, (V_{VBST} – V_{SW}) = 5 V	3	Ω
		Sink, I_{DRVH} = 50 mA, (V_{VBST} – V_{SW}) = 5 V	1.9	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –50 mA, V_{VREG5} = 5 V	3	Ω
		Sink, I_{DRVL} = 50 mA, V_{VREG5}= 5 V	0.9	

Figure 5. Driver Resistance

A crude estimate of the gate rising time can be calculated using simplified linear approximations of the gate drive current. The gate drive current can be determined using the below equation when MOSFET turns on. Equation 4 shows the gate current in procedure 1. Equation 5 is the gate current in procedure 2. Equation 6 is the gate current in procedure 3, and Equation 7 is the gate current in procedure 4. In the following equation, I_G is the gate current. V_{DRV} is drive voltage. R_{gate} is total drive resistance. It includes IC drive resistance, MOSFET internal gate resistance and gate resistance of PCB board.

$$I_{G1} = \frac{V_{DRV} - 0.5 \times V_{TH}}{R_{gate}} \tag{4}$$

$$I_{G2} = \frac{V_{DRV} - 0.5 \times (V_{TH} + V_{GS,Miller})}{R_{gate}} \tag{5}$$

$$I_{G3} = \frac{V_{DRV} - V_{GS,Miller}}{R_{gate}} \tag{6}$$

$$I_{G4} = \frac{V_{DRV} - 0.5 \times (V_{DRV} + V_{GS,Miller})}{R_{gate}} \tag{7}$$

Assuming that I_{G1} charges the input capacitor of the MOSFET from 0 to V_{TH}, use Equation 8 to calculate the charging time. I_{G2} charges the input capacitor of MOSFET from V_{TH} to $V_{GS,Miller}$. Equation 9 shows this period charging time. I_{G3} is the discharge current of the C_{RSS} capacitor while the drain voltage changes from V_{DS} to 0. Equation 10 shows the discharging time. I_{G4} charges input capacitor of MOSFET from $V_{GS,Miller}$ to V_{DRV}. Equation 11 shows the charging time.

$$t_1 = C_{ISS} \times \frac{V_{TH}}{I_{G1}} \tag{8}$$

$$t_2 = C_{ISS} \times \frac{V_{GS,Miller} - V_{TH}}{I_{G2}} \tag{9}$$

$$t_3 = C_{RSS} \times \frac{V_{DS}}{I_{G3}} \tag{10}$$

$$t_4 = C_{ISS} \times \frac{V_{DRV} - V_{GS,Miller}}{I_{G4}} \tag{11}$$

From the previous equation, the gate rising time depends on drive voltage, total gate resistance, and many MOSFET parameters. If a faster gate rising time is requested, it is better to use the MOSFET of the smaller C_{ISS}, C_{RSS}, and smaller gate resistance. If you use it the same way, gate falling time also can be estimated.

Switching loss of MOSFET is produced during period 2 and 3. During t_2, the drain voltage is V_{DS} and the current is ramping from 0 to I_D. Again, using linear approximations of the waveforms, the power loss of MSOFET for this period can be estimated from Equation 12. In the below equation, T is the switching period. During the time t_3, the drain voltage is falling from V_{DS} to near 0 V. Equation 13 shows how to calculate the power loss.

$$P_2 = \frac{t_2}{T} \times V_{DS} \times \frac{I_D}{2} \tag{12}$$

$$P_3 = \frac{t_3}{T} \times \frac{V_{DS}}{2} \times I_D \tag{13}$$

Calculating the exact switching losses is almost impossible. The reason is the effect of the parasitic inductive components significantly alters the current and voltage waveforms, as well as the switching times during the switching procedures. Taking into account the effect of the different source and drain inductances of a real circuit results in second order differential equations to describe the actual waveforms of the circuit. Since the variables, including gate threshold voltage, MOSFET capacitor values, and driver output impedances, have a very wide tolerance, the above described linear approximation seems to be a reasonable enough compromise to estimate gate rising time and switching losses in the MOSFET.

3.2 Bootstrap Circuit

Figure 6 shows the bootstrap circuit of the IC. Normally, there is a 5 V LDO power supply to charge the external cap, so the BST PIN voltage is higher 5 V than SW PIN that also connects with high-side MOSFET source terminal. When the current goes through from bootstrap cap to high-side MOSFET gate, high-side MOSFET turns on. When the current goes through from high-side gate to SW, high-side MOSFET turns off. During the time of high-side MOSFET turning off, 5 V LDO can charge the bootstrap cap.

The Bootstrap resister influences switching rising slew rate. If the resister is larger, the current of charging high-side MOSFET gate is smaller, so the slew rate of switching rising is slower. At the same time, the switching loss is larger and efficiency is lower. The advantage is that SW overshoot voltage decreases and EMI noise is small.

The bootstrap cap is used to turn on high-side MOSFET and maintain it on. If the cap is too small, it cannot maintain enough time for high-side MOSFET on. It can happen to the BST under voltage protection. If the cap is too large, it needs a long time to charge the cap. Normally, a 0.1 µF cap is enough for TPS512XX family parts.

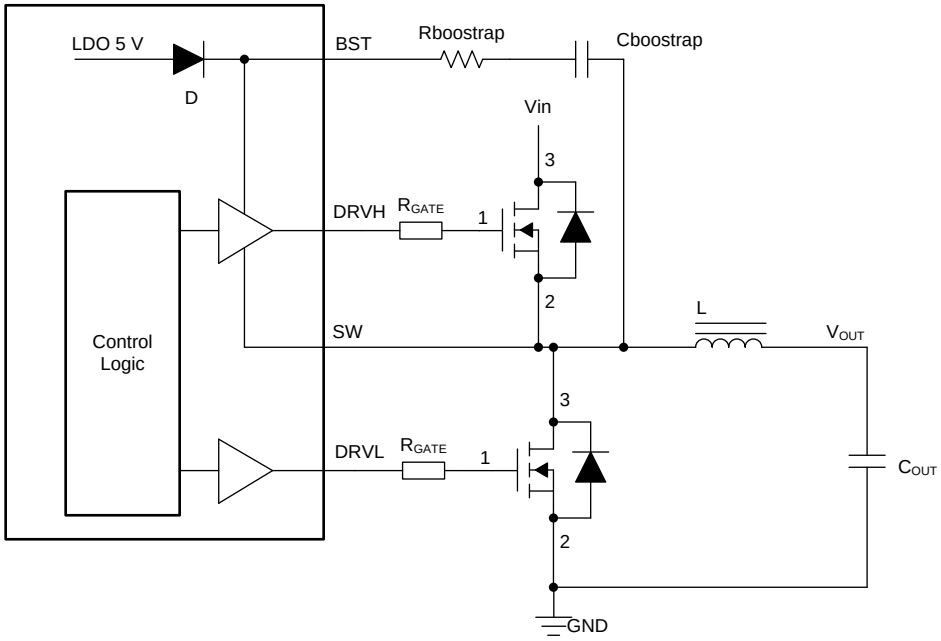


Figure 6. Bootstrap Circuit

4 Adjust Driver Parameters

In theory, the quickest slew rate of switching is the best, because the switching loss is the lowest. It can cause larger switching over voltage and EMI noise. So the driver parameters must be adjusted to guarantee the safety of the MOSFET. The best solution, under the premise of ensuring safety, is that the slew rate of switching must be as fast as it can.

The following waveforms are tested based on TPS51285B with CSD87330Q3D. The information of other parts is available for reference of the *Dual Synchronous Step-Down Fixed Output Controller with 5-V and 3.3-V LDOs User's Guide*. In the following waveforms, channel 1 is the high-side MOSFET gate to GND. Channel 2 is the low-side MOSFET gate to GND. Channel 3 is the SW waveform. Channel M is the high-side MOSFET gate to high-side MOSFET source voltage. The input voltage is 12 V, the output voltage is 3.3 V, and the output current is 5 A.

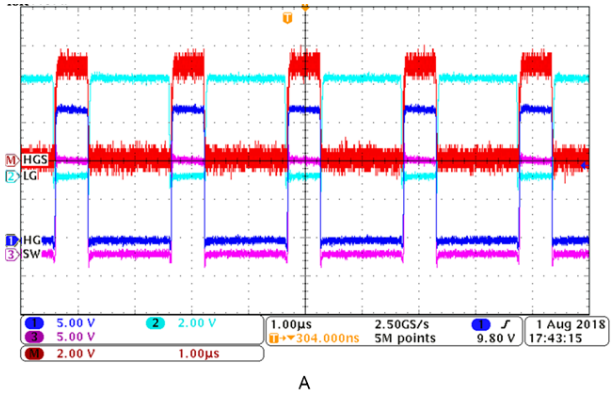


Figure 0. UNDEFINED

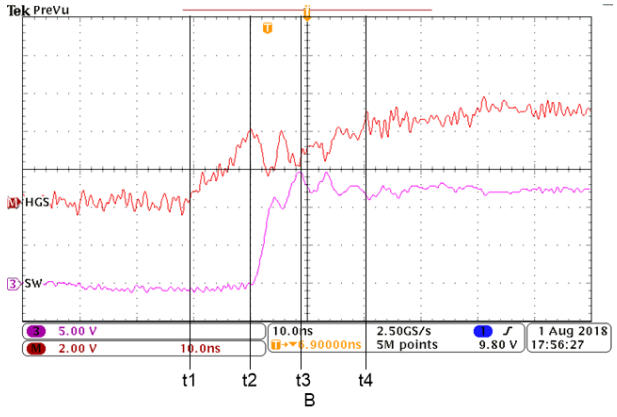


Figure 0. UNDEFINED

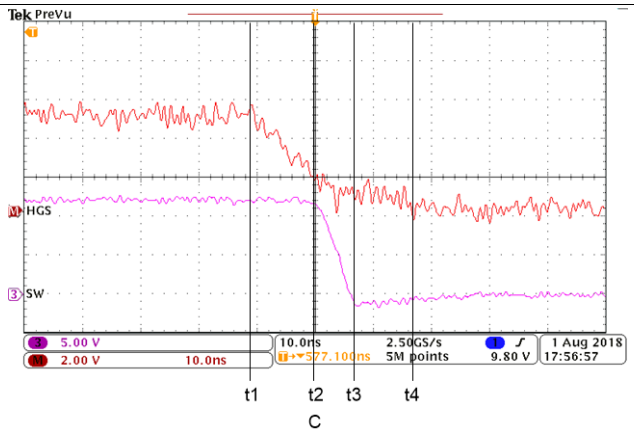


Figure 7. TPS51285B Switching Waveform

In waveform (B), t1~t2 is the time that gate voltage rises from 0 V to $V_{GS,Miller}$. t2~t3 is the time that gate voltage keeps in the Miller plateau, which lasts about 8 ns. At the time of t3, SW voltage has got to the max voltage, and Cgd has been charged. From t3, gate voltage still goes up to 5 V. Switching rising time is about 8 ns, which is same with the Miller plateau time. The switching overshoot voltage is 15 V. The slew rate of switching rising is about 2 V/ns. In waveform (C), t1~t2 is turnoff delay time. t2~t3 is the Miller plateau which lasts about 8 ns. From t3, V_{gs} continues to decrease to 0.

Driver parameters of the controller IC include bootstrap resister, bootstrap cap, and gate resister. See Figure 6 for a reference. For the bootstrap cap, as discussed above, 0.1 µF is enough.

When the low-side MOSFET turns on, the SW voltage is nearly 0 V. When the low-side MOSFET turns off, the SW voltage is about -0.7 V. At the procedure of low-side MOSFET turning on or off, SW voltage does not change too much and does not produce large overshoot or undershoot. For a low-side MOSFET, the slew rate of switching must be as fast as it can. Normally, low-side gate resister is not required. The low-side MOSFET gate resister is set as 0 Ω.

Next, the high-side MOSFET gate resister has an effect on switching rising and falling. The bootstrap resister only affects switching rising. The high-side MOSFET gate resister must be firstly confirmed depending on switching falling and undershoot, then bootstrap resister can be confirmed by switching rising and overshoot.

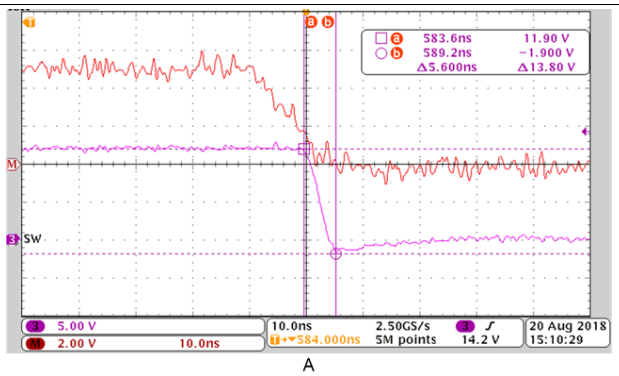


Figure 0. UNDEFINED

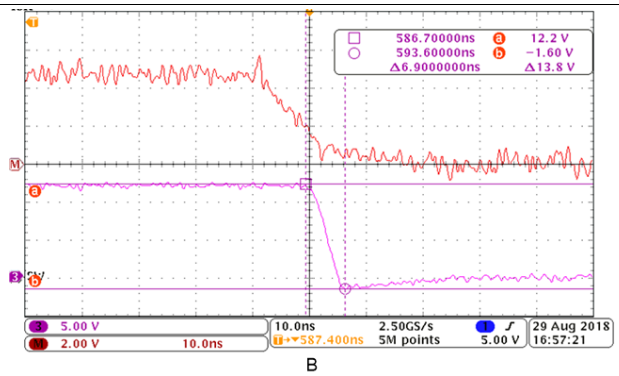
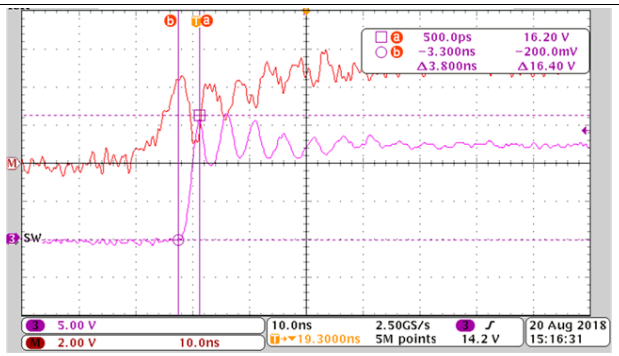


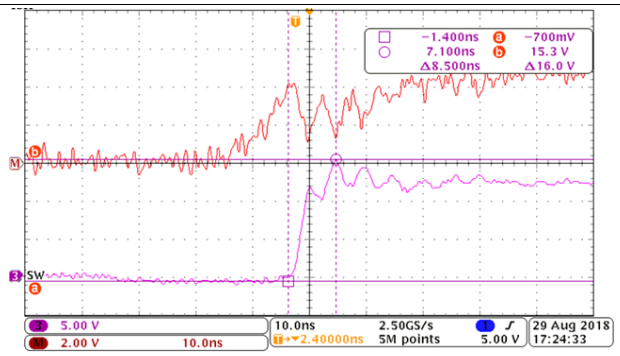
Figure 8. The Falling of Switching

Figure 8 shows the tested waveform with different gate resister. In waveform (A), the bootstrap resister and gate resistor are 0 Ω. The SW falling time is about 5.6 ns, and SW undershoot voltage is -1.9 V. The slew rate of falling is about 2.52 V/ns. The efficiency is 93.8%. In waveform (B), the bootstrap resister is 0 Ω, and the gate resister is 4.7 Ω. The SW falling time is about 6.9 ns and SW undershoot voltage is -1.6 V. The slew rate is about 2 V/ns, and the efficiency is 93.7%. For the TPS51285B, the switching slew rate is best when below 2 V/ns. The high-side MOSFET gate resister is set as 4.7 Ω.



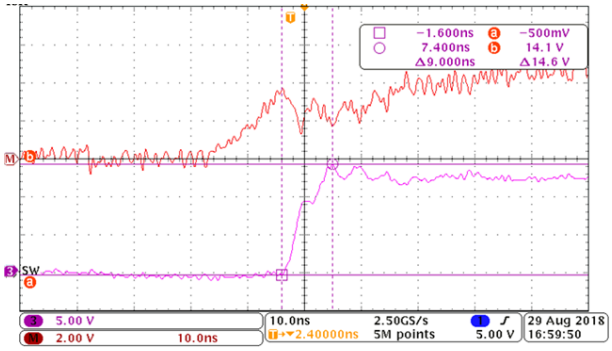
A

Figure 0. UNDEFINED



B

Figure 0. UNDEFINED



C

Figure 9. The Rising of Switching

In Figure 9, the gate resister is always 4.7 Ω and does not change. The bootstrap resister is 4.7 Ω in waveform (A), 10 Ω in waveform (B), and 15 Ω in waveform (C). In waveform (A), SW overshoot voltage is the biggest at 16.2 V. The slew rate of SW rising is about 4.31 V/ns. The efficiency is 93.7%. In waveform (B), SW overshoot voltage is about 15.3 V and slew rate is about 1.88 V/ns. The efficiency is about 93.6%. In waveform (C), the SW overshoot voltage is about 14.1 V and slew rate is about 1.6 V/ns. The efficiency is about 93.4%. Comparing the three waveforms, a 10 Ω bootstrap resister is better.

Use different types of MOSFET and a smaller Qg MOSFET. The driver parameters must be adjusted depending on the MOSFET you use. The key factor is to adjust switching slew rate and SW overshoot to guarantee the safety of IC and MOSFET and efficiency as high as it can.

5 Summary

This application report mainly introduces how to adjust driver parameters depending on MOSFET about TPS512xx IC. It does not need a low-side gate resistor to get faster switching of the low-side MOSFET turning on or off. The gate resister of high-side MOSFET is confirmed by the falling of switching, then the bootstrap resistor is confirmed by the rising of switching.

6 References

- Texas Instruments, *Ultra-Low Quiescent (ULQ) Dual Synchronous Step-Down Controller with 5 V and 3.3 V LDOs Data Sheet*
- Texas Instruments, *Dual Synchronous Step-Down Fixed Output Controller with 5-V and 3.3-V LDOs User's Guide*
- Texas Instruments, *Fundamentals of MOSFET and IGBT Gate Driver Circuits Seminar*
- Texas Instruments, *CSD87330Q3D Synchronous Buck NexFET Power Block Data Sheet*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2018) to A Revision	Page
• Edited application report for clarity.	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265