Architecture for Brushless-DC Gate Drive Systems

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ABSTRACT

Brushless-DC motor drive systems can take on a number of different possible architectures ranging from low-end sensored trapezoidal control to high-end sensorless field oriented control (FOC). A different architecture may have different care-abouts in terms of system implementation involving current sense amplifiers, power management, and diagnostics. The DRV832x and DRV835x family allows designers to choose devices that can closely meet architecture requirements while including the optimal features.

Related Products: DRV8320   DRV8320R   DRV8323   DRV8323R

DRV8350   DRV8350R   DRV8353   DRV8353R

Contents

Trademarks

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1   Current Sense Amplifiers

Current sense amplifiers are used to measure the motor current, either the total motor current through the use of a single sense amplifier or the individual phase currents using two or three sense amplifiers (using two sense amplifiers requires calculation of the third phase current in the microcontroller).

In low end systems, the most basic use of a single current sense amplifier is to provide system protection: if there is a short across the windings of the motor or the motor current becomes too large, the microcontroller (MCU) can detect the abnormal current and shut down the system. A single current shunt amplifier can also be used to regulate the motor current while running a trapezoidal commutation (6-step).

Two or three current sense amplifiers will be used in Field Oriented Control (FOC) solutions, since in order to properly drive each phase the microcontroller needs to measure each phase current. Additionally, any system that implements a completely sensorless control scheme requires accurate current monitoring of each motor phase in order to properly estimate the rotor position. In very-high-end systems, current can be measured in-line with the motor instead of using traditional low-side current shunt amplifiers.

2   Power Management

System power management varies widely from system to system depending on the MCU used, peripheral features, Hall-Effect sensors (or absence), system voltage, and target system efficiency.

A low-end brushless-DC system may implement a very low power MCU running a basic trapezoidal commutation algorithm. These simple MCU's may only require 10 mA to operate, with other circuits on the board (including Hall-Effect sensors) consuming an additional 10-20mA. For this low power consumption, a simple LDO from the system supply voltage down to 5.0V or 3.3V will be a cost effective solution. However if a key system parameter is power consumption or heat generation, customers may opt to design a DC/DC regulator instead of an LDO in order to minimize power dissipation and maximize power conversion efficiency.

High-end brushless-DC systems may require much higher end MCUs or even processors, especially when implementing sensorless or FOC solutions. In these cases much more current is consumed by the controller and additional circuitry, potentially exceeding hundreds of mA. For these high currents LDOs become ineffective due to the high power consumption and low efficiency, so a DC/DC regulator is often implemented to generate the required 5.0V or 3.3V.

3 Serial Interface

A third feature of brushless-DC systems is the interface between the system controller and the driver. While the control of the PWM is a given in almost every system, there is an additional level of interface. Some systems require no configuration or diagnostic features. Other systems implement on-the-fly configuration of the operation or fault diagnostics to get a detailed look at a problem if it occurs.

The most discrete implementation of a brushless-DC motor system uses three 1/2-H gate drivers. No configuration is required from the microcontroller and all settings are designed in the hardware of the board. For example, the gate drive current is set using series resistors to limit the current. This solution requires very little from the system controller other than PWM outputs to drive the motor. Even in more integrated motor gate drivers, the requirment of simple configuration is common in order to use a low-end microcontroller. Even though features like protection or gate drive current adjustability may be integrated into the driver, many customers look for a simple way to configure these settings in the schematic.

A brushless-DC system that emphasizes configurability and diagnostics may opt for a motor drive solution that has a serial interface, like SPI. A serial interface unlocks access to settings that would require far too many pins to implement in a hardware interface. The serial interface will typically have a wider variety of configuration options available. Additionally, a serial interface allows much more information to be collected about the state of the driver, particularly in fault conditions. A hardware interface, while very simple, will at most offer one pin to indicate that a fault has occurred.

4 DRV832x and DRV835x Family Introduction

The DRV832x and DRV835x family of Smart Gate Drivers include several variants integrating optional sense amplifiers, DC/DC buck regulator and SPI interface. The packages for this family are QFN-type, ranging from 5x5 mm and 32 pins to 7x7 mm and 48 pins.
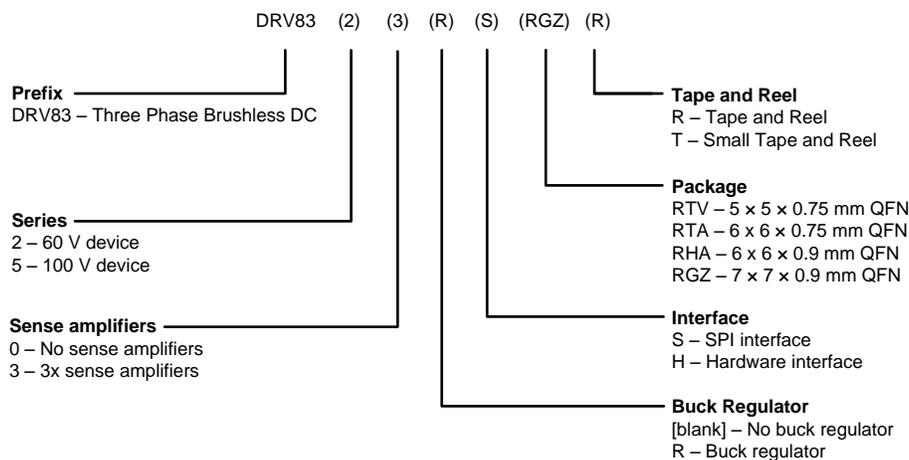
DRV83 (2) (3) (R) (S) (RGZ) (R)
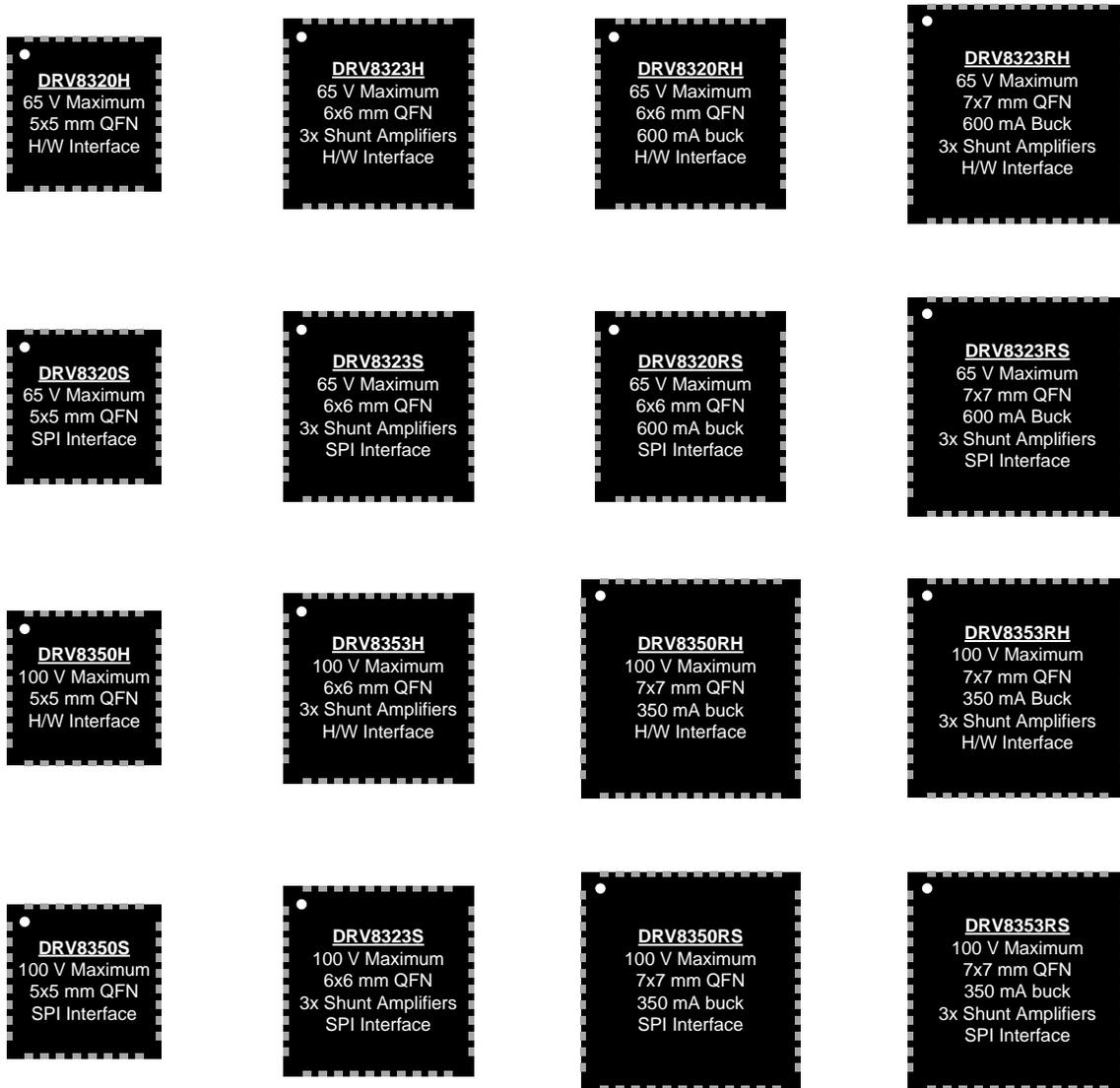
Prefix
DRV83 – Three Phase Brushless DC

Series
2 – 60 V device
5 – 100 V device

Sense amplifiers
0 – No sense amplifiers
3 – 3x sense amplifiers

Tape and Reel
R – Tape and Reel
T – Small Tape and Reel

Package
RTV – 5 × 5 × 0.75 mm QFN
RTA – 6 × 6 × 0.75 mm QFN
RHA – 6 × 6 × 0.9 mm QFN
RGZ – 7 × 7 × 0.9 mm QFN

Interface
S – SPI interface
H – Hardware interface

Buck Regulator
[blank] – No buck regulator
R – Buck regulator

Figure 1. Device Nomenclature

DRV8320H
65 V Maximum
5x5 mm QFN
H/W Interface

DRV8323H
65 V Maximum
6x6 mm QFN
3x Shunt Amplifiers
H/W Interface

DRV8320RH
65 V Maximum
6x6 mm QFN
600 mA buck
H/W Interface

DRV8323RH
65 V Maximum
7x7 mm QFN
600 mA Buck
3x Shunt Amplifiers
H/W Interface

DRV8320S
65 V Maximum
5x5 mm QFN
SPI Interface

DRV8323S
65 V Maximum
6x6 mm QFN
3x Shunt Amplifiers
SPI Interface

DRV8320RS
65 V Maximum
6x6 mm QFN
600 mA buck
SPI Interface

DRV8323RS
65 V Maximum
7x7 mm QFN
600 mA Buck
3x Shunt Amplifiers
SPI Interface

DRV8350H
100 V Maximum
5x5 mm QFN
H/W Interface

DRV8353H
100 V Maximum
6x6 mm QFN
3x Shunt Amplifiers
H/W Interface

DRV8350RH
100 V Maximum
7x7 mm QFN
350 mA buck
H/W Interface

DRV8353RH
100 V Maximum
7x7 mm QFN
350 mA Buck
3x Shunt Amplifiers
H/W Interface

DRV8350S
100 V Maximum
5x5 mm QFN
SPI Interface

DRV8323S
100 V Maximum
6x6 mm QFN
3x Shunt Amplifiers
SPI Interface

DRV8350RS
100 V Maximum
7x7 mm QFN
350 mA buck
SPI Interface

DRV8353RS
100 V Maximum
7x7 mm QFN
350 mA buck
3x Shunt Amplifiers
SPI Interface

Figure 2. Device Options

Table 1. Feature Comparison

Device Max Voltage	Generic Part Number	Current Sense Amplifiers	DC/DC Buck Regulator	Package	Interface	Orderable Part Number
65V	DRV8320	None	None	5x5mm, 32 pins, 0.75mm height, 0.5 mm pitch	Hardware	DRV8320HRTVR DRV8320HRTVT
					SPI	DRV8320SRTVR DRV8320SRTVT
	DRV8323	Three	None	6x6mm, 40 pins, 0.75mm height, 0.5 mm pitch	Hardware	DRV8323HRTAR DRV8323HRTAT
					SPI	DRV8323SRTAR DRV8323SRTAT
	DRV8320R	None	0.8-60V, 600mA LMR16006X	6x6mm, 40 pins, 0.9mm height, 0.5 mm pitch	Hardware	DRV8320RHRHAR DRV8320RHRHAT
					SPI	DRV8320RSRHAR DRV8320RSRHAT
	DRV8323R	Three	0.8-60V, 600mA LMR16006X	7x7mm, 48 pins, 0.9mm height, 0.5 mm pitch	Hardware	DRV8323RHRGZR DRV8323RHRGZT
					SPI	DRV8323RSRGZR DRV8323RSRGZT
100V	DRV8350	None	None	5x5mm, 32 pins, 0.75mm height, 0.5 mm pitch	Hardware	DRV8350HRTVR DRV8350HRTVT
					SPI	DRV8350SRTVR DRV8350SRTVT
	DRV8353	Three	None	6x6mm, 40 pins, 0.75mm height, 0.5 mm pitch	Hardware	DRV8353HRTAR DRV8353HRTAT
					SPI	DRV8353SRTAR DRV8353SRTAT
	DRV8350R	None	2.5-75V, 350mA LM5008A	7x7mm, 48 pins, 0.9mm height, 0.5 mm pitch	Hardware	DRV8350RHRGZR DRV8350RHRGZT
					SPI	DRV8350RSRGZR DRV8350RSRGZT
	DRV8353R	Three	2.5-75V, 350mA LM5008A	7x7mm, 48 pins, 0.9mm height, 0.5 mm pitch	Hardware	DRV8353RHRGZR DRV8353RHRGZT
					SPI	DRV8353RSRGZR DRV8353RSRGZT

5   Current Sense Amplifiers Options

Devices in the DRV832x and DRV835x families are available either with zero or three current shunt amplifiers. These amplifiers are used for low-side current shunt measurement and have adjustable gain between 5, 10, 20, and 40 V/V. These amplifiers are bidirectional and can measure positive and negative currents.

A unidirectional mode for the amplifier is available on devices with the SPI interface. In this mode the amplifier will only measure positive current through the half-bridge (current flowing through the sense resistor into GND).

A VDS Current Sense mode is also available on devices with the SPI interface. VDS Current Sense mode internally routes the sense amplifier inputs across the low-side external MOSFET. This allows measurement of the motor current without needing a sense resistor, however for accurate systems this requires some knowledge about the external MOSFET $R_{DS(ON)}$ as well as variation over temperature.

Figure 3. Bidirectional Current Sense Configuration

Figure 4. Resistor Sense Configuration

Figure 5. V$_{DS}$ Current Sense Mode

6 DC/DC Buck Regulator Options

Devices in the DRV832x and DRV835x family are available with or without a DC/DC buck regulator. This DC/DC buck regulator requires external components to operate, including an external inductor, schottky diode, bulk capacitance, and other passives.

This regulator found in the DRV832x family is functionally the same as LMR16006X. The DC/DC regulator can support 0.8-60V output with current up to 600mA. The DRV835x family regulator is functionally equivalent to the LM5008A, which can support 2.5-75V output with current up to 350mA.

The DC/DC buck regulator can be enabled or disabled independently from the gate driver portion of the device, which allows it to be used even when the gate driver is in sleep mode. For additional details on the specifications of these regulators, including design information, refer to the *LMR16006* data sheet or the *LM5008A* data sheet
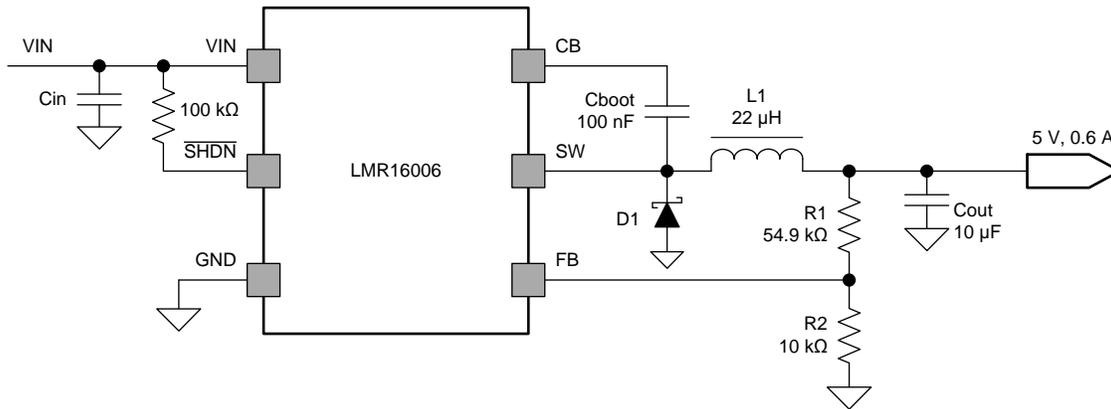
Figure 6. Application Circuit with 5-V Output DC/DC the LMR16006

7 Interface Options

All DRV832x and DRV835x devices support 6x/3x/1x & Independent PWM modes to drive the motor; however there are two interface options available for configuration of the device settings.

The Hardware (H/W) Interface allows the user simple configuration of the device for the easiest use. The H/W interface allows configuration of key parameters (Gate drive current, VDS Monitor Threshold, PWM Mode, & Sense Amplifier Gain) using a resistor on a pin (IDRIVE, VDS, MODE, GAIN).

The SPI Interface is a serial interface allowing reading and writing of device registers. This interface allows more configuration options as well as fault diagnostics.

Table 2. Settings Available on DRV832x and DRV835x

Configuration Setting	H/W Interface	H/W Pin	SPI Interface	SPI Register
Fault Report	nFAULT pin		nFAULT pin, diagnostics available through SPI	Fault Status 1 (0x0h), VGS Status 1 (0x1h)
Overcurrent effect	**DRV832x**: all three half-bridges can be shutdown in response to VDS_OCP and SEN_OCP, **DRV835x**: only associated half-bridge is shutdown		**DRV832x**: all three half-bridges can be shutdown in response to VDS_OCP and SEN_OCP, **DRV835x**: only associated half-bridge or all three half-bridges can be shutdown	**DRV832x**: No setting available, **DRV835x**: OCP_ACT (0x2h bit 10)
Charge Pump and Gate Drive Undervoltage	**DRV832x**: Charge pump undervoltage enabled, **DRV835x**: Charge pump and low-side gate drive undervoltage enabled		**DRV832x**: Charge pump undervoltage enabled or disabled, **DRV835x**: Charge pump and low-side gate drive undervoltage enabled or disabled	**DRV832x**: DIS_CPUV (0x2h bit 9) **DRV835x**: DIS_GDUV (0x2h bit 9)
Gate Drive Fault	Enabled		Enabled or disabled	DIS_GDF (0x2h bit 8)
Overtemperature Warning	Not Available		Enabled or disabled	OTW_REP (0x2h bit 7)

Table 2. Settings Available on DRV832x and DRV835x (continued)

Configuration Setting	H/W Interface	H/W Pin	SPI Interface	SPI Register
PWM Mode	6x, 3x, 1x PWM or independent PWM	MODE	6x, 3x, 1x PWM or independent PWM	PWM_MODE (0x2h bits 5-6)
1x PWM Conduction Mode	Synchronous		Synchronous or Asynchronous	1PWM_COM (0x2h bit 4)
Gate Drive Current (IDRIVE)	Up to 1A with 7 settings, sink set to 2x source	IDRIVE	Up to 1A with 16 settings, sink and source can be configured independently, High-side and low-side FET can be configured independently	IDRIVEP_HS (0x3h bits 4-7), IDRIVEN_HS (0x3h bits 0-3), IDRIVEP_LS (0x4h bits 4-7), IDRIVEN_LS (0x4h bits 0-3)
Gate Drive Time (TDRIVE)	4 us		500 ns to 4 μs with 4 settings	TDRIVE (0x4h bits 8-9)
Cycle-By-Cycle Fault Response	Enabled		Enabled or disabled	CBC (0x4h bit 10)
Fault Retry Time	**DRV832x**: 4 ms, **DRV835x**: 8 ms		**DRV832x**: 4 ms or 50 μs , **DRV835x**: 8 ms or 50 μs	TRETRY (0x5h bit 10)
Dead Time	100 ns		50 ns to 400 ns with 4 settings	TDEAD (0x5h bits 8-9)
OCP Response Mode	Automatic retry		Latch off, automatic retry, report only, or ignore	OCP_MODE (0x5h bits 6-7)
OCP Deglitch Time	4 μs		2 μs to 8 μs with 4 settings	OCP_DEG (0x5h bits 4-5)
VDS Overcurrent Threshold	**DRV832x**: 0.06 V to 1.88 V with 6 settings & disable option, **DRV835x**: 0.06 V to 2 V with 6 settings & disable option	VDS	**DRV832x**: 0.06 V to 1.88 V with 16 settings (disable available through OCP_MODE), **DRV835x**: 0.06 V to 2 V with 16 settings (disable available through OCP_MODE)	VDS_LVL (0x5h bits 0-3)

Table 3. Settings Only Available on DRV8323, DRV8353, DRV8323R, and DRV8353R (Devices With 3x Current Sense Amplifiers)

Configuration Setting	H/W Interface	H/W Pin	SPI Interface	SPI Register
Current Sense Mode	Standard (measure across low-side sense resistor)		Standard (measure across low-side sense resistor) or VDS (measure across FET drain-source)	CSA_FET (0x6h bit 10)
Sense Amplifier Output Mode	Bidirectional		Bidirectional or Unidirectional	VREF_DIV (0x6h bit 9)
VDS Monitor Low Side Reference	SPx		SPx or SNx	LS_REF (0x6h bit 8)
Sense Amplifier Gain	5, 10, 20, 40 V/V	GAIN	5, 10, 20, 40 V/V	CSA_GAIN (0x6h bits 6-7)
Sense Pin Overcurrent Fault	Enabled		Enabled or Disabled	DIS_SEN (0x6h bits 5)
Sense Amplifier Calibration	One pin used to short all inputs of the Current Sense Amplifiers	CAL	Can calibrate any of the three sense amplifiers independently	CSA_CAL_A, B, C (0x6h bits 2-4)
Sense Pin Overcurrent Threshold	1V		0.25 to 1 V with 4 settings	SEN_LVL (0x6h bits 0-1)

8   References

Refer to these references for additional information:
*   Texas Instruments, *DRV832x 6 to 60-V Three-Phase Smart Gate Driver* data sheet
*   Texas Instruments, *DRV835x 100-V Three-Phase Smart Gate Driver* data sheet
*   Texas Instruments, *LMR16006* data sheet
*   Texas Instruments, *LM5008A* data sheet

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2018) to A Revision **Page**

*   Added the DRV835x family of devices 1