Application Report
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Extracting a Lumped Output Impedance Model With SIMPLIS or SiMetrix

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ABSTRACT

This application report shows how to use the Simplis Technologies SiMetrix™ simulator to extract a lumped output impedance model for the TPS74801 low dropout linear regulator (LDO), and how to use the SIMPLIS™ simulator to extract the output impedance of the TPS62130A buck converter. Both the output impedance characteristic and a lumped output impedance model help signal integrity engineers spot potential problems and validate entire systems in a time-efficient manner.

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1 Introduction

System-level validation engineers are increasingly concerned with the output impedance characteristics of the power supplies on their boards. The output impedance versus frequency characteristic show how the supply behaves when loaded at dc, or with varying transient loads. If the transients have significant frequency content where the output impedance rises, the engineer can pay special attention to testing in that frequency band. Figure 1 shows the output impedance characteristic of an LDO. The magnitude curve (green) shows that there may be some concern if there are transients around 100 kHz where the impedance peaks. Signal integrity engineers often specify a target impedance for each rail that keeps the voltage excursion within specified limits, and an output impedance plot is an easy way to see if there is a problem. One caution is that the results are only as good as the model. Some LDO models are built on a simplified framework and may give poor results. Switching converters have many nonlinear effects that are not always modeled well with a lumped output impedance model; therefore, transient simulation and bench testing is still good design practice for each regulator.

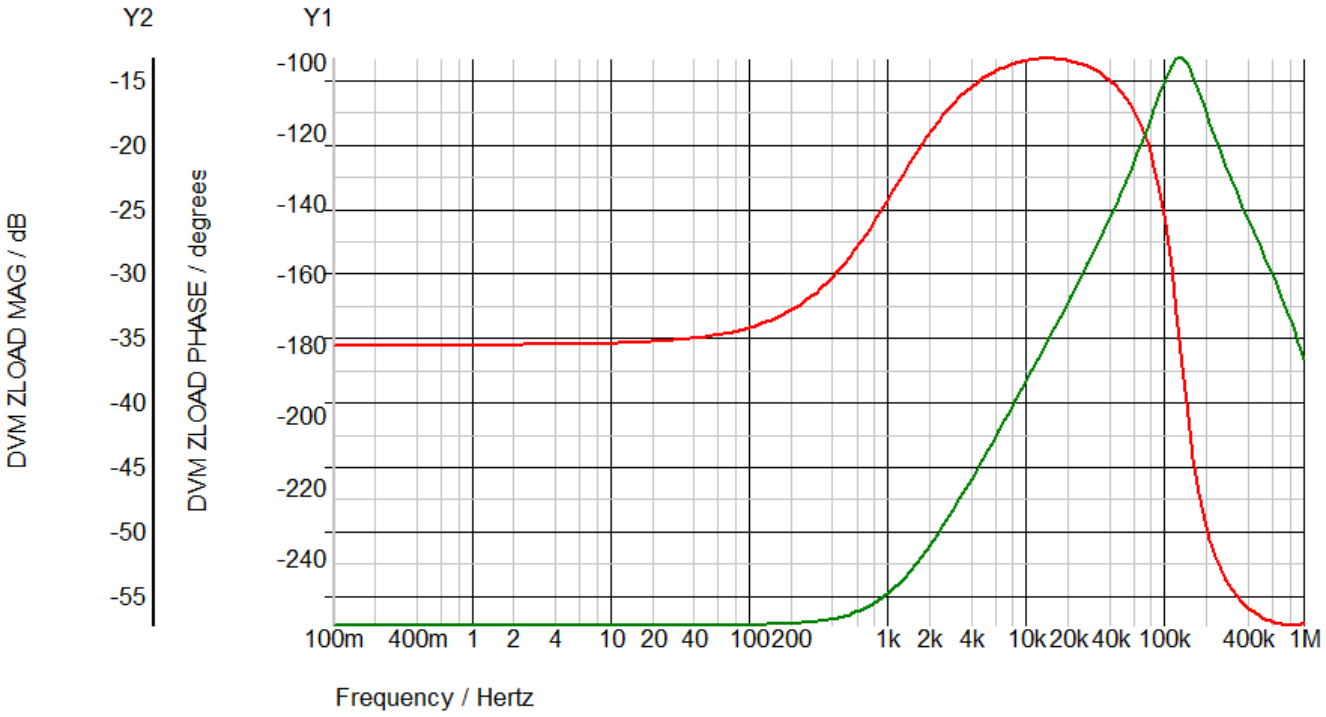

Figure 1. SiMetrix Screen Shot: LDO Output Impedance Simulation Result

Large system boards may have many point-of-load converters, and running system-level simulations with full-switching converter models is time prohibitive. A reasonable compromise is to extract a lumped-element model of the output impedance, and model the power supply as an ideal source in series with the lumped output impedance model. For more accurate results, include any power distribution network characteristics extracted from the board.

2 The Design Verification Module in SiMetrix and SIMPLIS

SiMetrix and SIMPLIS are two circuit simulators developed by SiMetrix Technologies Ltd. The SiMetrix simulator uses a syntax that is similar to PSpice. The SIMPLIS simulator uses a different fast simulation technique with simplified models that enables fast, ac-type analyses on switching transient models. The design verification module (DVM) feature of SiMetrix and SIMPLIS is a very convenient way to run an entire suite of tests on power-converter models. Make use of the output impedance feature of the DVM to allow for quick and easy generation of plots, such as the plot shown in Figure 1.

NOTE: The DVM requires an additional license. The DVM is not available in the basic versions of SiMetrix and SIMPLIS.

3 LDO Example Using SiMetrix

For linear circuits like an LDO, the DVM feature of the SiMetrix simulator works well for extracting output impedance. Switching converters, however, require a SIMPLIS model. The SIMPLIS simulator has features to detect steady-state operation in the switching model in order to determine when to run the analyses, and is described in Section 4.

To simulate the output impedance characteristic for an LDO, first create a simulation schematic using the SiMetrix LDO model. Next, set up the schematic for DVM analysis. A DVM schematic requires familiarity with some new simulation circuit blocks. From the SiMetrix menu, select *DVM → Place → Source → Input Source*. This menu selection allows for placement of the required DVM source that supplies the LDO, as shown in Figure 2.

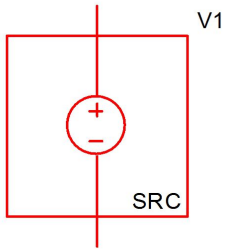

Figure 2. DVM Source Graphic From SiMetrix

Next, select *DVM → Place → Load → 3 Terminal Output Load*. The DVM load symbol shown in Figure 3 is the load for the output of the LDO; notice the third SENSE terminal. The SENSE terminal connects to the top of the feedback divider string. The three-terminal load allows the block to internally add a small resistance from the top of the divider to the output in order to serve as an injection point for the control loop. The DVM runs ac analyses exactly as the measurements are run with real hardware. The open-loop response is then just the output response divided by the sense terminal response. The three-terminal load is not necessary for closed-loop output impedance measurements, but allows for additional tests, such as Bode plots. Start with the three-terminal load to avoid schematic changes if control-loop response simulations are also necessary.

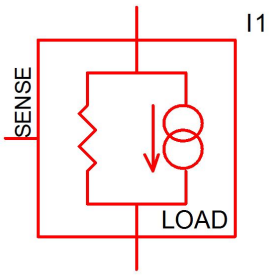

Figure 3. DVM Load Graphic From SiMetrix

Complete the schematic using the source and load symbols from the *DVM* menu. Figure 4 shows an example for the TPS74801.

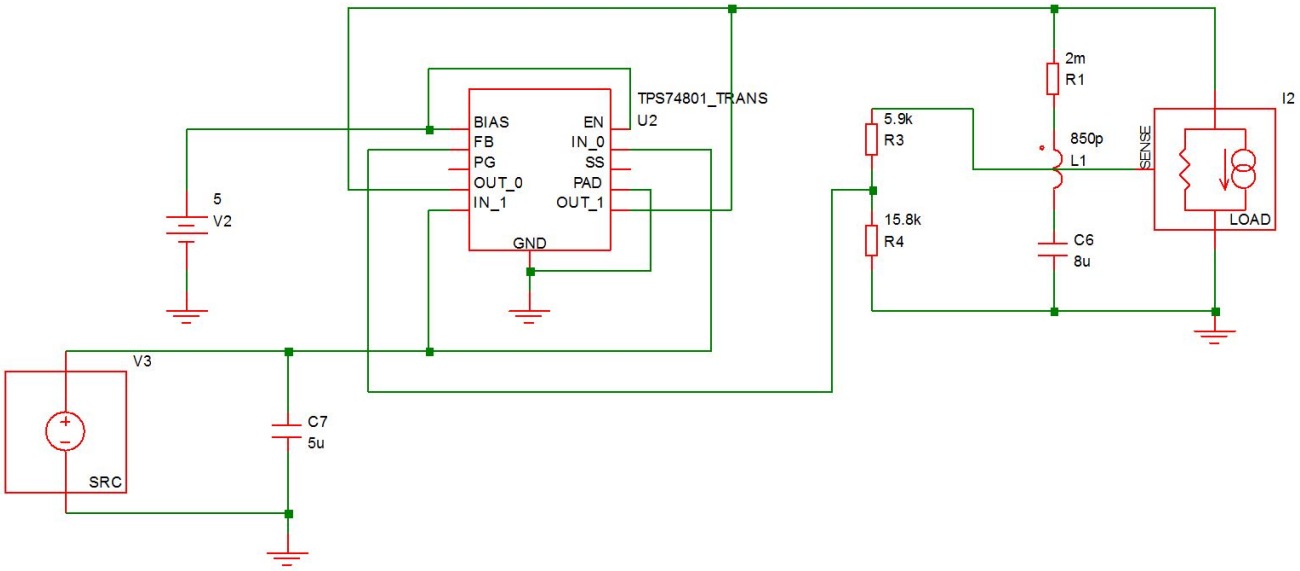

Figure 4. TPS74801 DVM Schematic Screen Capture From Simetrix

To place the DVM control block on the schematic, select *DVM → Place → Control → Full PowerAssist* (Figure 5) from the menu, and double-click on the symbol to set the source voltage, source resistance, output current, and output voltage. Select the frequency range for the impedance sweep on the *Analysis/AC* tab.

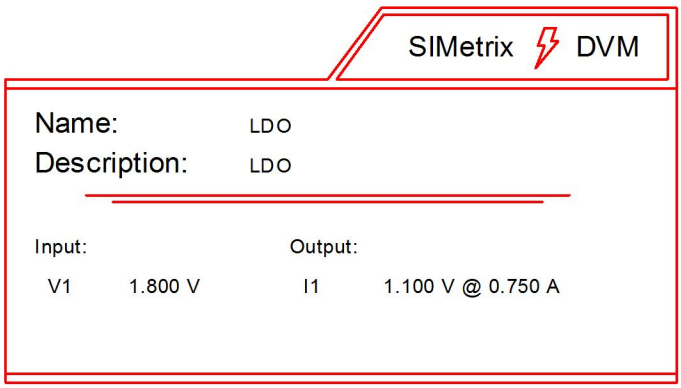

Figure 5. DVM Control Block Graphic From SiMetrix

The DVM uses *.testplan* files to control the tests. Built-in test plans are included for DC/DC converters, but there is no built-in plan for LDOs. The following testplan file defines an output impedance test for LDOs at three different load levels. The testplan file shown here generated the plots shown in this report. Copy the following lines into a text editor, and save the file as *filename*.testplan to use the file as shown.

```
***
*** LDO_OUTPUT_IMPEDANCE.testplan
***
*?@ analysis objective source load label
***
Ac Impedance(OUTPUT:1) "SOURCE(INPUT:1, Nominal)" "LOAD(OUTPUT:1, Light)" Ac Analysis|Output Impedance|Vin Nominal|Light Load
Ac Impedance(OUTPUT:1) "SOURCE(INPUT:1, Nominal)" "LOAD(OUTPUT:1, 50%)" Ac Analysis|Output Impedance|Vin Nominal|50% Load
Ac Impedance(OUTPUT:1) "SOURCE(INPUT:1, Nominal)" "LOAD(OUTPUT:1, 100%)" Ac Analysis|Output Impedance|Vin Nominal|100% Load
```

To run the simulation, select *DVM → Run → Choose Testplan*. Browse to and select the testplan file. Figure 6 shows the dialog box that appears. Select the desired tests to run. For this example, select *Output Impedance* at *Vin Nominal* and *100% Load*. SiMetrix generates a test report and an output impedance vs frequency graph. An example graph is shown in Figure 1

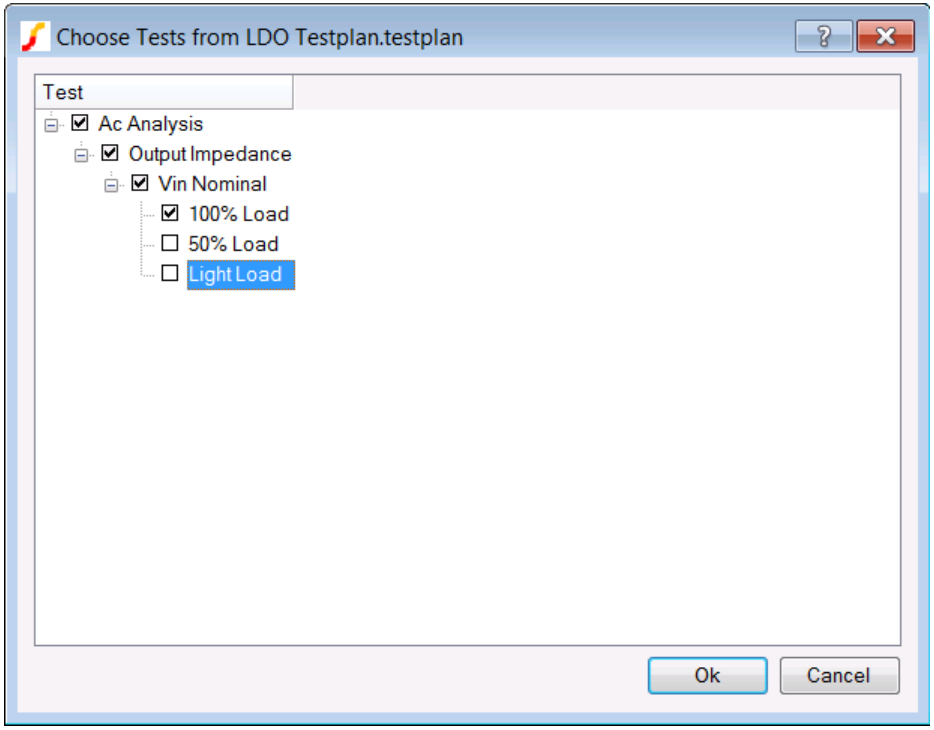

Figure 6. SiMetrix DVM Menu

4 Switching Supply Example Using SIMPLIS

The procedure to run an output impedance simulation on a switching supply model is very similar to the previous LDO example. The input source, output load, and DVM control blocks are identical. Figure 7 shows a simulation schematic for the TPS62130A.

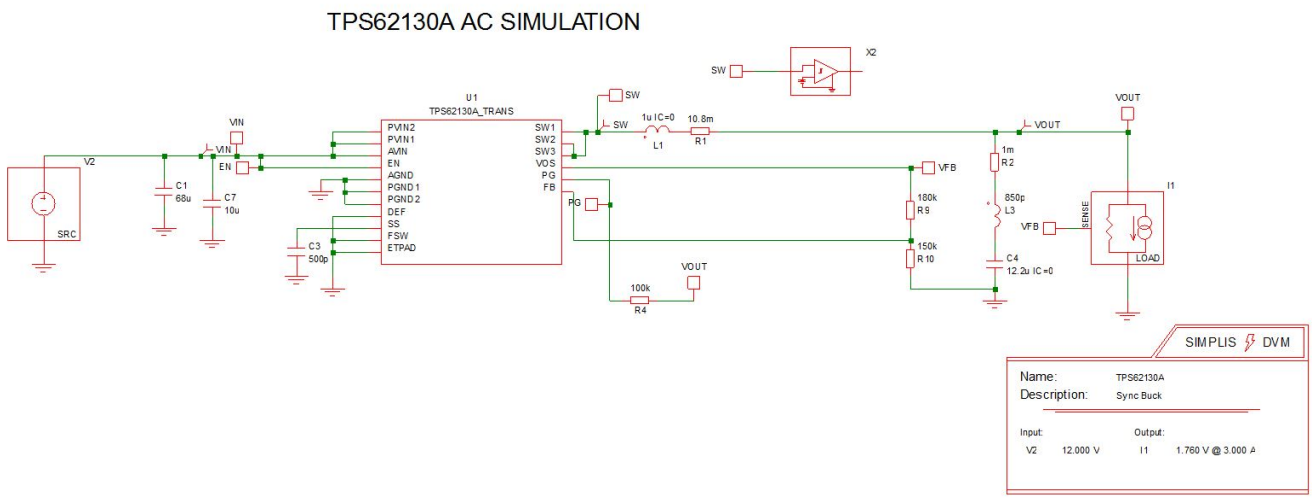

Figure 7. TPS62130A Schematic Screen Capture From SIMPLIS

The two main differences from a linear model, such as the LDO, are the POP control element labeled X2, and the built-in synchronous buck test plan. The POP block helps SIMPLIS detect when the circuit reaches steady-state operation before running the impedance sweep. See Section 7 for details on SIMPLIS documentation. For a simple output impedance measurement, select the built-in testplan, and check the output impedance test as shown in Figure 8. Be sure to check the *Use POP Trigger* box in the *Simulator → Choose Analysis → Periodic Operating Point* tab.

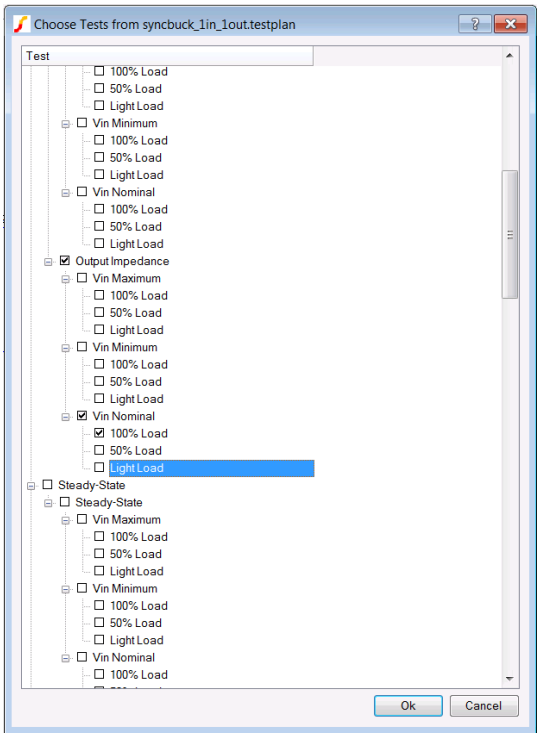

Figure 8. SIMPLIS DVM Menu

Running the analysis results in the output impedance sweep shown in Figure 9.

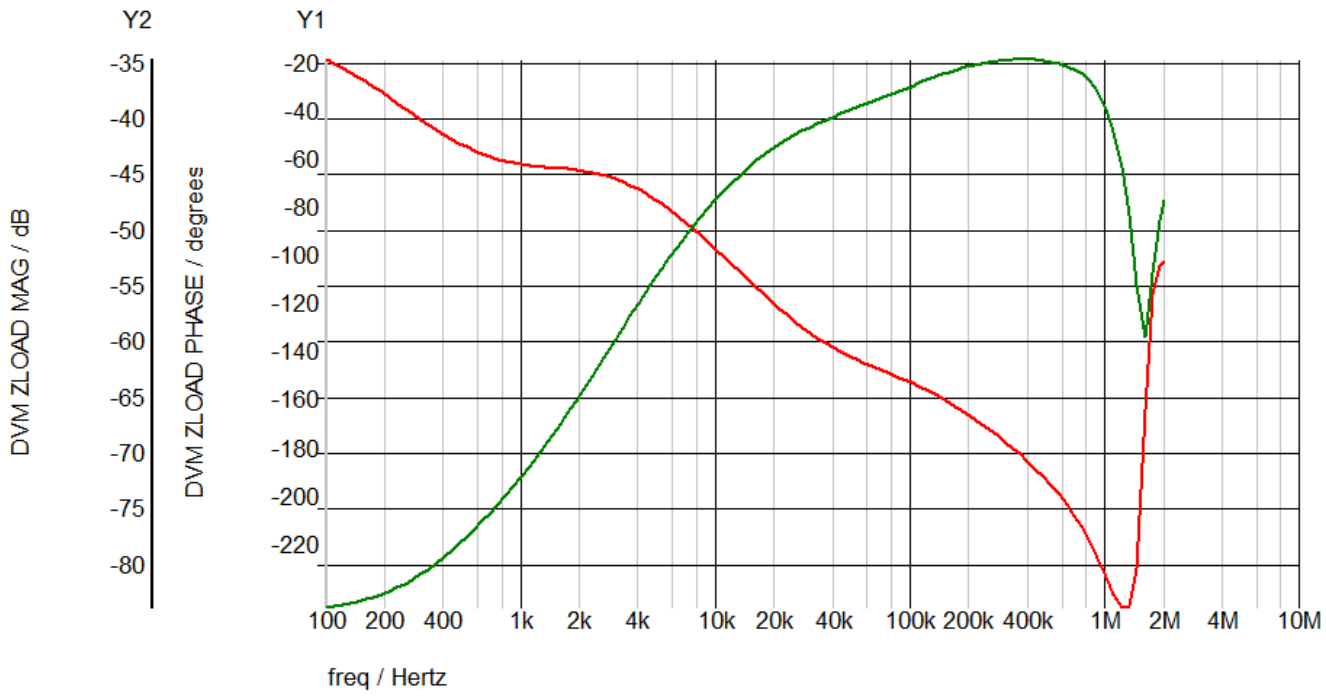

Figure 9. SIMPLIS Screen Shot: TPS62130A Output Impedance Simulation Result

The impedance response is useful, but the goal is to extract a lumped parameter model for the supply.

5 Extracting and Validating the Lumped Parameter Model

To extract a lumped parameter model of the LDO output impedance, examine Figure 10. The low-frequency impedance portion of the green magnitude curve is approximately –57 dBΩ, and is an impedance of 1.36 mΩ.

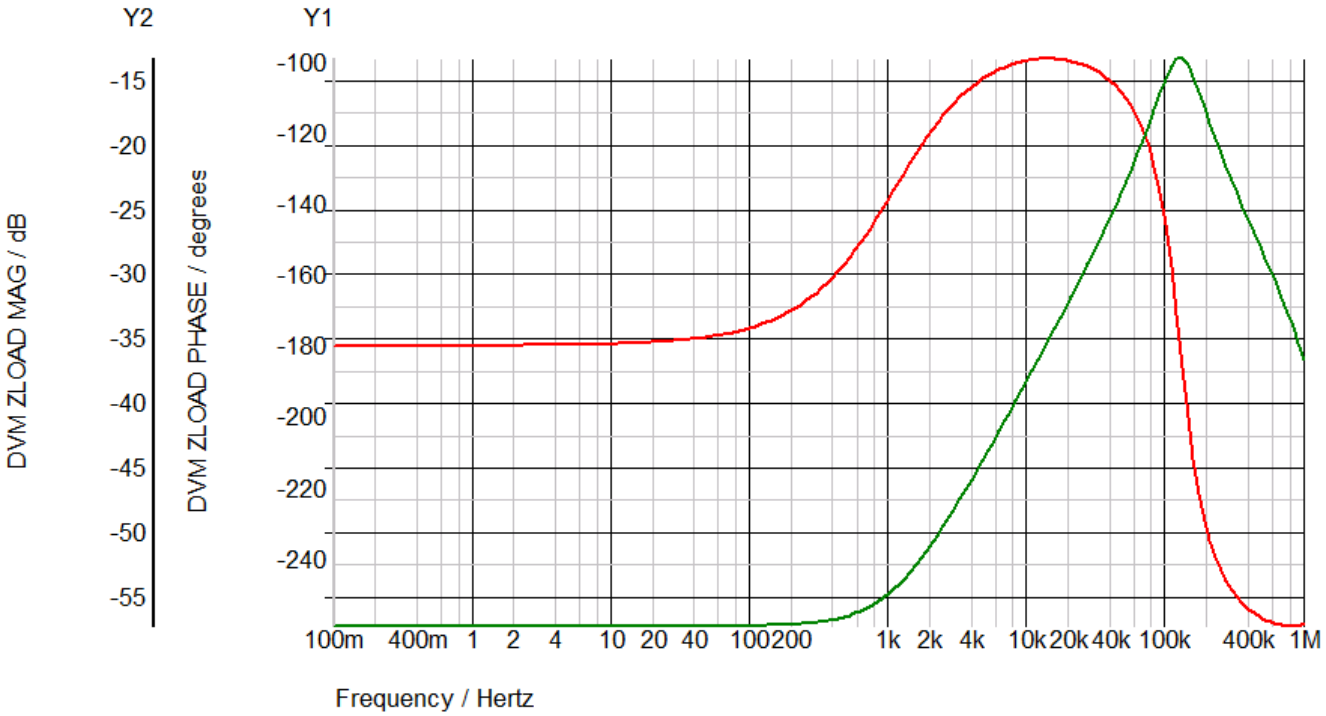

Figure 10. SiMetrix Screen Shot: LDO Output Impedance Simulation Result

After the control loop gain diminishes, the output impedance is dominated by the output capacitor; an effective capacitance of 8 µF with an ESR of 2 mΩ. The low-frequency impedance and output capacitor impedance are starting points for the lumped model at low and high frequencies. By inspection, there is a single zero causing the 20-dB/decade slope starting at 1.12 kHz, therefore, the low-frequency portion of the curve is easily modeled as a 1.36-mΩ resistor and an inductor with a reactance of 1.36 mΩ at 1.12 kHz. At the 3-dB corner, the inductive reactance equals the resistance, as shown in Equation 1 and Equation 2.

$$L * 2\pi f = X_L \tag{1}$$

and

$$L = \frac{1.36m\Omega}{2\pi(1.12kHz)} = 193nH \tag{2}$$

A 1.36-mΩ resistor in series with a 193-nH inductor and an 8-µF capacitor with 2 mΩ of ESR in parallel is a good place to start, as shown in Figure 11.

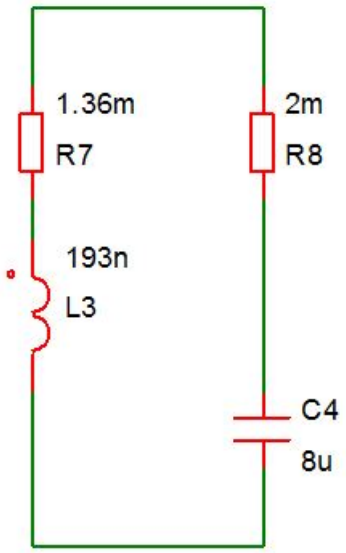

Figure 11. Two Branch Lumped Model Screen Capture From SiMetrix

The circuit in Figure 11 has an impedance curve that looks similar to Figure 12. This plot was analytically calculated using a math application.

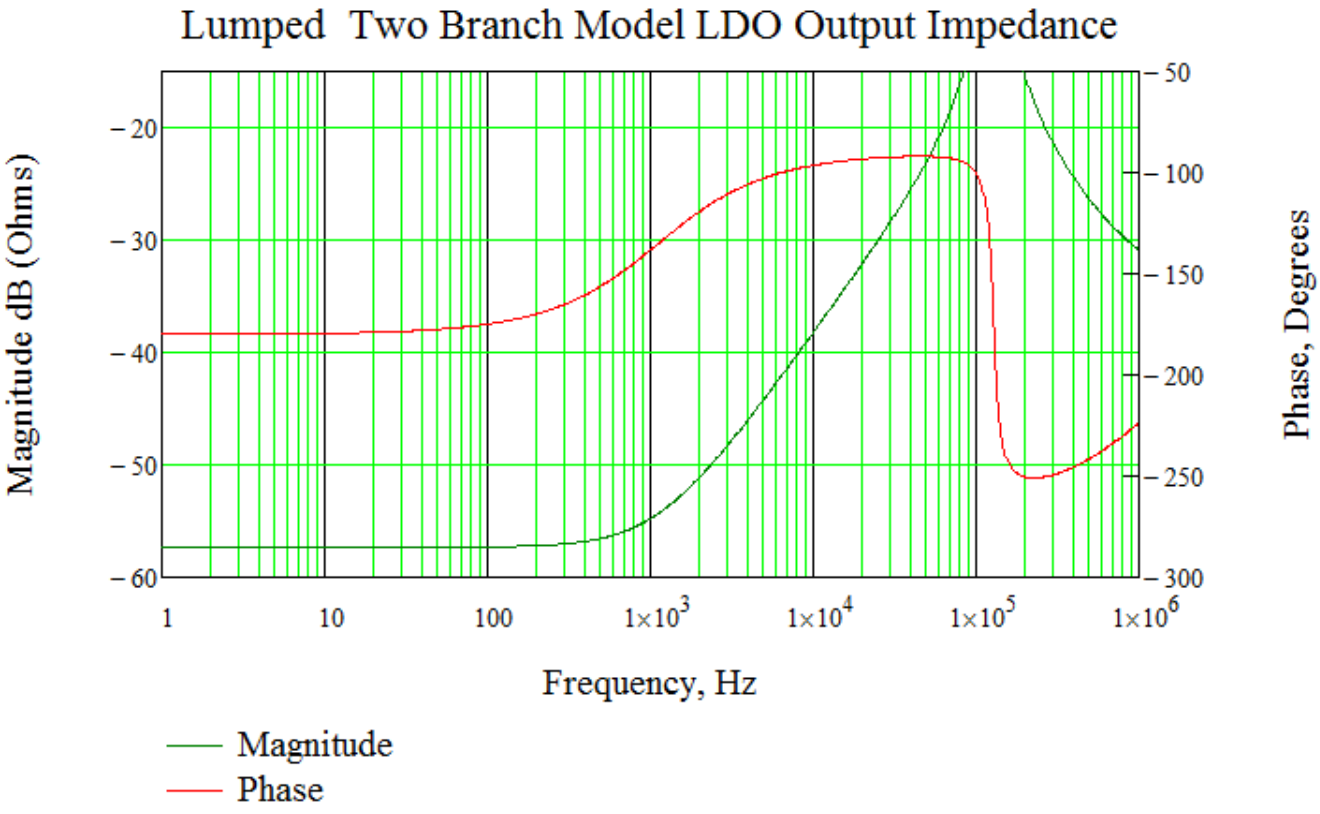

Figure 12. Two Branch Lumped Model Response

The resulting model is close, but there appears to be an extra pole in the simulated response caused by the loop gain of the regulator falling off. The pole is evident in the flatter slope of the gain curve of the simulated result versus the two-branch lumped model shown in Figure 13.

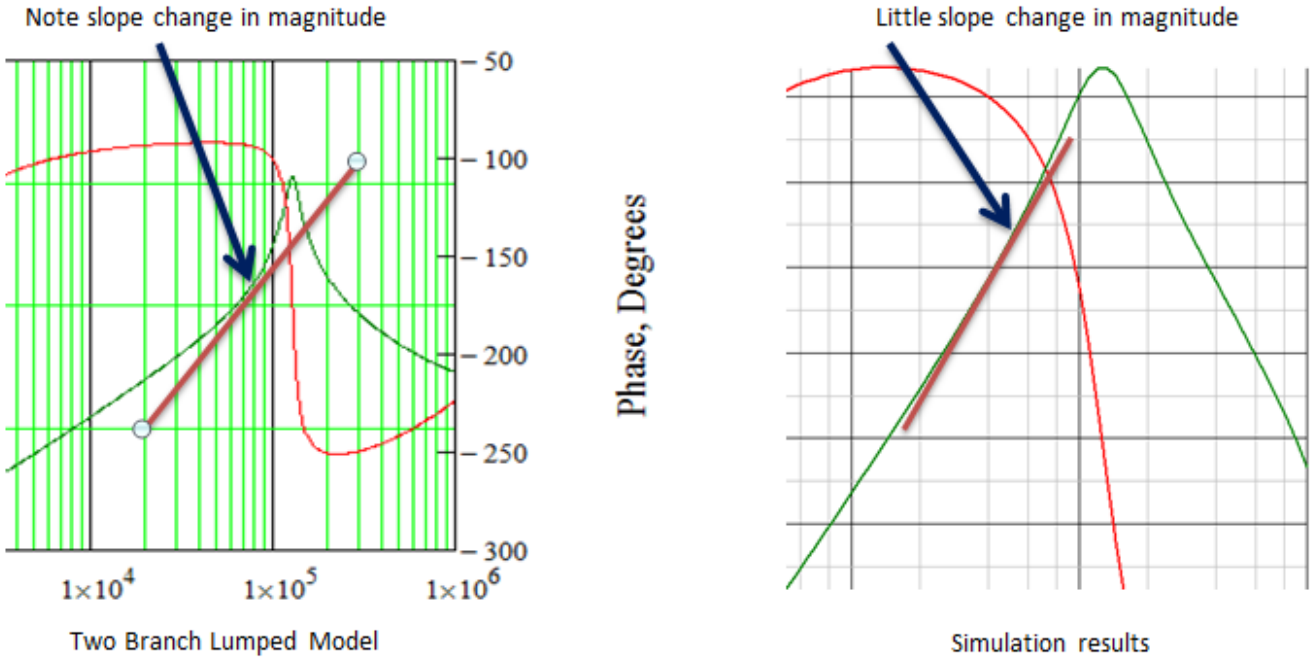

Figure 13. Two Branch Model Versus Simulation Results

The slope change of the magnitude at near 60 kHz is not evident in the simulated result. Add an additional R-C branch to cancel the magnitude increase with a pole at 60 kHz. The corner frequency is approximately 60 kHz by inspection, and capacitive reactance equals resistance. Equation 3 constrains the resistance and capacitance.

$$R = \frac{1}{2\pi C(60\text{kHz})} \tag{3}$$

However, Equation 3 contains two unknown variables, and cannot be solved yet. To find the unknown variable, match the peak impedance between the simulated and lumped models, as shown in Equation 4. This simulated model has a peak impedance of –13.34 dBΩ, and equals 215.3 mΩ. The two-branch lumped model has a peak impedance of 1.13 dBΩ, and equals 1.126 Ω. Impedances are read from the magnitude curves using the cursor feature of SiMetrix and the math application. The reactance of the new branch must bring the peak impedance down to 215.3 mΩ. The peak occurs at 129 kHz. There are now two equations with two unknown variables to solve that give the resistance and capacitance of the third branch.

$$R + \frac{1}{2\pi C(129\text{kHz})} = 266m\Omega \tag{4}$$

Combining Equation 3 and Equation 4 yields Equation 5.

$$\frac{1}{2\pi C(60\text{Khz})} + \frac{1}{2\pi C(129\text{kHz})} = 266m\Omega \tag{5}$$

Solving for the impedance needed in parallel with 1.126 Ω to get 215 mΩ yields 266 mΩ at 129 kHz.

Solving Equation 5 for C gives 14.6 µF. Back substitution into Equation 3 gives a resistance value of 182 mΩ. Figure 14 shows the new lumped model.

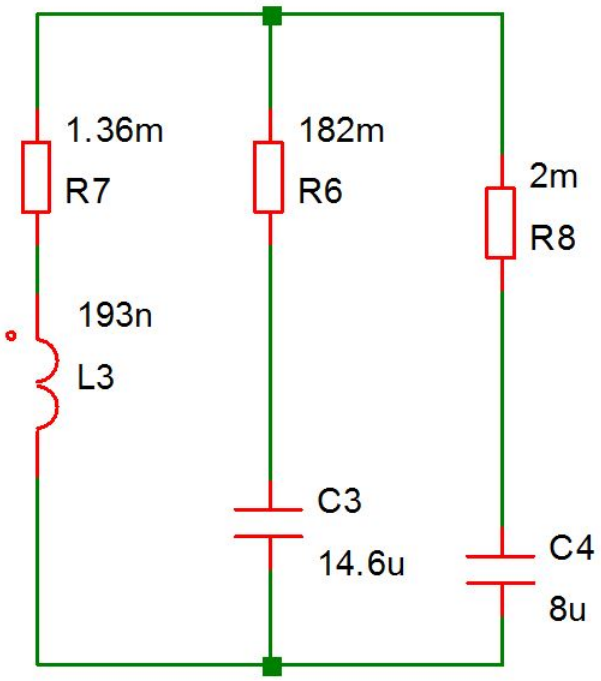

Figure 14. Three-Branch Lumped Model Screen Capture From SiMetrix

The new lumped model has the impedance characteristic shown in Figure 15, along with the simulated result for reference. Observe the flatter slope around 60 kHz and the matching impedance peak. Given that the actual circuit will have substantial variation in component values and parasitic elements, the lumped model is likely good enough to be used.

The next step is to validate the model by comparing the lumped model with a full transient simulation of the SiMetrix model.

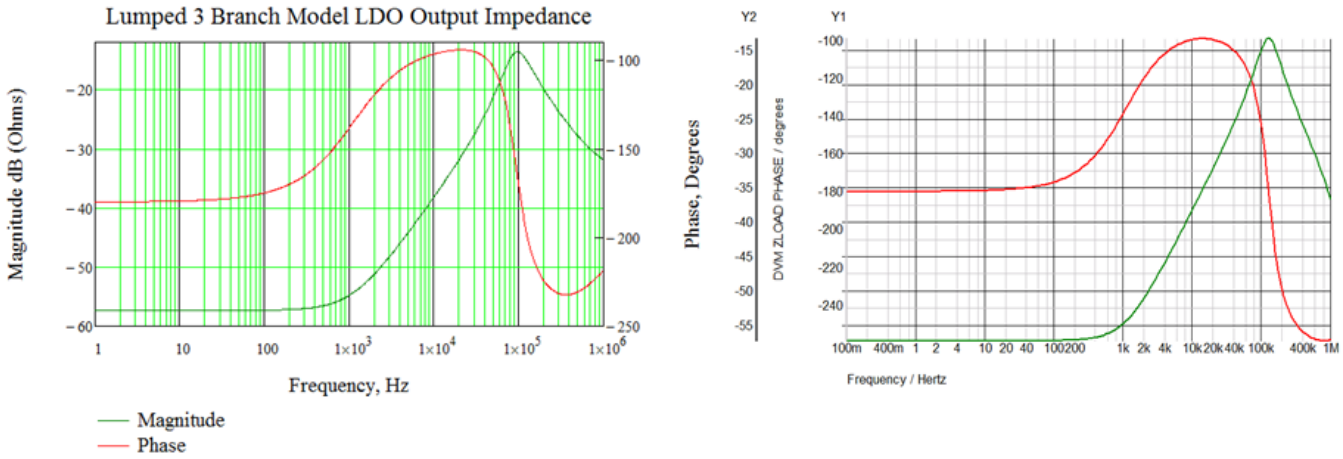

Figure 15. Three Branch Model Versus Simulation Results

The simulated load step for both the SiMetrix model and the lumped model shown in Figure 14 validates that the lumped model effectively models the output characteristics of the LDO.

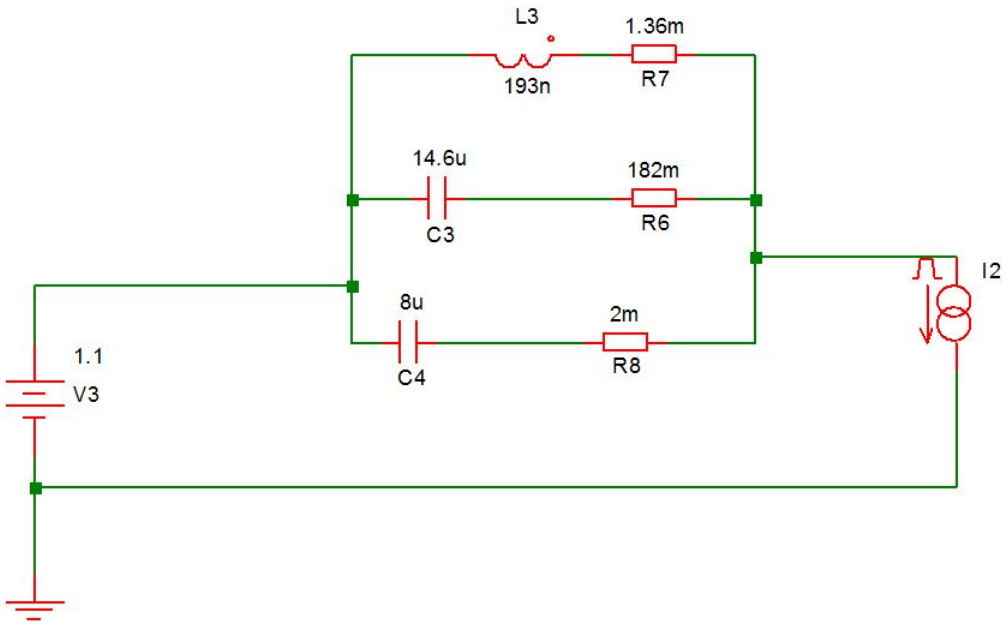

Figure 16. Three-Branch Model Simulation Test Circuit

In Figure 17, the blue line is the load step applied independently to the output of the LDO and lumped model. The green line is the full LDO SiMetrix transient simulation output, and the red line is the ideal voltage source in series with the previously developed lumped model (see Figure 16). The undershoot and overshoot match very closely, with some variation in the ringing frequency. Of course, if hardware is available, then bench test results provide additional verification of the model.

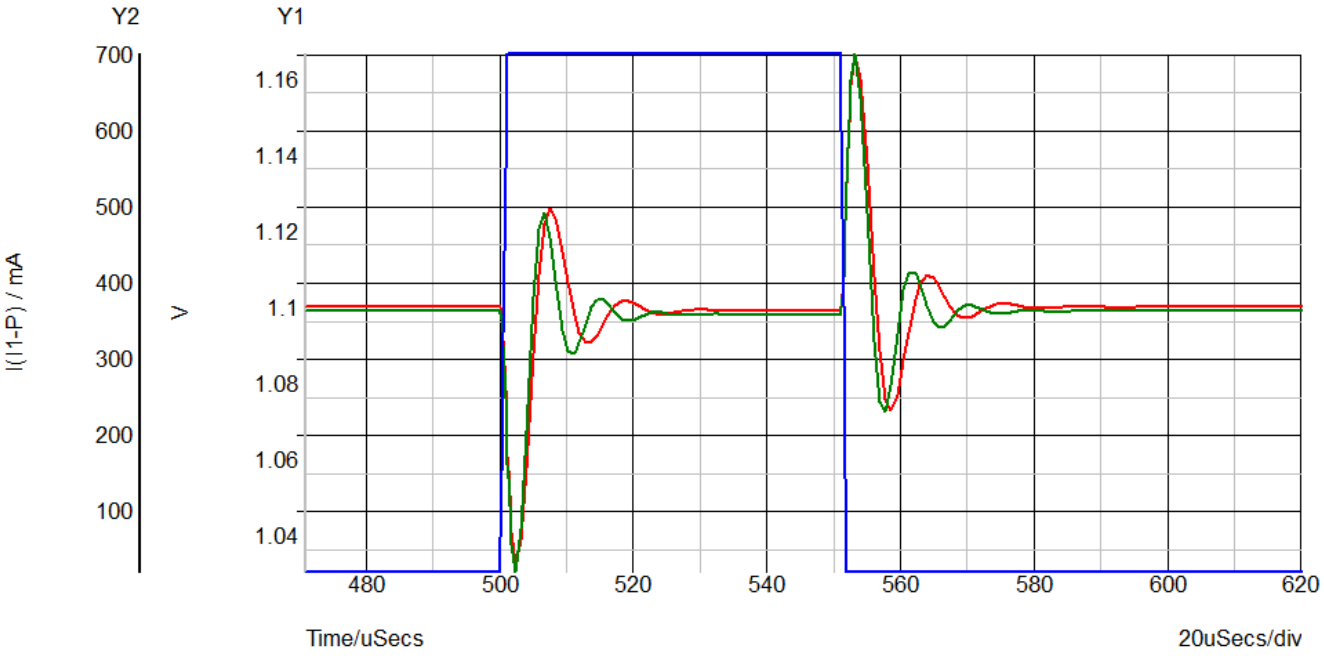

Figure 17. Step Response for Lumped Model vs SiMetrix Model

6 Summary

A lumped output impedance model is a useful tool for system validation. Where direct measurement is not possible, simulation provides the output impedance characteristic, and the designer can extract a lumped model from the simulation results.

7 References

See the SiMetrix website for information on the simulator user manuals.

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