Application Report
SLVA943–February 2018

Power Supply Design for NXP i.MX 6 Using the TPS65023

ABSTRACT

This document details the design considerations of a power management unit solution for the NXP i.MX 6Solo and 6DualLite processors using the TPS65023 power management IC (PMIC).

The TPS65023 device has an input range from 2.5 to 6 V. The device has three low-dropout (LDO) regulators and three step-down converters that provide the 1.425-, 3-, 1.8-, 3.3-, and 1.35-V power rails in the appropriate power-up and power-down sequence that is required by the i.MX 6Solo and 6DualLite processors. For minor variations on this design to provide power to the i.MX 6 SoloX, SoloLite, SLL, UltraLite, and ULL processor variants, refer to the modified block diagrams in Appendix A. For an i.MX 6-SL power solution targeted at IoT Gateway applications, refer to the VVDN design on the RadiumBoards website.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

This reference design applies to the NXP i.MX 6Solo and 6DualLite family of applications processors. This report provides all the required external components necessary to achieve the required output and sequence to power-up and power-down the i.MX 6 processor. This reference design provides a solution for a VSYS voltage being 5 V, DDR3L SDRAM requiring 1.35 V, and NVCC power domain requiring 3 V. However if DDR3, LPDDR2, or LPDDR3 SDRAM is desired, the required output can be achieved by modifying a resistor divider, which is detailed in Section 2.3 of this document.

2 Power Requirements

Figure 1 shows a block diagram of the TPS65023 device and i.MX 6Solo and 6DualLite processor interfaces. Table 1 lists the power output capabilities of the TPS65023 and matches them to the power requirements of the i.MX 6Solo and 6DualLite processor.Figure 3 shows a circuit schematic detailing the TPS65023 device and the sequencing circuit.

NOTE: The generic part number TPS65023 is used for simplicity in this document. The TPS65023B device is shown in the block diagram and schematic because the TPS65023B has improved I^2C performance. The -B version is also on the BOM and should be assembled on the final solution.

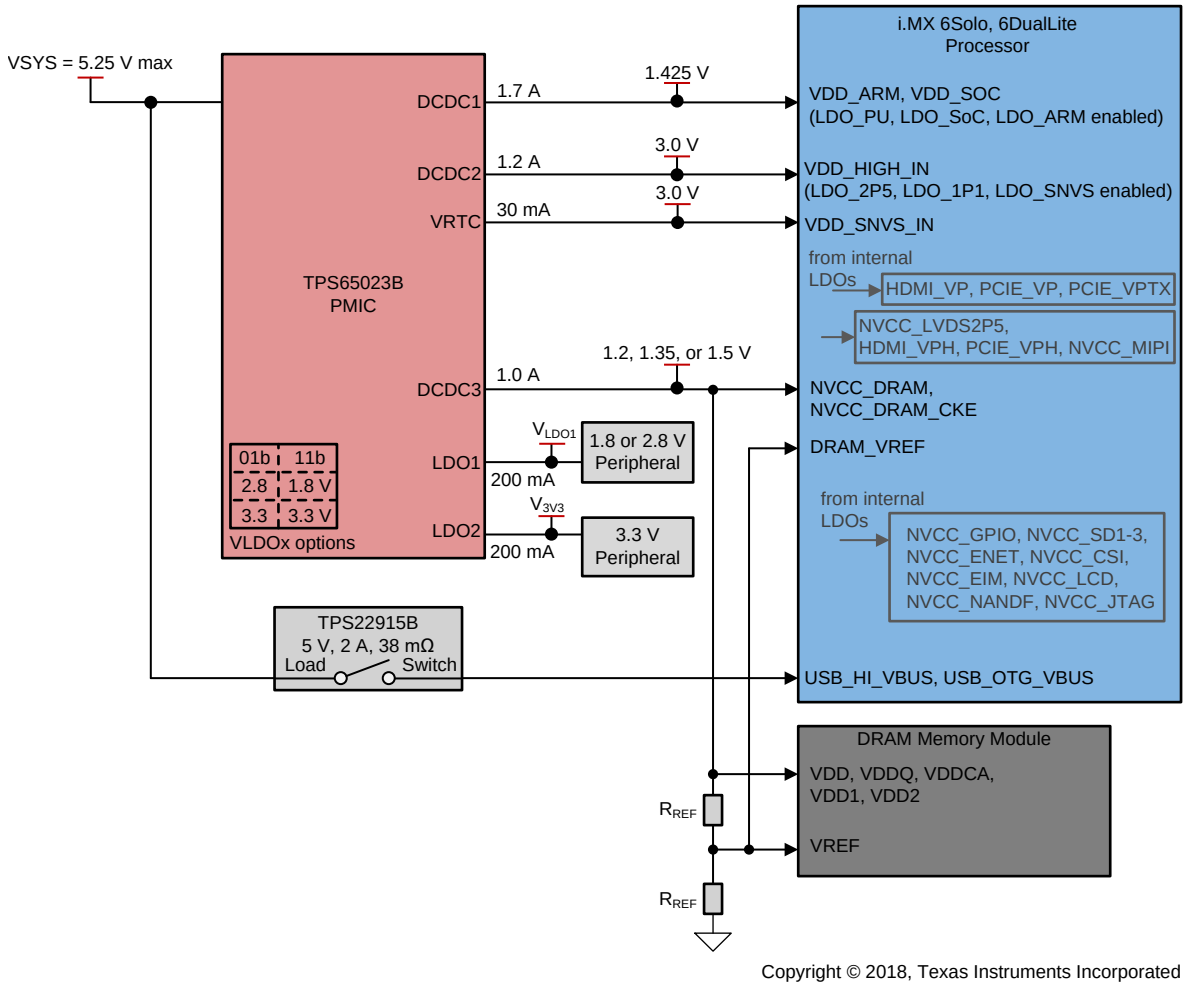

Figure 1. TPS65023 Power Solution Block Diagram for i.MX 6Solo and 6DualLite

Table 1 lists the i.MX 6 power requirements which are determined from the *i.MX 6Solo/6DualLite Applications Processors for Consumer Products* Data Sheet and the *i.MX 6Solo/6DualLite Applications Processors for Industrial Products* Data Sheet.

Table 1. i.MX 6Solo and 6DualLite Power Requirements

TPS65023					i.MX 6Solo/6DualLite		
POWER-UP SEQUENCE	POWER-DOWN SEQUENCE	POWER SUPPLY (OUTPUT)	OUTPUT CURRENT [mA]	OUTPUT VOLTAGE [V]	POWER SUPPLY (INPUT)	NOMINAL RATING [V]	MAX CURRENT [mA]
2 or 3	1 or 2	DCDC1	1700	1.425	VDD_ARM, VDD_SOC(1)	Minimum: 1.35 Typical: 1.425 Maximum: 1.5	1510(2)
2	2	DCDC2	1200	3	VDD_HIGH_IN(3)	Minimum: 2.9 Maximum: 3.3	125 + Maximum IO current
3	1	DCDC3	1000	1.35	NVCC_DRAM, NVCC_DRAM_CKE	Minimum: 1.283 Typical: 1.35 Maximum: 1.45	1000
3	1	LDO1	200	1.8 or 2.8	1.8-V or 2.8-V peripherals and NVCC rails not supplied by internal LDO regulators	N/A	N/A
3	1	LDO2	200	3.3	3.3-V peripherals and NVCC rails not supplied by internal LDO regulators	N/A	N/A
1	3	VRTC	30	3	VDD_SNVS_IN(4)	3 V ± 20%	1

(1) LDO_PU, LDO_SoC, and LDO_ARM internal LDO regulators are enabled to generate the specific voltage required by the ARM and SoC inputs.

(2) The maximum current for the VDD_ARM and VDD_SOC core rails is determined from the *Typical max power* section in the AN4576 Application Note.

(3) LDO_2P5, LDO_1P1, and LDO_SNVS internal LDO regulators are enabled to generate voltages for all NVCC power inputs as well as the HDMI_VPH and PCIE_VPH supply voltages.

(4) Coin cell battery can be used as backup power for VDD_SNVS_IN, which is usually powered by the VDD_HIGH_IN supply voltage.

The TPS65023 device fulfills all the power requirements with three step-down converters and three LDO regulators. To meet the power sequence requirements, a simple sequencing circuit is used, which is detailed in Figure 3.

Combining the VDD_ARM and VDD_SOC core rails does not limit the clocking frequency when the LDO_PU, LDO_SoC, and LDO_ARM internal LDO regulators are used to set the ideal voltage for the ARM and SoC point-of-load. As a result, all the clock frequency setpoints of 996 MHz, 792 MHz, 396 MHz, and sub-328 MHz can be supported by modifying the VDD_ARM_CAP, VDD_SOC_CAP, and VDD_PU_CAP LDO output setpoints.

The input power rails of the i.MX 6 processor, USB_HI_VBUS and USB_OTG_VBUS, require 5 V (typical) and 5.25 V (maximum). The input power to this system, VSYS, must be 5 V and cannot be greater than 5.25 V because the TPS22915B load switch provides power to these two rails and a load switch does not convert voltage. The USB_HI_VBUS and USB_OTG_VBUS rails are not shown in Table 1 because they are not regulated voltages and are not supplied by the TPS65023B device. The TPS22615B load switch is enabled and disabled by the controller of the system for saving power.

2.1 Power-Up Sequence

The required power-up sequence of the supply rails specified by the i.MX 6Solo/6DualLite data sheet is as follows:

1. VDD_SNVS_IN which is primarily supplied by the VRTC regulator
2. VDD_HIGH_IN which is supplied by the DCDC2 converter
3. VDD_SOC and VDD_ARM which are supplied by the DCDC1 converter, and NVCC_DRAM and NVCC_DRAM_CKE which are supplied by the DCDC3 converter

NOTE: The SRC_POR_B input pin of the i.MX6 processor controls the processor power-on reset (POR) and must be immediately asserted at power-up and stay asserted until the ARM and SoC core rails are in regulation. Additionally, the USB_OTG_VBUS and USB_H1_VBUS rails are not part of the power supply sequence, and the load switches that provide these rails can be enabled at any time.

The first step in the power-up sequence is turning on the VDD_SNVS_IN rail with the VRTC regulator. In the TPS65023 device one of the three LDO regulators is designated as VRTC with an output of 3 V. The VRTC regulator defaults to turning on when the TPS65023 device powers on, which means the VDD_SNVS_IN rail is always the first rail on.

The second step is part of the sequencing circuit. A slider switch is used in the schematic; however, the switch can be replaced with an outside enable signal going HIGH. By setting the signal HIGH, it will set the D1 diode to forward bias, whereas, the D2 and D3 diodes are reverse bias. With the D1 diode in forward bias, the EN_1 signal goes HIGH and turns on the DCDC2 converter. The DCDC2 converter turns on at this time because no sequence requirements are required for what is powered by the DCDC2 converter. The threshold voltage for the enable input is 1.3 V. The DCDC2 converter has an output voltage of 3 V and must be used to turn on the remaining enable pins.

The DCDC1 converter provides power to the core rails, VDD_ARM and VDD_SOC. The only power-up requirement for the iMX6 Solo and DualLite processors is that VDD_SNVS_IN rail is powered on first. As a result, an option to sequence the VDD1 voltage with the DCDC2 converter from the EN_1 signal (R12 installed) or with the DCDC3 converter from the EN_2 signal (R13 installed) is available. By default, the R13 resistor is installed and the DCDC1 converter will sequence at the same time as the DCDC3 converter.

When the DCDC2 voltage is greater than 1.3 V, the DCDC2 output goes through an RC (R14 and C14) delay before enabling the DCDC3 converter and the remaining two LDO regulators. After reaching the operating level, the DCDC3 voltage goes through a resistor divider and RC delay before going to the PWRFAIL_SNS pin, which sets the internal comparator for the PWRFAIL signal. The PWRFAIL output of the TPS65023 device is directly connected to the SRC_POR_B signal of the i.MX 6 processor with correct polarity.

The USB_HI_VBUS and USB_OTG_VBUS rails do not require sequencing. As a result, the ON pin of the TPS22915B load switch is pulled up to the VSYS voltage and the switch is enabled by default when the system input voltage is greater than 1 V.

The power-up sequence is complete. Figure 3 shows the schematic for the correct connections for the power-up sequence.

2.2 Power-Down Sequence

The i.MX 6 data sheet lists no specific restrictions for the power-down sequence of the i.MX 6Solo/DualLite IC. Because of the analog power-up sequence implemented in this design, the processor is powered off in the reverse order of the power-up sequence. The power-down sequence of the supply rails is as follows:

1. VDD_SOC and VDD_ARM which are supplied by the DCDC1 converter, and NVCC_DRAM and NVCC_DRAM_CKE which are supplied by the DCDC3 converter
2. VDD_HIGH_IN which is supplied by the DCDC2 converter
3. VDD_SNVS_IN which is primarily supplied by the VRTC regulator

To start the power-down sequence, the switch is turned off or the enable signal is set LOW which makes the D2 and D3 diodes forward biased. The PWRFAIL_SNS signal becomes LOW which pulls the PWRFAIL output LOW. The EN_2 signal becomes LOW and causes the output of the DCDC3 converter and LDO regulators to ramp down.

The D1 diode is now reverse biased, letting the C13 capacitor discharge into the R11 resistor, which creates a delay longer than the ramp down of the DCDC3 converter and LDO regulators. At this point, DCDC3 and DCDC1 converters are powered down in the correct order. The VRTC regulator is tied to the input voltage and, therefore, is only powered down when the input voltage starts ramping down. When a backup coin-cell battery is used, the VRTC regulator will remain on even when the main system input voltage is unavailable. This power-down sequence makes sure that the VRTC rail is the last rail on which fulfills all the requirements for the power-down sequence.

Figure 3 shows the correct connections for the power-down sequence.

2.3 Adjusting the Step-Down Output

Figure 2 shows the external resistor divider circuit.

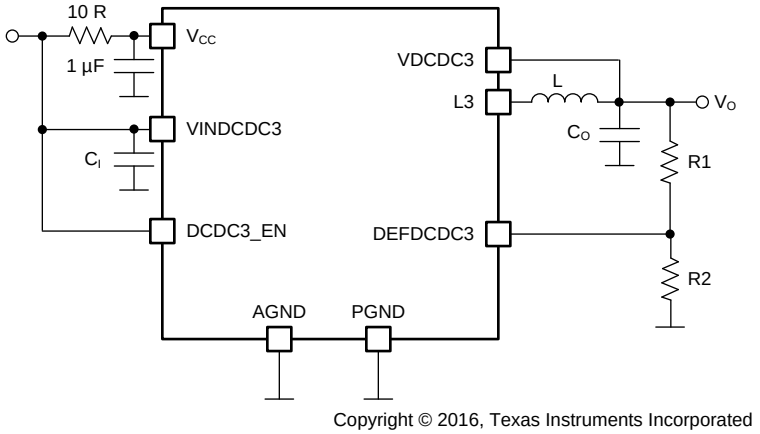

Figure 2. External Resistor Divider

The DEFDCDC1, DEFDCDC2, and DEFDCDC3 pins are used to set the output voltage for each step-down converter. By using an external resistor divider, the output voltage can be set from 0.6 up to the input voltage, $V_{(bat)}$. The total resistance (R1 + R2) of the voltage divider must be kept in the 1-MΩ range to keep a high efficiency at light loads.

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1 + R2}{R2}$$

where

$$V_{(DEFDCDCx)} = 0.6\ V$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDCx}} \right) - R2$$

2.4 Adjusting the Sequencing Circuit

In the schematic shown in Figure 3, the sequence circuit is designed with a DCDC3 output of 1.35 V. If DDR3, LPDDR2, or LPDDR3 SDRAM is desired over DDR3L SDRAM, then the resistor divider (R16 and R17) must be changed accordingly to provide 1 V to the PWRFAIL_SNS pin.

3 Schematic

Figure 3 shows the circuit schematic and details the external components required for the TPS65023 device to achieve the 1.425-, 3-, 1.8-, 3.3- and 1.35-V, power rails required by the i.MX 6Solo and 6DualLite processor. The sequencing circuit is also detailed to achieve the correct power-up and power-down sequence. A slider switch is shown in the schematic; however, any switching mechanism can be used, for example, an external enable signal.

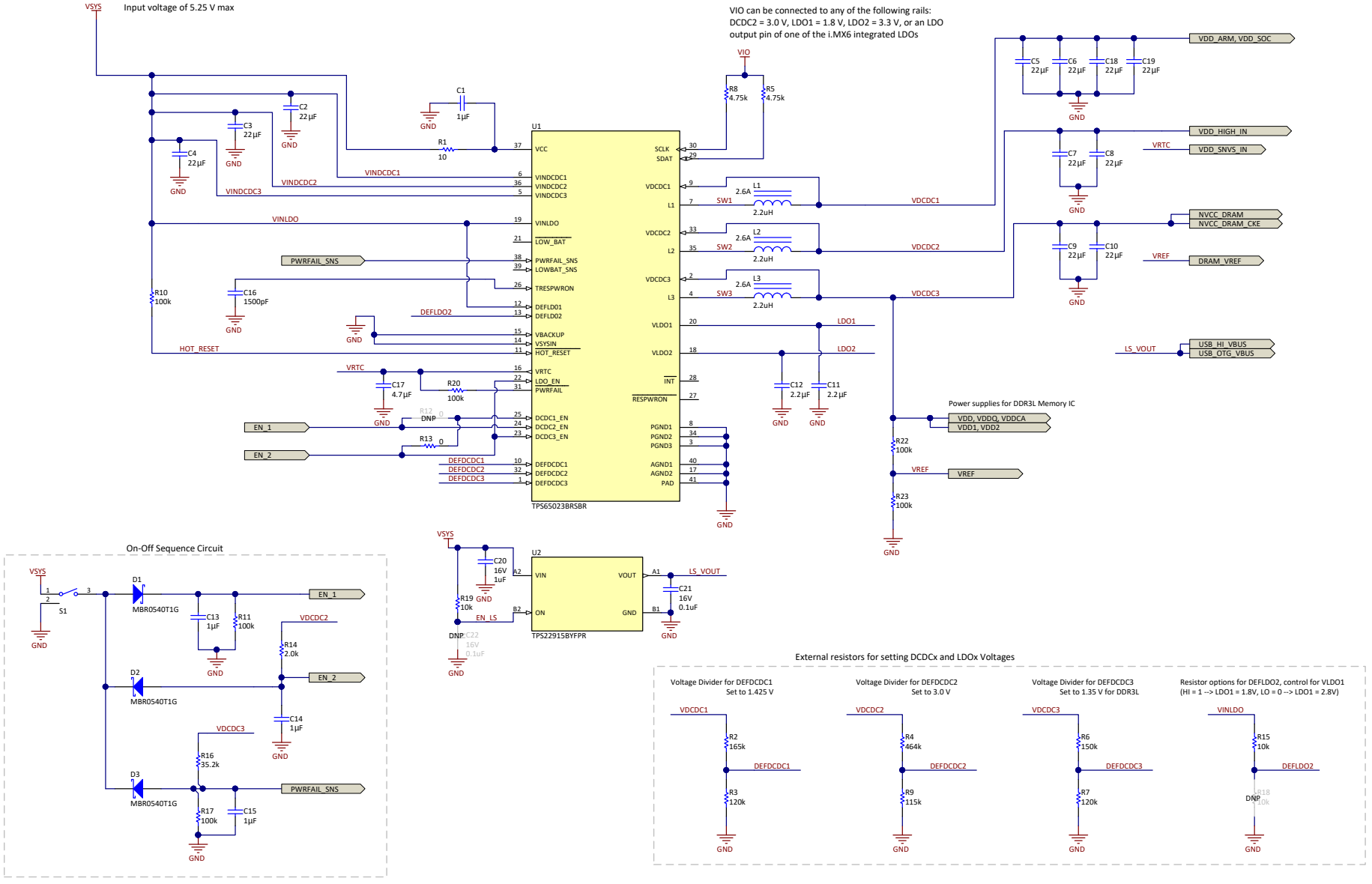

Figure 3. TPS65023 Circuit for i.MX 6Solo and 6DualLite Power Requirements

4 Bill of Materials (BOM)

Table 2 lists the BOM for this design.

Table 2. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB	1		Printed Circuit Board		XX####	Any
C1, C13, C14, C15	4	1uF	CAP, CERM, 1 µF, 16 V, +/- 20%, X5R, 0603	0603	885012106017	Wurth Elektronik
C2, C3, C4, C5, C6, C7, C8, C9, C10, C18, C19	11	22uF	CAP, CERM, 22 µF, 10 V, +/- 20%, X5R, 0603	0603	C1608X5R1A226M080AC	TDK
C11, C12	2	2.2uF	CAP, CERM, 2.2 µF, 10 V, +/- 20%, X5R, 0603	0603	C0603C225M8PACTU	Kemet
C16	1	1500pF	CAP, CERM, 1500 pF, 10 V, +/- 10%, X5R, 0201	0201	GRM033R61A152KA01D	MuRata
C17	1	4.7uF	CAP, CERM, 4.7 µF, 10 V, +/- 20%, X5R, 0402	0402	GRM155R61A475M	MuRata
C20	1	1uF	CAP, CERM, 1 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603	GCM188R71C105KA64D	MuRata
C21	1	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0603	0603	GRM188R71C104KA01D	MuRata
D1, D2, D3	3	40V	Diode, Schottky, 40 V, 0.5 A, SOD-123	SOD-123	MBR0540T1G	ON Semiconductor
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
L1, L2, L3	3	2.2uH	Inductor, Film, 2.2 uH, 2.6 A, 0.084 ohm, AEC-Q200 Grade 0, SMD	2.5x2mm	TFM252012ALMA2R2MTAA	TDK
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
R1	1	10	RES, 10, 5%, 0.063 W, 0402	0402	CRCW040210R0JNED	Vishay-Dale
R2	1	165k	RES, 165 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1653X	Panasonic
R3, R7	2	120k	RES, 120 k, 1%, 0.063 W, 0402	0402	CRCW0402120KFKED	Vishay-Dale
R4	1	464k	RES, 464 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402464KFKED	Vishay-Dale
R5, R8	2	4.75k	RES, 4.75 k, 1%, 0.063 W, 0402	0402	CRCW04024K75FKED	Vishay-Dale
R6	1	150k	RES, 150 k, 1%, 0.063 W, 0402	0402	CRCW0402150KFKED	Vishay-Dale
R9	1	115k	RES, 115 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402115KFKED	Vishay-Dale
R10, R11, R17, R20, R22, R23	6	100k	RES, 100 k, 1%, 0.063 W, 0402	0402	CRCW0402100KFKED	Vishay-Dale
R13	1	0	RES, 0, 5%, 0.063 W, 0402	0402	MCR01MZPJ000	Rohm
R14	1	2.0k	RES, 2.0 k, 5%, 0.063 W, 0402	0402	CRCW04022K00JNED	Vishay-Dale
R15, R19	2	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale
R16	1	35.2k	RES, 35.2 k, 0.1%, 0.1 W, 0603	0603	RT0603BRD0735K2L	Yageo America
S1	1		Switch, Slide, SPST, On-Off, 1 Pos, 0.4VA, 20V, SMT	10.03x9.14mm	ES02MSABE	C&K Components
U1	1		POWER MANAGEMENT IC FOR LI-ION POWERED SYSTEMS, RSB0040B (WQFN-40)	RSB0040B	TPS65023BRSBR	Texas Instruments
U2	1		5.5V, 2A, 38mΩ Load Switch With Quick Output Discharge, YFP0004AAAA (DSBGA-4)	YFP0004AAAA	TPS22915BYFPR	Texas Instruments
C22	0	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X5R, 0402	0402	GRM155R61C104KA88D	MuRata
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R12	0	0	RES, 0, 5%, 0.063 W, 0402	0402	MCR01MZPJ000	Rohm
R18	0	10k	RES, 10 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040210K0JNED	Vishay-Dale

5 Waveforms

The following waveforms demonstrate the power-up and power-down sequence of the TPS65023 device as required by the i.MX 6Solo and 6DualLite processors.

Figure 4 shows the start of the power-up sequence where the VSYS rail turns on with the primary enable switch (SW1) in the *ON* position (pins 1 and 3 shorted). The VRTC regulator turns on first and the DCDC2 converter turns on after a short delay.

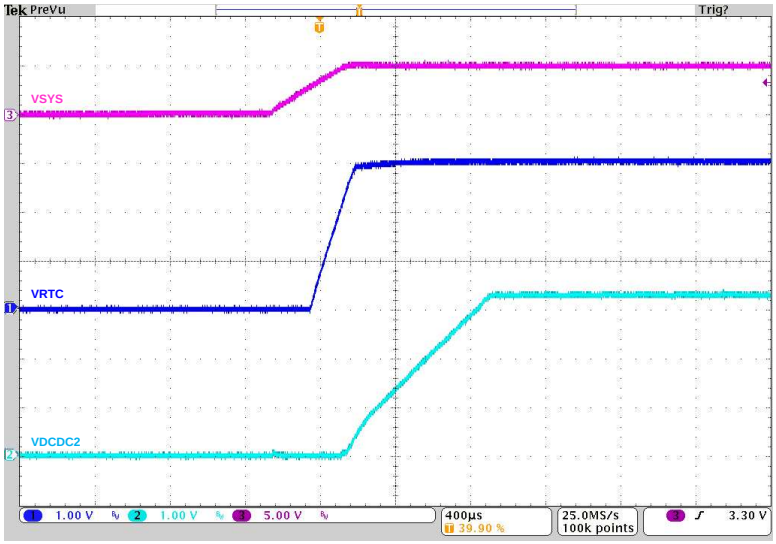

Figure 4. Power-Up Sequence for VRTC and DCDC2

Figure 5 shows the start of the power-up sequence again where the VSYS voltage turns on with SW1 in the *ON* position. In this waveform, the timing shown is from the DCDC2 converter being enabled by the EN_1 signal to the DCDC1 converter being enabled by the EN_2 signal, which is driven high by the output of the DCDC2 converter.

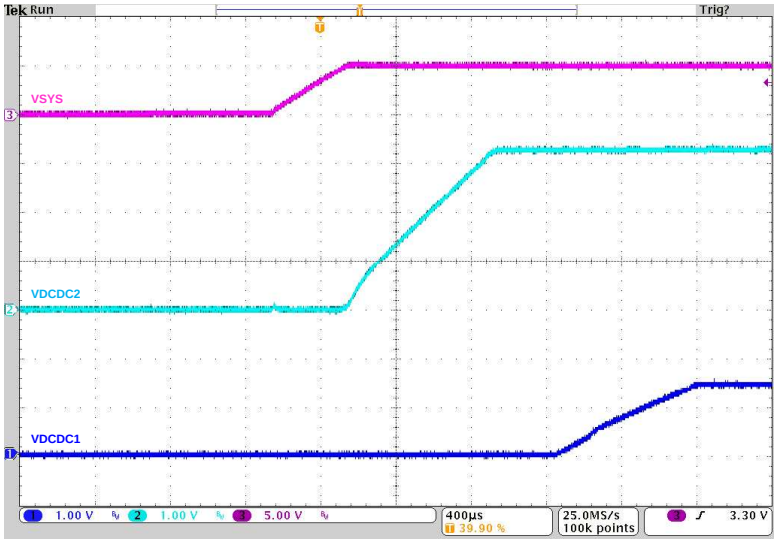

Figure 5. Power-Up Sequence for DCDC2 and DCDC1

Figure 6 shows the portion of the power-up sequence where the DCDC2 converter turns on after being enabled by the EN_1 signal. The output of the DCDC2 converter drives the EN_2 signal and is delayed by the RC delay (R14 and C14). This delay should make sure that DCDC2 converter reaches its final voltage and is in regulation before the DCDC1 and DCDC3 converters are enabled. After the EN_2 signal has risen to greater than the V_{IH} threshold of the enable pin, both the DCDC1 and DCDC3 converters are enabled at the same.

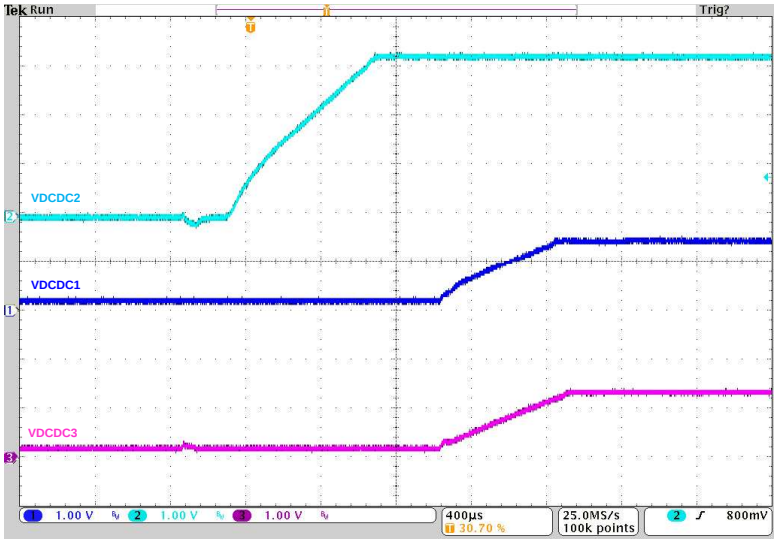

Figure 6. Power-Up Sequence for DCDC2, DCDC1, and DCDC3

Figure 7 shows the portion of the power-up sequence where the DCDC1 and DCDC3 converters turn on at the same time. The LDO regulators, which are also controlled by the EN_2 signal, do not require any internal pre-biasing and seem to be enabled slightly before the DCDC1 and DCDC3 converters. This timing is acceptable because the LDO regulators are not part of the power-up sequence requirements of the i.MX 6 processor. Only one of the LDO regulators (LDO1) is captured; however, both LDO regulators share the same enable pin and are enabled at the same time.

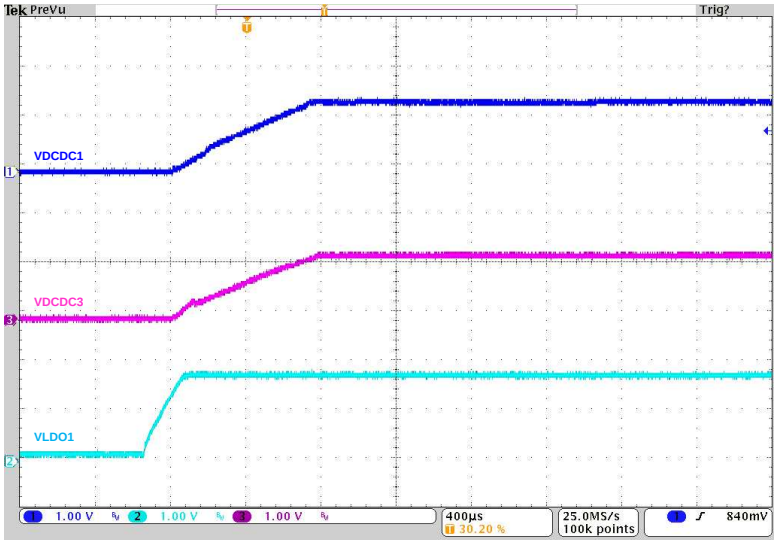

Figure 7. Power-Up Sequence for DCDC1, DCDC3, and LDO1

All power-down sequencing diagrams are shown as a reference only because the i.MX 6Solo and 6DualLite processors have no requirements for power-down sequencing.

Figure 8 shows the power-down sequence for each output showing that the DCDC1 and DCDC3 converters turn off at the same time. The relative power-down timing of the LDO regulators (LDO1) is shown as a reference, but all three power rails shown in the diagram are controlled by the same EN_2 signal. The EN_2 signal is pulled low immediately when the SW1 switch is set to the *OFF* position (pins 1 and 2 shorted).

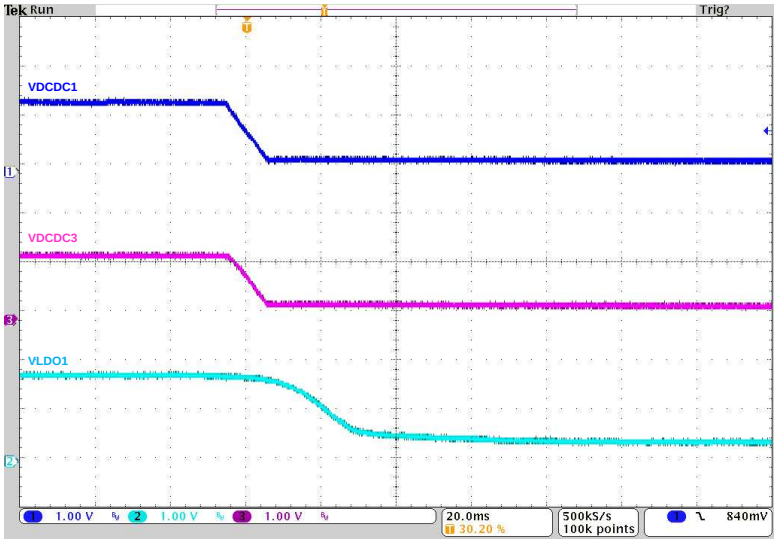

Figure 8. Power-Down Sequence for DCDC1, DCDC3, and LDO1

Figure 9 shows the power-down sequence for each output showing that the DCDC2 converter turns off after the DCDC1 and DCDC3 converters turn off at the same time. The DCDC2 converter is controlled by the EN_1 signal, which is low when the voltage on the C13 capacitor has discharged through the R11 resistor and drops to less than the V_{IL} threshold of the enable pin. The DCDC1 and DCDC3 converters have a load of 300 Ω applied at the output.

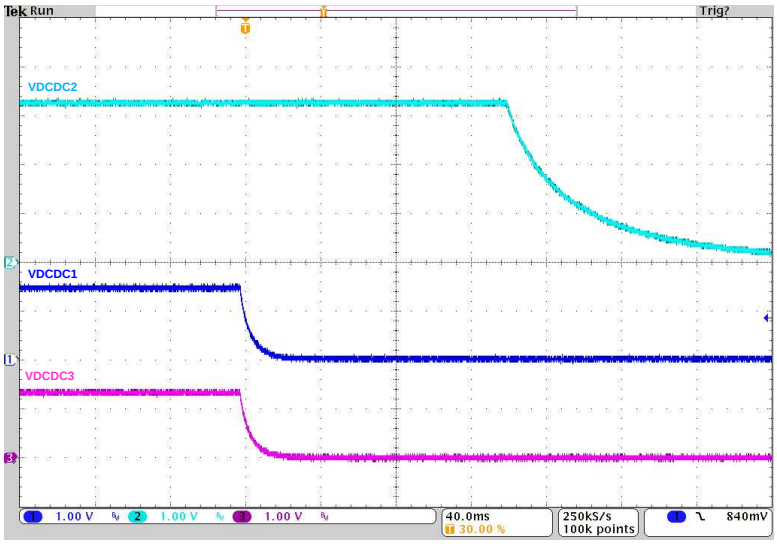

Figure 9. Power-Down Sequence for DCDC2, DCDC1, and DCDC3

Figure 10 shows the power-down sequence for the DCDC2 and DCDC1 converters again. This waveform shows that the VSYS input voltage can stay high when the SW1 switch is set to the *OFF* position. The EN_1 and EN_2 signals follow the change in position of the switch to disable the regulators and achieve power savings in the design, if desirable by the application.

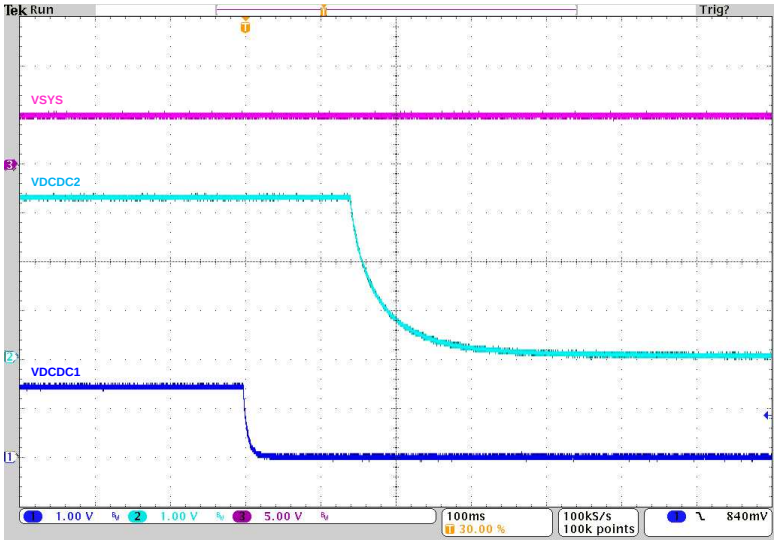

Figure 10. Power-Down Sequence for VSYS, DCDC2, and DCDC1

Figure 11 shows the power-down sequence timing from when the primary ENABLE signal is pulled low (the result of the SW1 switch in the *OFF* position) to when the DCDC2 converter turns off. The VRTC regulator is also shown to verify that this is the last voltage to turn off. In the waveform, the input voltage (VSYS) does not turn off, so the VRTC regulator stays on the entire time. The VRTC regulator stays on when the VSYS voltage does turn off but a backup battery is also available, attached to the VBACKUP pin of the TPS65023 device.

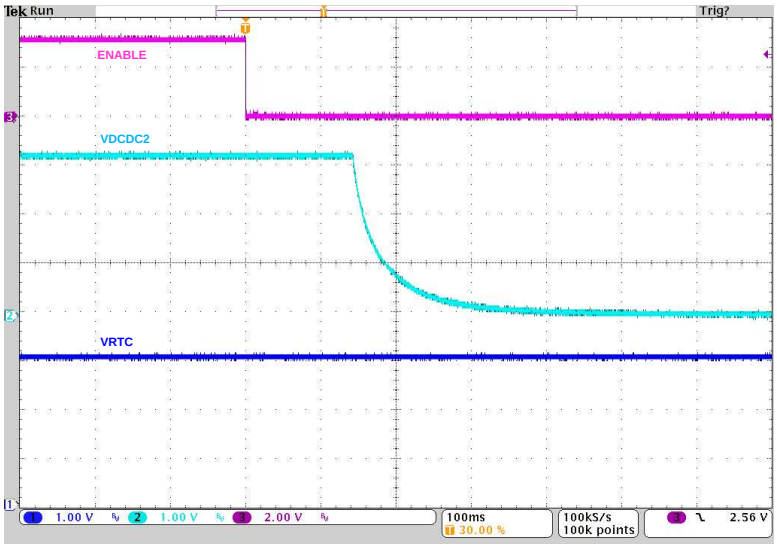

Figure 11. Power-Down Sequence for ENABLE, DCDC2, and VRTC

6 Transient Response

Table 3 lists the transient requirements and results for each DC-DC step-down converter. Transient requirements are provided by the i.MX 6Solo/6DualLite data sheet.

Table 3. Transient Requirements and Results

STEP-DOWN CONVERTER	DCDC1 (mV)		DCDC1 RESULTS		i.MX 6 REQUIREMENTS	
	MINIMUM (–)	MAXIMUM (+)	MINIMUM (–)	MAXIMUM (+)	MINIMUM (–)	MAXIMUM (+)
DCDC1 (1.425-V typical voltage)	50	54.4	5%	5.44%	5.26%	12.3%
DCDC2 (3-V typical voltage)	52	54.4	2.89%	3.02%	6.67%	10%
DCDC3 (1.35-V typical voltage)	62	61.2	4.59%	4.53%	4.96%	7.41%

Figure 12 shows the transient response of the DCDC1 converter with a load going from 450 to 1500 mA in 1-µs steps. The transient response shows that the DCDC1 converter fits within the required range of 1.425 V – 5.26% to 1.425 V + 12.3%.

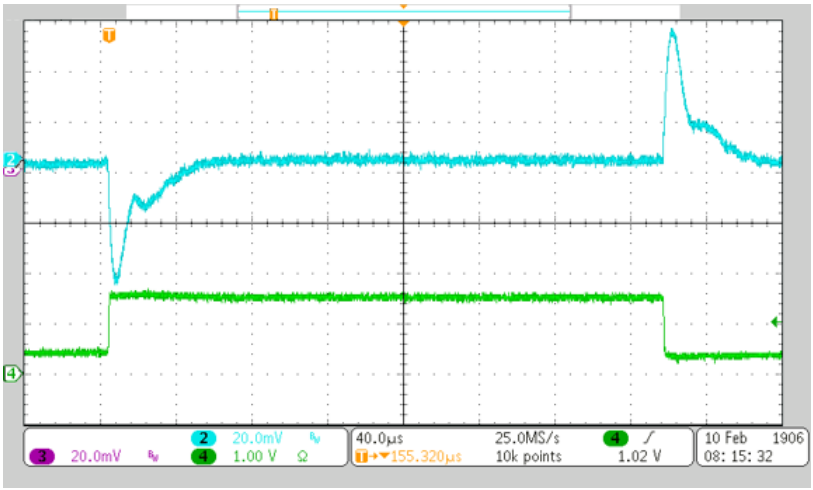

Figure 12. Transient Response for DCDC1

Figure 13 shows the transient response of the DCDC2 converter with a load going from 360 to 1200 mA in 1µs steps. The transient response shows that the DCDC2 converter fits within the required range of 3 V – 6.67% to 3 V ± 10%.

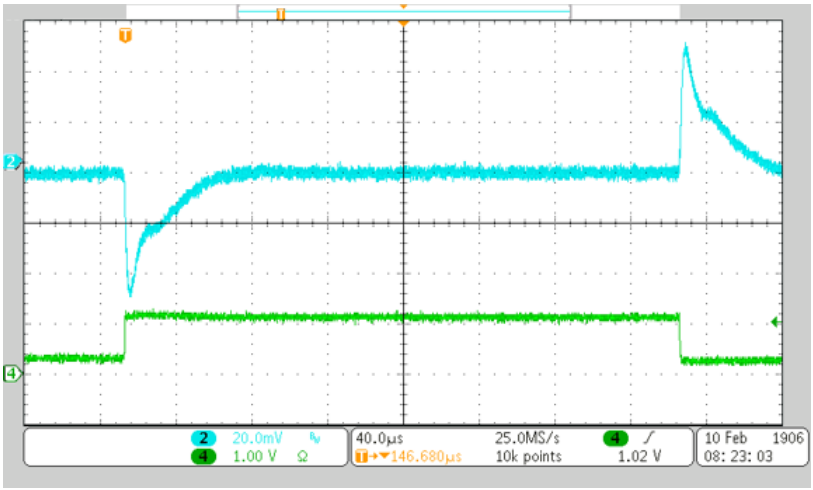

Figure 13. Transient Response for DCDC2

Figure 14 shows the transient response of the DCDC3 converter with a load going from 300 to 1000 mA in 1-µs steps. The transient response shows that the DCDC3 converter fits within the required range of 1.283 ≤ 1.35 ≤ 1.45.

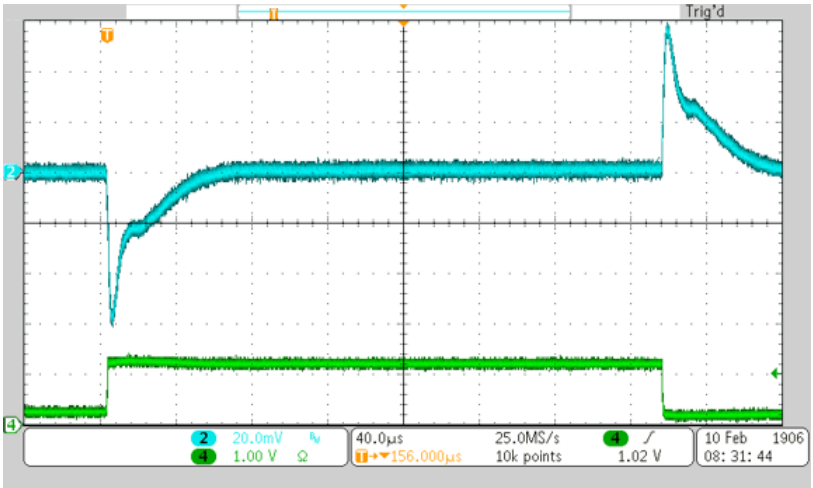

Figure 14. Transient Response for DCDC3

7 Efficiency Curves

The following efficiency curves show the efficiency for each of the converters over the possible range of output currents.

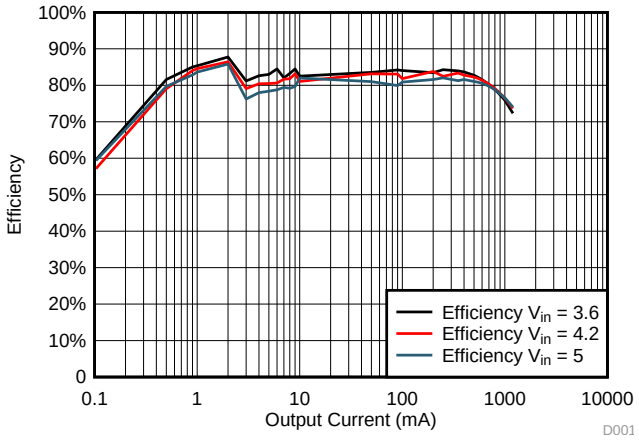

Figure 15. DCDC1 Efficiency

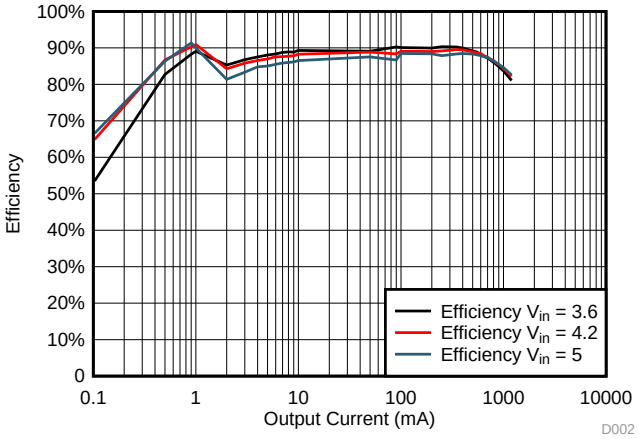

Figure 16. DCDC2 Efficiency

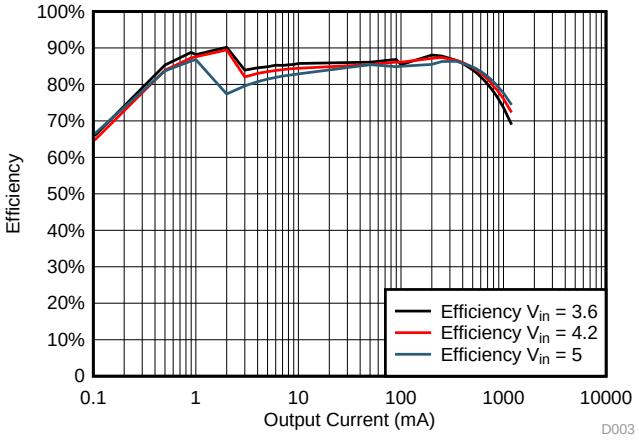

Figure 17. DCDC3 Efficiency

8 Layout

8.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Correct function of the device demands careful attention to the layout of the printed circuit board (PCB). If the layout is not done carefully, the converters and regulators may show poor line, load regulation, or both in addition to stability issues and electromagnetic interference (EMI) problems. Providing a low-impedance ground path is critical. Therefore, use wide and short traces for the primary current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

For the TPS65023 device, connect the PGND pins of the device to the thermal pad land of the PCB, and connect the analog ground connections (AGND) to the PGND at the thermal pad. Provide a good thermal and electrical connection of all GND pins using multiple vias to the ground plane. Keep the common path to the AGND pins, which return the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx line must be connected directly to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, and L3 traces).

8.2 Layout Example

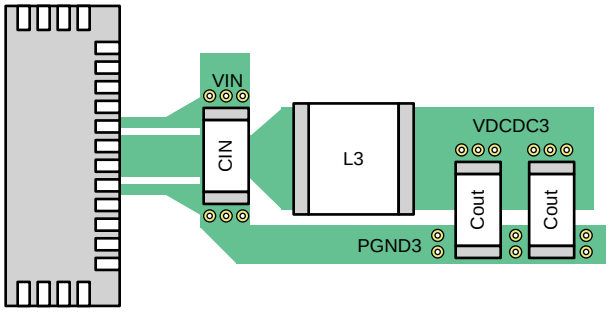

Figure 18. Layout Example of a DC-DC Converter

9 Conclusion

The TPS65023 device provides a low-cost, comprehensive power solution for the i.MX 6Solo and 6DualLite family of application processors. This design demonstrates the ability to use external components to adjust the output of the TPS65023 device to provide the required voltage rails for the i.MX 6Solo/6DualLite. The provided schematic shows a simple sequencing circuit that fits the power-up and the power-down sequence required by the i.MX 6Solo/6DualLite. If DDR3, LPDDR2, or LPDDR3 SDRAM is desired instead of DDR3L SDRAM, the output voltage of the DCDC3 converter can be adjusted by changing the resistor value in the resistor divider and in the sequencing circuit. Overall, the TPS65023 device is a solution with the flexibility and ability to meet the power requirements demanded by the i.MX 6Solo and 6DualLite. In addition, Appendix A provides a modification of the system block diagram to accommodate the i.MX 6 SoloX, SoloLite, SLL, UltraLite, and ULL processor variants using the TPS65023 device in a similar design with minor variations.

10 References

1. Texas Instruments, *TPS65023x Power Management IC for Li-Ion and Li-Polymer Powered Systems* data sheet
2. Texas Instruments, *TPS2291xx, 5.5-V, 2-A, 37-mΩ On-Resistance Load Switch* data sheet
3. NXP Semiconductors, *i.MX 6Solo/6DualLite Family of Applications Processors for Consumer Products* Data Sheet (IMX6SDLCEC), Rev. 8, 09/2017
4. NXP Semiconductors, *i.MX 6Solo/6DualLite Family of Applications Processors for Industrial Products* Data Sheet (IMX6SDLIEC), Rev. 8, 09/2017
5. NXP Semiconductors, i.MX 6DualLite Power Consumption Measurement Application Note (AN4576), Rev. 1, 3/2013

Block Diagram Variations for i.MX 6 Processor Variants

A.1 System Block Diagram for i.MX 6SoloX

Figure 19 shows a modified system block diagram for the i.MX 6SLL processor variant. The maximum input voltage to the system, VSYS, is 5.5 V. The DCDC2 converter output voltage is set to 3.3 V because the VDD_HIGH_IN power input has a 3.6-V maximum input voltage. The DCDC2 converter output rail is also split off and wired to the VDDA_ADC_3P3 pin through a filter to decrease noise. The NVCC_xx GPIO power inputs are wired directly to the LDO1 and LDO2 regulators, which are set to 1.8 V and 3.3 V, respectively.

Changes in the processor variant are determined from the *i.MX 6SoloX Applications Processors for Consumer Products* Data Sheet.

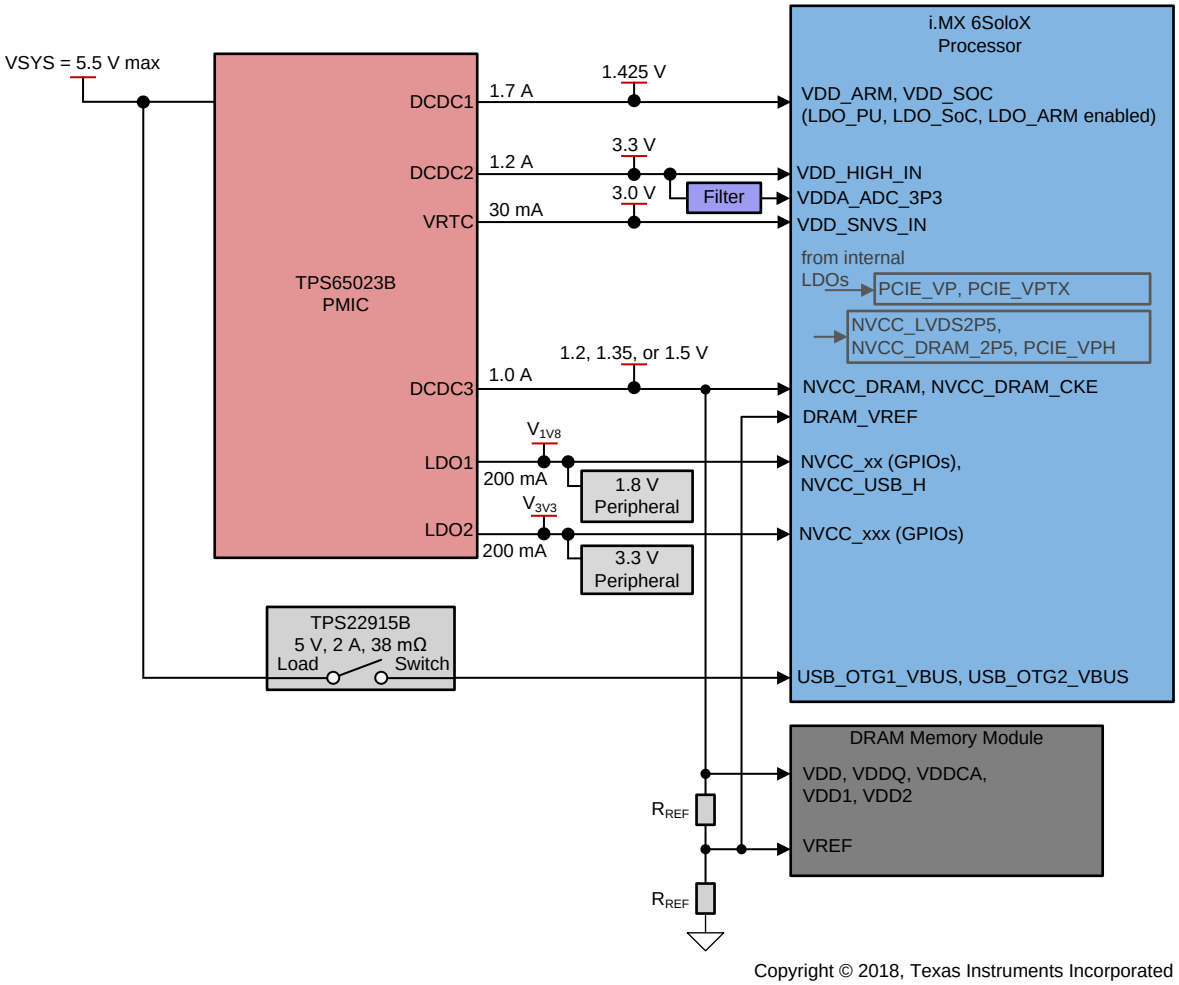

Figure 19. TPS65023 Power Solution Block Diagram for i.MX 6SoloX

A.2 System Block Diagram for i.MX 6SoloLite

Figure 20 shows a modified system block diagram for the i.MX 6SoloLite processor variant. The maximum input voltage to the system, VSYS, is 5.25 V again because the SoloLite is more similar to the Solo than the SoloX. Similarly, the DCDC2 converter output voltage is returned to 3 V because the VDD_HIGH_IN power input has a 3.3 V maximum input voltage. The NVCC18_IO and NVCC33_IO GPIO power inputs are wired directly to the LDO1 and LDO2 regulators, which are set to 1.8 V and 3.3 V, respectively.

Changes in the processor variant are determined from the *i.MX 6SoloLite Applications Processors for Consumer Products* Data Sheet.

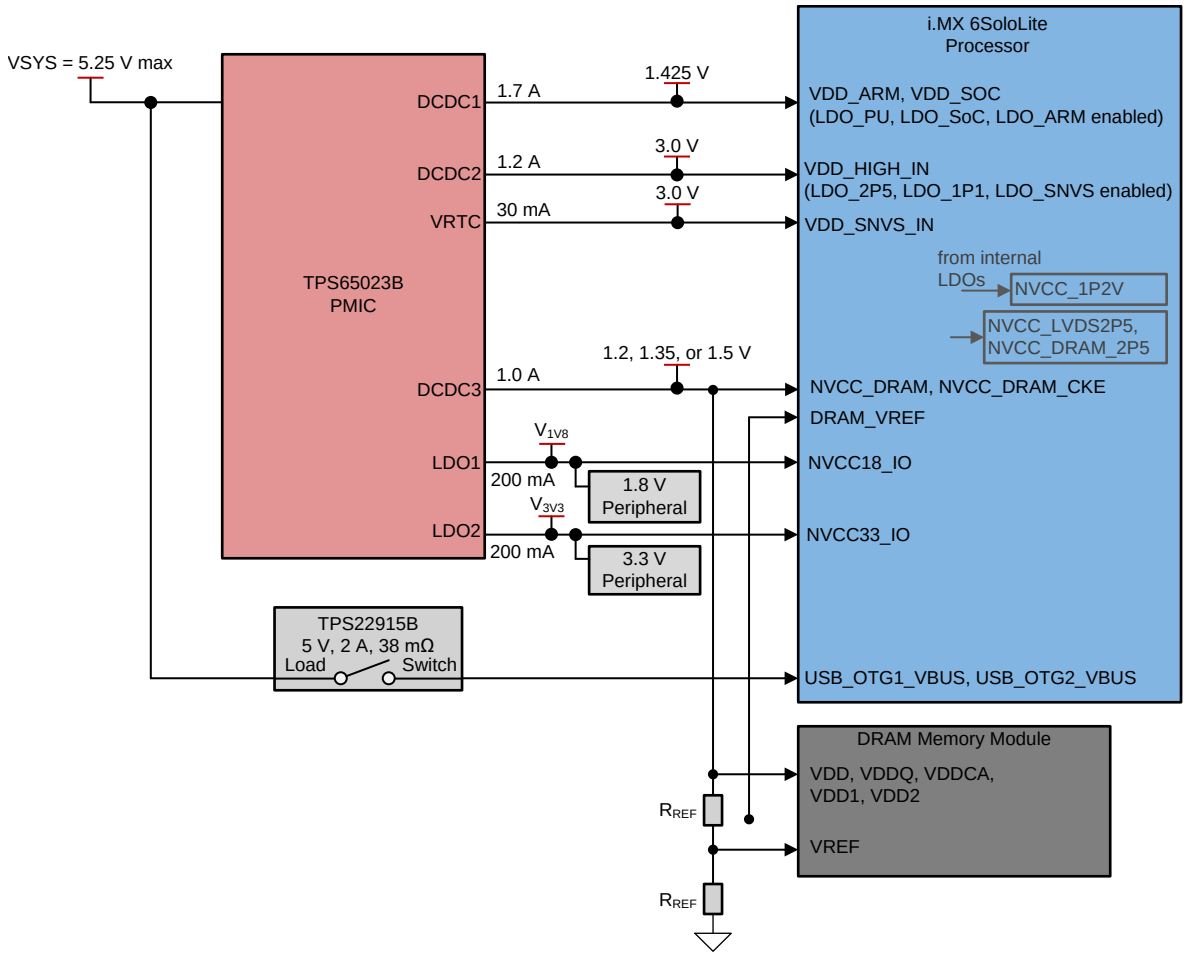

Figure 20. TPS65023 Power Solution Block Diagram for i.MX 6SoloLite

A.3 System Block Diagram for i.MX 6SLL

Figure 21 shows a modified system block diagram for the i.MX 6SLL processor variant, which does not include LDO regulators to generate the ideal voltages for the VDD_ARM and VDD_SOC rails. As a result, the DCDC1 converter output voltage is set to 1.15 V and both the VDD_ARM and VDD_SOC core rails must be in the *always-on* domain. The maximum input voltage to the system, VSYS, is 5.5 V. The DCDC2 converter output voltage is set to 3.3 V because the VDD_HIGH_IN power input has a 3.6 V maximum input voltage. The NVCC18_IO and NVCC33_IO GPIO power inputs are wired directly to the LDO1 and LDO2 regulators, which are set to 1.8 V and 3.3 V, respectively.

Changes in the processor variant are determined from the *i.MX 6SLL Applications Processors for Consumer Products* Data Sheet.

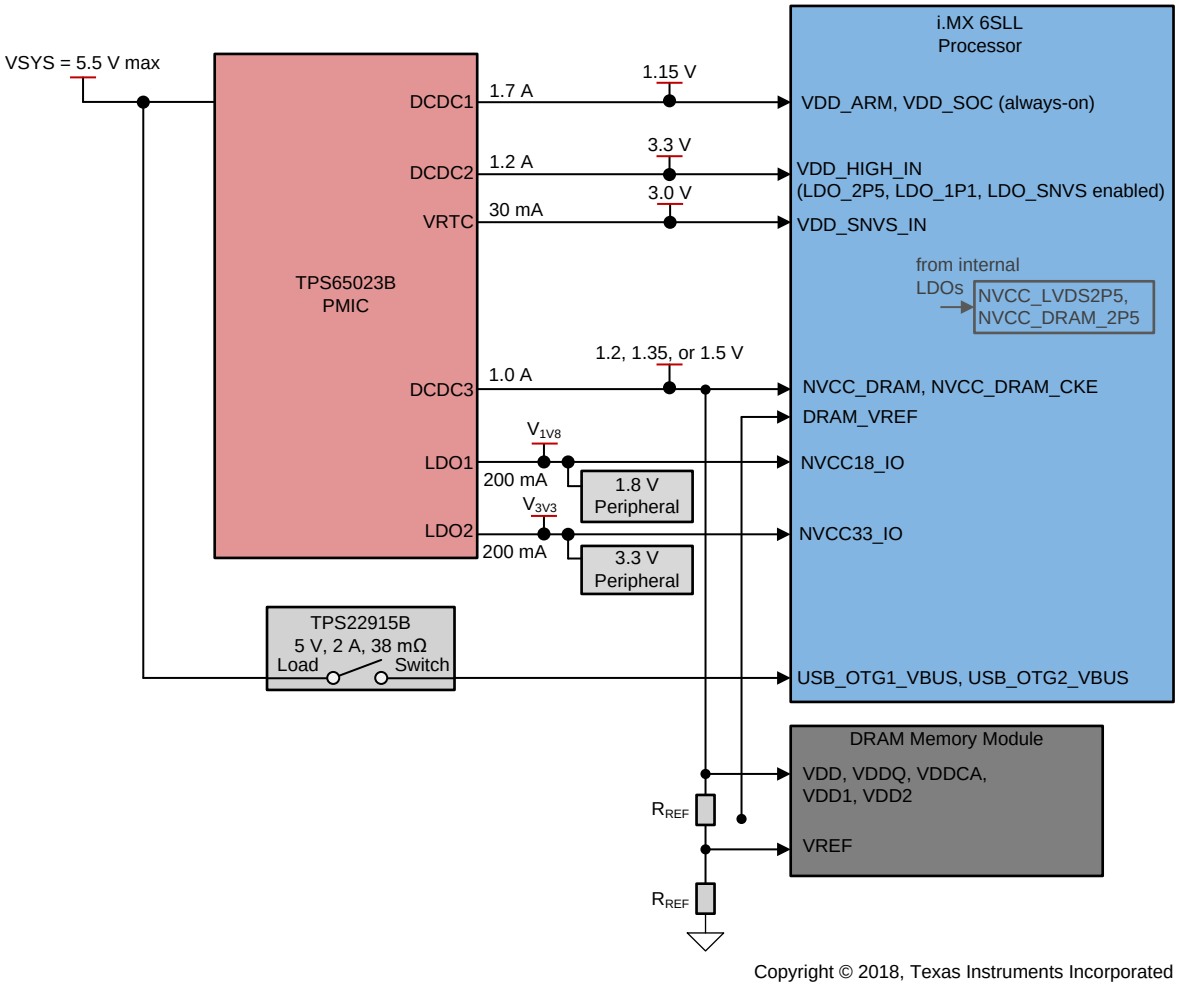

Figure 21. TPS65023 Power Solution Block Diagram for i.MX 6SLL

A.4 System Block Diagram for i.MX 6UltraLite and 6ULL

Figure 22 shows a modified system block diagram for the i.MX 6Ultralite and 6ULL processor variant. The DCDC1 converter output voltage is set to 1.375 V because the LDO regulators to generate the ideal voltages for the VDD_ARM and VDD_SOC rails are integrated again in this variant of the processor. The voltage is lowered as a result of the lower maximum clocking frequency of the UltraLite (696 MHz) and ULL (900 MHz) when compared to the other versions (1 GHz) of the processor that can be powered by the TPS65023 device. Aside from the change in voltage for the DCDC1 converter, the i.MX 6UltraLite and 6ULL are most similar to the i.MX 6SoloX.

Changes in the processor variant are determined from the *i.MX 6UltraLite Applications Processors for Consumer Products* Data Sheet and *i.MX 6ULL Applications Processors for Consumer Products* Data Sheet.

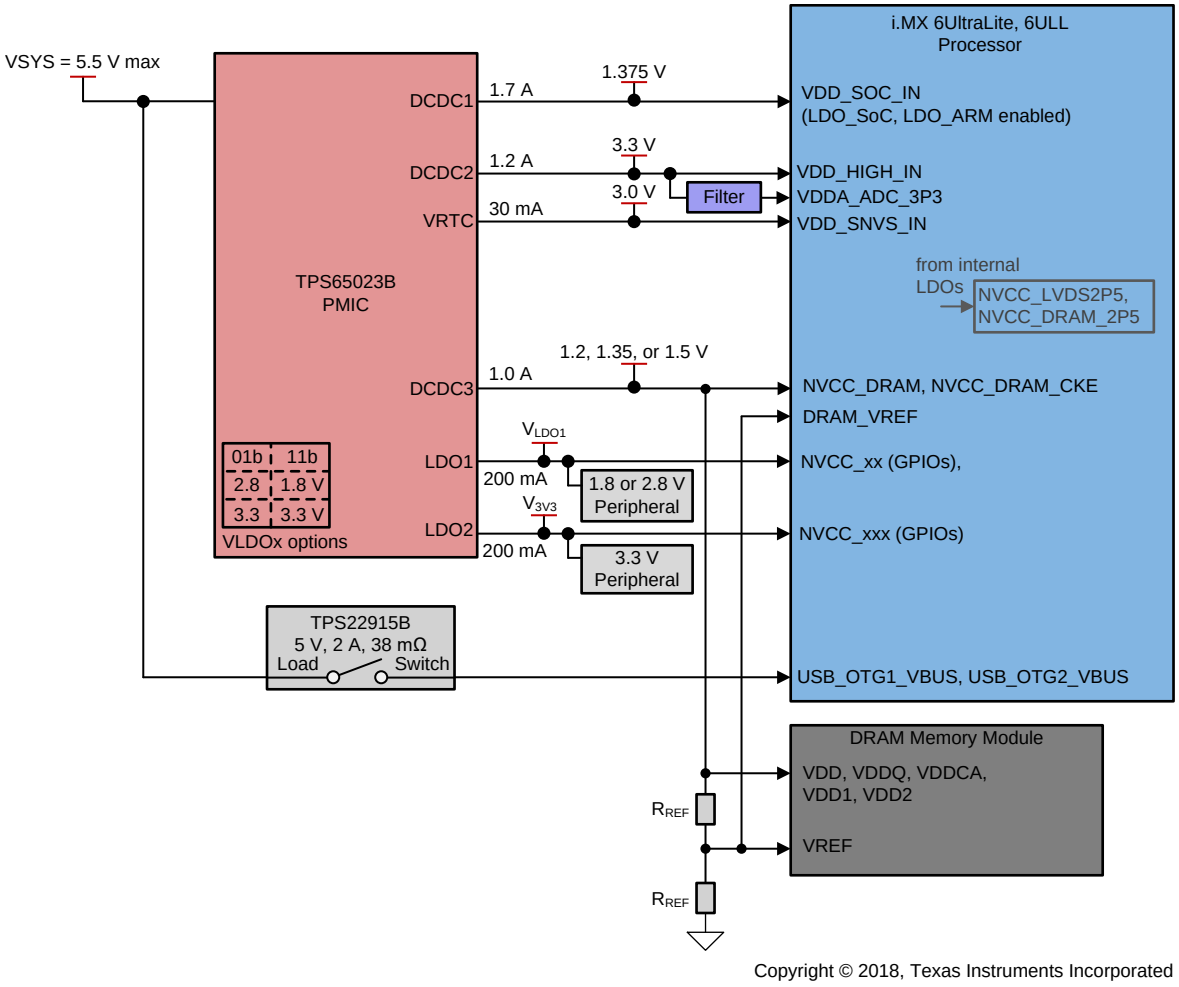

Figure 22. TPS65023 Power Solution Block Diagram for i.MX 6UltraLite and 6ULL

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