Application Report
SLVA883–April 2017

Timing of Load Switches

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ABSTRACT

Timing of load switches can vary depending on the operating conditions of the system and feature set of the device. At a glance, these variations can seem complex; but, when broken down, each operating condition and feature has a correlation to a change in timing. This application note goes into detail on how each condition or feature can alter the timing of a load switch so that the variations can be prepared for.

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1 Overview and Main Questions

1.1 Definition of Timing Parameters

First, let's look at the key behaviors of a load switch and how they relate to timing parameters. See Figure 1.

- Delay time, t_{DELAY}, accounts for the time required to prepare the subsystems of a load switch before the pass FET can be turned on. Delay time is defined as the time from the device being enabled until V_{OUT} starts to rise (typically to 10%).
- Rise time, t_{RISE}, is set by the slew rate of the load switch. Rise time is defined as the time for V_{OUT} to rise from 10% to 90%. The 10% and 90% marks are used for higher test and measurement accuracy during device characterization.
- Fall time, t_{FALL}, is heavily affected by the load resistance and load capacitance but can be influenced by devices with quick output discharge. Fall time is defined as the time for V_{OUT} to fall from 90% to 10%. The 90% and 10% marks are used for higher test and measurement accuracy during device characterization.
- On time, t_{ON}, represents the time for a switch to turn on. t_{ON} is typically defined as a combination of t_{DELAY} and t_{RISE} but can vary based on the test methodology used for each device. For this app note, t_{ON} will be defined as $t_{DELAY} + t_{RISE}$.
- Off time, t_{OFF}, represents the time for a switch to turn off but varies based on the test methodology used for each device. For this app note, t_{OFF} will be defined as the time from the device being disabled until V_{OUT} begins to fall (90%).

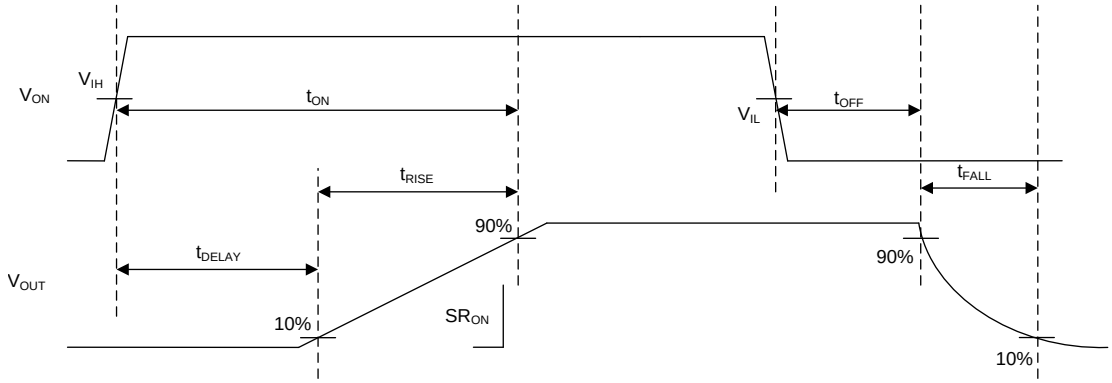

Figure 1. t_{DELAY}, t_{ON}, t_{OFF}, t_{RISE}, and t_{FALL} Waveforms

1.2 Alternative Timing Methods

The definitions above are the way the timing parameters will be addressed in this app note, but there are other ways of defining the above parameters. The waveform in Figure 2, shows:

- Delay time as the enable signal at 50% until V_{OUT} rises to 10%.
- On time as the enable signal at 50% until V_{OUT} rises to 50%.
- Off time as the enable signal at 50% until V_{OUT} falls to 50%.
- Rise time as V_{OUT} rising from 10% to 90%.
- Fall time as V_{OUT} falling from 90% to 10%.

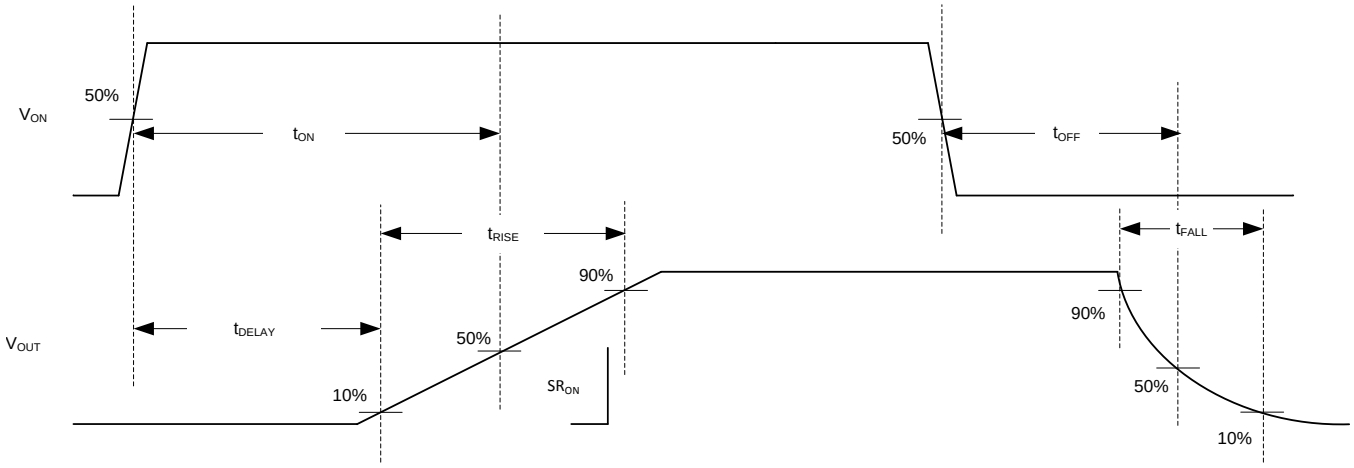

Figure 2. Alternative Timing Waveform

The on time for a device will be different depending on which method is used to calculate it. It is important to always double check the datasheet for how each device defines its timing.

1.3 Why is My Rise Time Different than Expected?

Rise Time is affected by many operating conditions and external components around a load switch. The main factors are: *Slew Rate*, *Load Resistance*, *Input Voltage* and *Bias Voltage*. The slew rate of the device controls how quickly the output rail ramps up to the input rail when the device turns on. The load resistance, with respect to the decreasing FET resistance, determines the point at which the output rail reaches 90% of the input. Input voltage is directly proportional to rise time, a higher input voltage results in a higher rise time. Bias voltage powers the charge pump which can improve rise time if the bias voltage is higher than the input voltage.

1.4 Why is My Fall Time Different than Expected?

Fall time is affected by *Load Capacitance* and *Quick Output Discharge* (part dependant). When a load switch is turned off the charge on the load capacitance needs to be discharged to bring the output rail down. Load resistance and load capacitance are directly proportional to the fall time based on RC capacitive discharging. Quick Output Discharge can be used to increase the current being pulled out of the load capacitance. Quick Output Discharge has a larger impact on discharging the load capacitance the larger the load resistance is.

1.5 Why Do NMOS and PMOS Pass FETs Affect Timing Differently?

NMOS and PMOS pass FETs behave differently while the FETs are turning on. NMOS rise time is less affected by external components (load resistance and load capacitance) while the rise time of PMOS is almost exclusively controlled by external components.

NMOS pass FETs have 4 key voltage parameters during turn on: input voltage, output voltage, gate voltage, and the V_{GS} threshold voltage. See Figure 3. The output starts at 0 V, rises to, and stops at the input voltage when the FET is fully on. The V_{GS} threshold voltage is the difference in voltage needed between the gate voltage and the output voltage for the output to begin to rise, the V_{GS} threshold voltage is typically around 0.7 V.

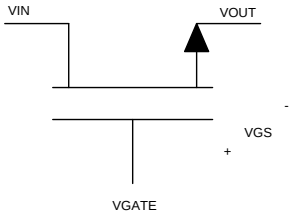

Figure 3. Voltages on NMOS FET

As the voltage on the gate begins to rise no change occurs at the output until the difference between the gate and output equals the V_{GS} threshold voltage. Once the V_{GS} threshold voltage has been hit, both the gate and output voltages increase linearly and parallel to each other. Once the output has reached the input voltage the output stops increasing.

PMOS pass FETs are pulled to ground to turnon. Once the gate voltage is low and the device turns on the input is immediately passed to the output. The amount of time it takes the gate voltage to reach 0V is typically uncontrolled or hard to control. This causes the output to very quickly rise up to the input voltage. Load resistance causes voltage division between the load and the FET resistance. A low load resistance results in a slower rise time while a high load resistance causes a quick rise time, See the *Load Resistance* section.

The way the output of an NMOS pass FET increases is dependant on how quickly the gate voltage increases and is negligibly affected by load capacitance and resistance. The way the output of a PMOS pass FET increase is heavily dependant on the load on the switch.

2 Effect of System Operating Specifications on Timing

Timing parameters of a load switch are affected by many typical operating conditions and system specifications such as: *Temperature*, *Load Resistance*, *Load Capacitance*, *Input Voltage*. The effect temperature has on the timing parameters can vary greatly from device to device depending on the specific design architecture. A larger load resistance will reduce t_{RISE} while increasing t_{FALL}. A larger load capacitance increases t_{FALL} based on RC capacitive discharging. Input voltage is directly proportional to t_{RISE}. Section 2.1 through Section 2.4 cover each of these topics individually.

2.1 Temperature

The two main subsystems of a load switch that are affected by temperature which result in a timing change are the V_{GS} threshold of the pass FET and the reference current of the charge pump. The V_{GS} threshold of the pass FET decreases as temperature increases. The reduction in the V_{GS} threshold reduces t_{DELAY}. The reference current of the charge pump controls how quickly the gate will ramp and in turn how quickly the output will rise. Typically, as temperature increases the reference current increases which causes the gate of the pass FET to charge faster. The increase in the reference current causes a reduction in both t_{DELAY} and t_{RISE}.

The overall affect on the device from an increase in temperature, in the case of the TPS22975, reduces t_{DELAY} and t_{RISE}, as shown in Figure 4; while t_{FALL} is relatively constant, as shown in Figure 5. Both figures are based on the following parameters: V_{IN} = 2.5 V, V_{BIAS} = 2.5 V, and CT = 1000 pF. Regardless of which V_{IN}, V_{BIAS}, and CT values are used, the change in the timing parameters, for the TPS22975, due to temperature is consistent.

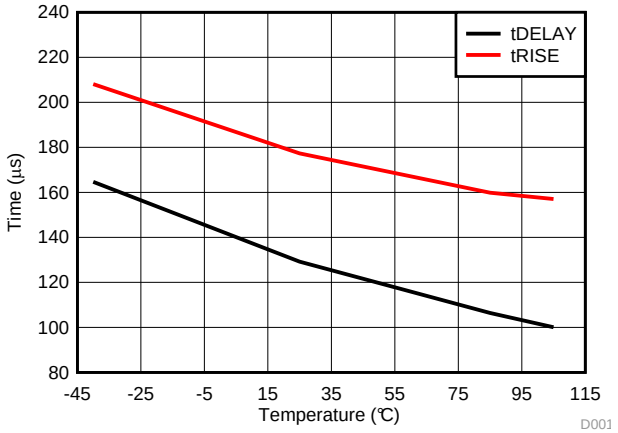

Figure 4. TPS22975 t_{RISE} and t_{DELAY} Across Temperature

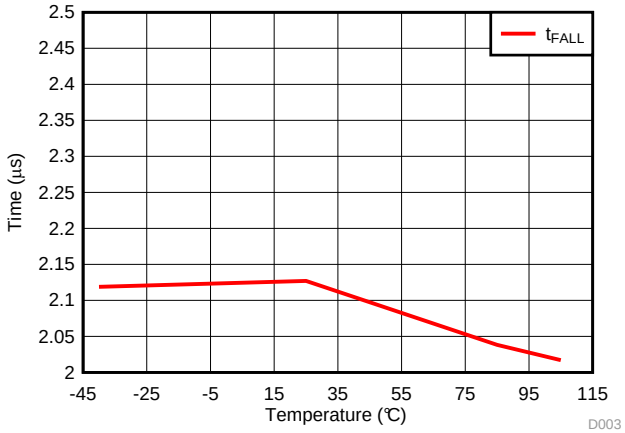

Figure 5. TPS22975 $_{FALL}$ Across Temperature

The overall affect on the device from an increase in temperature, in the case of the TPS22918, is different than the TPS22975. As temperature increases: t_{DELAY} linearly decreases while t_{RISE} linearly increases, as shown in Figure 6. Fall time is relatively constant, as shown in Figure 7. Both figures are based on the following parameters: V_{IN} = 2.5 V and CT = 1000 pF. Regardless of which V_{IN} and CT values are used, the change in the timing parameters, for the TPS22918, due to temperature is consistent.

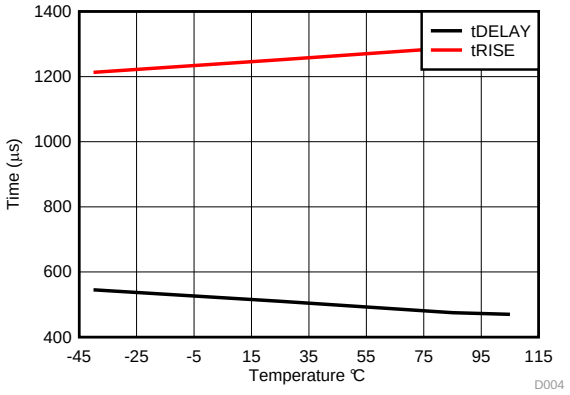

Figure 6. TPS22918 t_{RISE} and t_{DELAY} Across Temperature

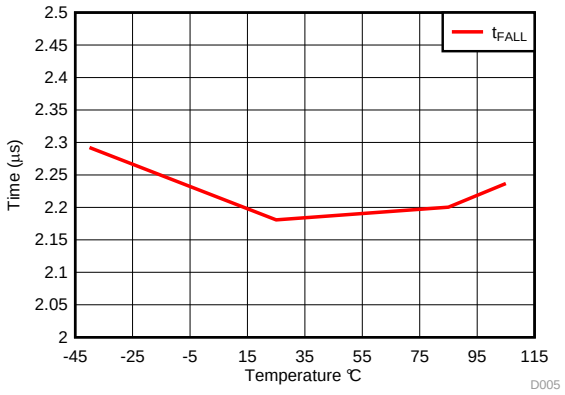

Figure 7. TPS22918 t_{FALL} Across Temperature

The TPS22975 is an example of both the switching threshold and the reference current changing with temperature resulting in a larger reduction of t_{DELAY} and t_{RISE} than the TPS22918. The TPS22918 is largely affected by the change in switching threshold, which is why t_{DELAY} decreases with increasing temperature; but the TPS22918 has a relatively constant reference current over temperature which is why t_{RISE} does not decrease with increasing temperature. The fact that t_{RISE} increases on the TPS22918 is due to many small parasitic changes that occur with increasing temperature.

Temperature also affects load resistance and load capacitance values. See the *Load Resistance* and *Load Capacitance* sections to see how they affect timing.

2.2 Load Resistance

The internal FET of the load switch can simply be modeled as a non-linear potentiometer, which starts typically in the 10s of MΩ and ends at R_{ON}(typically in 10s to 100s of mΩ). The FET resistance, R_{FET}, and the load resistance, R_{LOAD}, make a voltage divider circuit. See Figure 8.

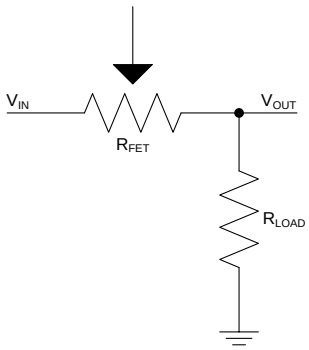

Figure 8. R_{FET} and R_{LOAD} Voltage Divider

If the load resistance is 500 Ω - the FET resistance will reach 55.5 Ω in time X, creating a 90% voltage divider resulting in t_{ON}.

If the load resistance is 10 Ω - the FET resistance will still reach 55.5 Ω in time X but this creates a 15% voltage divider rather than a 90%. This means a lower load resistance results in a longer time for the output to finish ramping.

Load resistance also affects t_{FALL}, as explained in Section 2.3.

2.3 Load Capacitance

As load capacitance and load resistance increase: t_{FALL} increases. The larger the load resistance or load capacitance is, the longer it will take to discharge the capacitor, resulting in a longer fall time.

Capacitance discharge follows Equation 1.

$$t_{FALL} = -R_L \times C_L \times \ln(V_{10\%}/V_{90\%}) \quad (1)$$

Where

- $V_{10\%}$ is 10% of the initial output voltage
- $V_{90\%}$ is 90% of the initial output voltage
- R_L is the load resistance
- C_L is the load capacitance

All the energy stored in the load capacitance has to discharge through the load resistance, for example let's use: a 0.1-uF load capacitance, a 500-Ω load resistance, and initial V_{OUT} = 5 V, see Equation 2.

$$t_{FALL} = -500\Omega \times 0.1uF \times \ln(0.5V/4.5V) = 110\mu sec \quad (2)$$

2.4 Input Voltage

As input voltage increases: t_{DELAY} and t_{RISE} increase. If the output rises at a constant rate, a higher voltage will take longer to reach. Rise time and delay time are directly proportional to input voltage.

For example, in the TPS22976, t_{RISE} and t_{DELAY} increase with increasing input voltage, see Figure 9 and Figure 10.

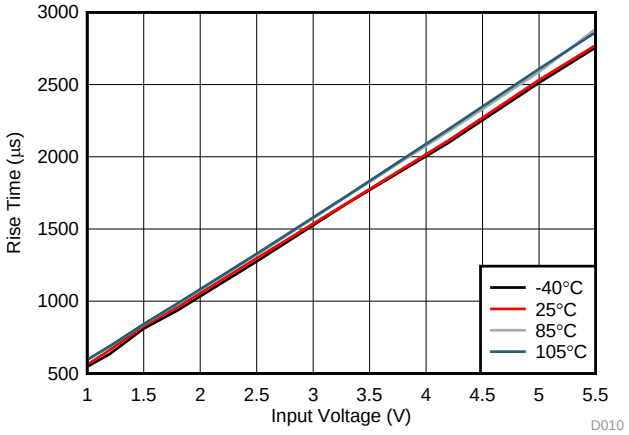

Figure 9. TPS22976 t_{RISE} vs V_{INPUT}

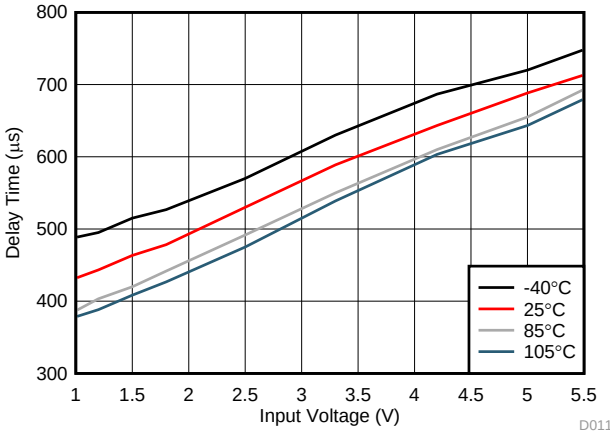

Figure 10. TPS22976 t_{DELAY} vs V_{INPUT}

3 Effects of Device Features on Timing

Timing parameters of a load switch are affected or controlled with device features such as: *Slew Rate*, *Bias Voltage*, and *Quick Output Discharge*. Slew rate directly controls the rise time of the load switch. Bias voltage can affect t_{RISE} and t_{DELAY} but the way timing is affected is part specific. Quick Output Discharge can be implemented to reduce t_{FALL}. Section 3.1 through Section 3.3 cover each of these topics individually in more detail.

3.1 Slew Rate

Slew rate is used to manually control the rise time of a device. Slew rate can be controlled by either selecting a part with an internally fixed slew rate or by selecting a part that has the ability to adjust the slew rate with external components.

An example of a integrated load switch with adjustable slew rate is the TPS22975 which uses a CT pin. An equation for slew rate is given in each datasheet for parts that have an adjustable slew rate, Equation 3 is pulled as an example from the TPS22975 datasheet (SLVSDD0).

This estimate does not apply for CT capacitor values less than 100 pF. For this device, values smaller than 100 pF have little describable impact on the slew rate because they are relatively small compared to the FET gate capacitance. Whereas a larger CT capacitance will be the dominant factor in determining the slew rate. This can be seen in Figure 11, the slopes of the CT = 0 pF and CT = 220 pF lines are marginally discernable from each other, showing minimal impact of a 220-pF CT capacitor over an open CT pin. In general, a lower CT capacitor value in this range results in higher deviation of the estimated slew rate from the actual slew rate as shown in Equation 3.

$$SR = 0.43 \times CT + 26 \quad (3)$$

Where

- SR = Slew Rate (in µs/V)
- CT = The capacitance value of the CT pin (in µF)
- The units for the constant 26 are µs/V.
- The units for the constant 0.43 are us/(V × pF)

Equation 3 is an approximation. Slew rate can be affected by the tolerance of the CT or dV/dt capacitor and the board parasitics around the device. Selecting a CT or dV/dt capacitor tolerance with the application in mind can help reduce unwanted board-to-board rise time variation. Proper board layout is important due to the low value CT or dV/dt capacitor value (100 pF to 1000 pF) being used. Capacitance due to board traces or other planes can be in the 10s to 100s of pF and can affect the overall capacitance on the pin. The CT or dV/dt capacitor should have the shortest traces available between the pin and ground. Refer to the datasheet (SLVSDD0) for a board layout example.

Slew rate affects rise time following Equation 4.

$$t_{RISE} = V_{OUT} \times SR \times 0.8 \quad (4)$$

Where

- t_{RISE} is the rise time (in µs)
- V_{OUT} is the final output voltage (in V)
- SR is the slew rate (in µs/V)
- 0.8 constant accommodates the 10% to 90% definition

Figure 11, from the TPS22958 datasheet (SLVSCX7), shows the change of t_{RISE} across V_{IN} with multiple slew rates due to different CT values ranging from 0 pF to 10 nF.

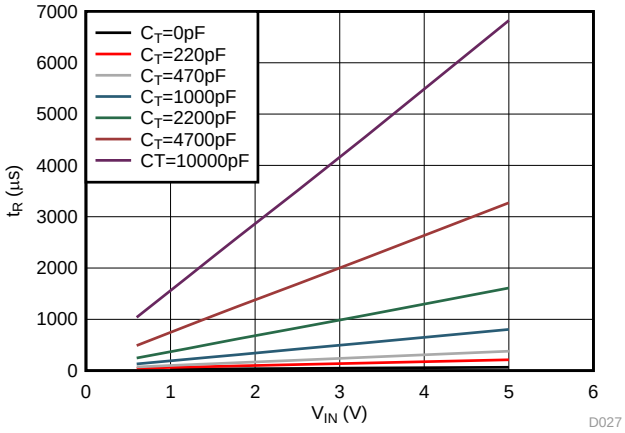

Figure 11. TPS22958 t_R vs V_{IN} With Changing CT

3.2 Bias Voltage

Bias Voltage, V_{BIAS}, can be utilized to reduce t_{RISE} and t_{DELAY}. V_{BIAS}, when available, is used to power the charge pump. In order for V_{BIAS} to affect t_{DELAY} and t_{RISE}, V_{BIAS} must be higher than V_{IN}. If V_{BIAS} is equal to V_{IN}, there will be no timing difference over just using V_{IN}.

Figure 12 (V_{BIAS} = 2.5V) and Figure 13 (V_{BIAS} = 5 V) from the TPS22976 datasheet (SLVSDE7) show that a higher V_{BIAS} results in a smaller delay time. Figure 12 only shows V_{IN} up to 2.5 V because it is not advised to operate a load switch with V_{IN} higher than V_{BIAS}.

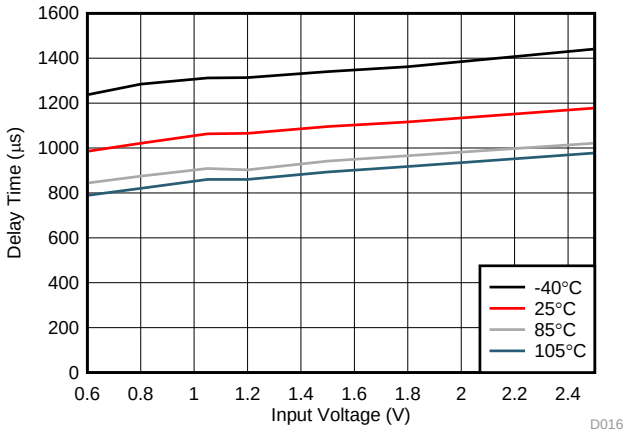

Figure 12. TPS22976 t_{DELAY} vs V_{INPUT}

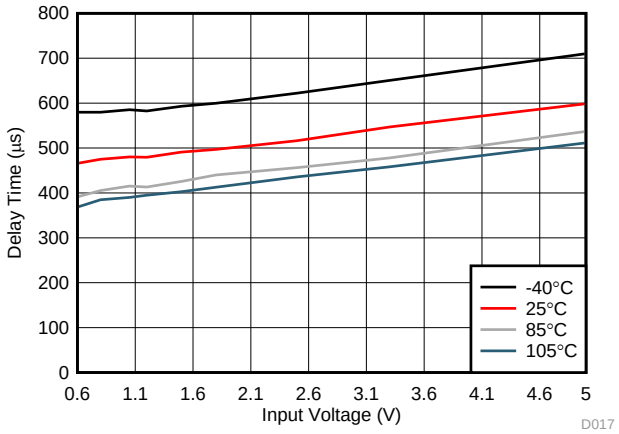

Figure 13. TPS22976 t_{DELAY} vs V_{INPUT}

The reduction in t_{RISE} is observed for the same reason that t_{DELAY} was reduced; a higher V_{BIAS} allows the device to turn on faster. Figure 14 from the TPS22958 datasheet (SLVSCX7) shows a V_{BIAS} sweep with V_{IN} at 2.5 V and CT = 1000 pF.

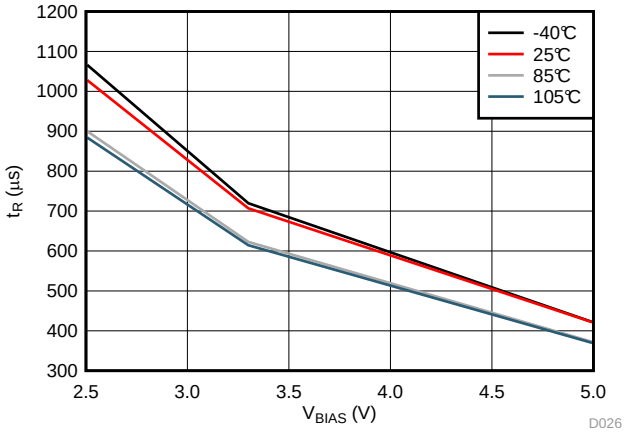

Figure 14. TPS22958 t_{RISE} vs V_{BIAS}

Typically, rise time decreases with an increasing V_{BIAS}, although some parts can be designed to have a flat rise time response with an increasing V_{BIAS} as seen in Figure 15 from the TPS22953 datasheet (SLVSCT5).

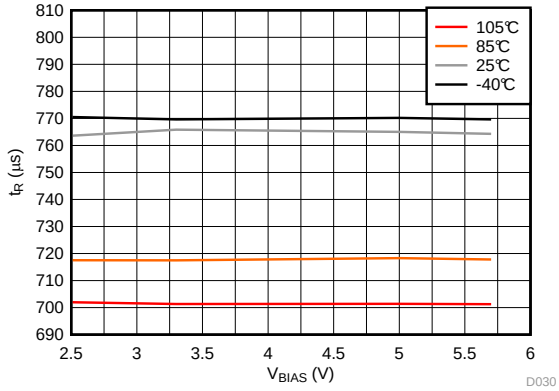

Figure 15. TPS22953 t_{RISE} vs V_{BIAS}

It is important to double check the AC characteristics of each device to verify its behavior.

3.3 Quick Output Discharge

Quick Output Discharge, QOD, is implemented with a bipolar transistor in series with an internal pull-down resistor. The way that the load capacitor is discharged with QOD depends on the operating mode of the transistor. The transistor operating modes are controlled by the bias voltage conditions of the transistor. As voltage on the capacitor falls, the transistor moves from forward-active mode into saturation then into cutoff mode.

- If the transistor is the forward-active mode, it acts as a constant current sink. This pulls current out of the load capacitance at a constant rate regardless of output voltage. An example circuit is shown in Figure 16. Discharging of a capacitor with a constant current sink follows Equation 5.

  $$V_{OUT}(t) = 1/C_L \times I_T \times t + V_{OUT}(0) \quad (5)$$

  Where

  - $V_{OUT}(t)$ is the output voltage at time t
  - C_L is the load capacitance
  - I_T is the current pulled to ground by the transistor
  - $V_{OUT}(0)$ is the initial output voltage

- If the transistor is in saturation mode, it acts as a resistor in series with the pull down resistor. This pulls current out of the load capacitance based on the output voltage at a given time. An example circuit is shown in Figure 17. In this mode, the current pulled out of the capacitor follows the typical *RC Discharge Equation* as described in the *Load Capacitance* section.
- Once the transistor reaches cutoff mode, the transistor opens the connection from the pull-down resistor to ground. Current will only follow through the load resistance now.

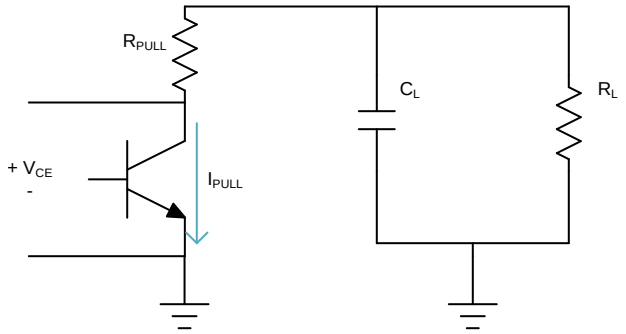

Figure 16. QOD - Constant Current

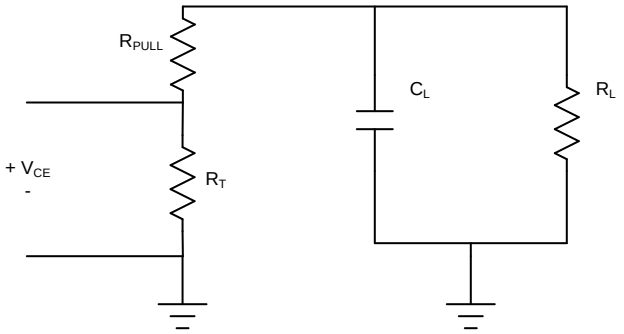

Figure 17. QOD - Resistive Pull-Down

4 Conclusion

When characterizing the timing of load switches within each system it is best to consider the effect of each of the above conditions, components, and features. Although seemingly complex when all combined together, each operating condition has a direct effect on each of the timing parameters. It is best to consult the datasheet to determine how each part will be affected by the operating specifications and features discussed in this app note.

5 References

1. *TPS22975 5.7V, 6A, 16mΩ Load Switch with Adjustable Rise Time & Optional QOD for Cost-Conscious Applications* (SLVSDD0)
2. *TPS22976 5.5V, 6A, 14mΩ, Dual Load Switch with Adj. Rise Time & Optional QOD for Cost-Conscious Applications* (SLVSDE7)
3. *TPS22958 5.5V, 4A 13mΩ Load Switch with Adjustable Rise Time and Optional Quick Output Discharge* (SLVSCX7)
4. *TPS22918 5.5V, 2A, 52mΩ Load Switch with Adjustable Rise Time and Adjustable Quick Output Discharge* (SLVSD76)
5. *TPS22953 5.7V, 5A, 14mΩ Load Switch with Voltage Monitoring and Reverse Current Protection*(SLVSCT5)

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